BSM-8800A
BSM-8800J
BSM-8800K

MU-881RA
MU-881RJ
MU-881RK

VD-881RA
VD-881RJ
VD-881RK

RY-881PA

AC-800PA
AC-800PJ
AR-800PA
AW-800PA
AP-800PA
AH-800PA
AE-800PA
AL-800PA
AP-851PA
AP-860PA
AG-800PA
AG-820PA
AG-830PA
ZR-800P
ZB-810PK
ZB-820PK
ZB-821PK
ZB-860PK

Life Scope 14
BEDSIDE MONITOR
BSM-8800

0634-000148F

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1-1 General

This service manual consists of information needed to service the Bedside Monitor, BSM-8800J/K, manufactured by Nihon Kohden Corporation.

For easy maintenance, the monitors provide a SELF CHECK PROGRAM system. This system continuously checks the condition of each circuit even when the monitor is operating. If there is any trouble in a circuit, an error code message is displayed on the screen.

To familiarize yourself quickly with the functions, a series of functional block diagrams and explanations have been provided.

NOTE

There is a separate service manual for the input box JA-860/880P.

The major differences between the various models are as follows:

Model	AC power requirement	Safety standard
MU-881RJ VD-881RJ (BSM-8800J)	110–125 V	(IEC)
MU-881RK VD-881RK (BSM-8800K)	220–240 V	(IEC)

1-2 Specifications

◆ Display

CRT	14 inches, colored
Waveform display method	Non-fade, moving method
Number of waveform traces	8 traces max.
Sweep speed	30 mm/sec.
Sweep time	6 sec.

◆ Display waveform

ECG1, ECG2, BP1, BP2, BP3, BP4, respiration, thermodilution waveform, CO_2 waveform, EEG1, EEG2, pulse waveform, external input

◆ Numerical data display

Heart rate, VPC rate,
BP1 (systolic, diastolic and mean)
BP2 (systolic, diastolic and mean)
BP3 (systolic, diastolic, or mean)
BP4 (systolic, diastolic, or mean)
NIBP (systolic, diastolic and mean)
respiration rate, T1, T2, ΔT, Tb
$ETCO_2$, SpO_2, ST level, O_2

◆ Trendgraph

Items	Heart rate, VPC rate, respiration rate apnea (time and frequency) BP1 to 4 (systolic, diastolic and mean) NIBP (systolic, diastolic and mean) T1, T2, Tb, $ETCO_2$, SpO_2, ST level, O_2
Event mark	Asystole, V.Fib, V.Tachy, VPC run, couplet, noise/measure off
Trend time	1 hour, 2 hours, 4 hours, 8+1 hours, and 24+1 hours

◆ Alarm

Alarm items	Vital signs alarm (high/low): Heart rate, respiration rate BP1 to BP4 (systolic, diastolic and mean) NIBP (systolic, diastolic and mean) T1, T2, ΔT, Tb ETCO$_2$, SpO$_2$, O$_2$ Apnea alarm Arrhythmia alarm External instrument alarm
Alarm indication	Vital signs or arrhythmia message is reverse shaded and an alarm tone sounds
Alarm suspend	Available (for a specified period of time)

◆ ECG measurement

ECG leads (AC-800P)	5-electrode lead ECG1: Ⅰ, Ⅱ, Ⅲ, aVR, aVL, aVF, V, MCL ECG2: Ⅱ (fixed) 3-electrode lead ECG1: Ⅰ, Ⅱ, Ⅲ ECG2: not available
ECG leads (ZB-810P)	Single-lead
ECG leads (ZB-820P)	Dual-lead
ECG leads (ZB-860P)	Ⅰ, Ⅱ, Ⅲ lead selectable
Defibrillation discharge protection	Provided
ESU interference filter	Provided
Pacing pulse limiter circuit	Provided
Filter	Diagnosis/monitoring selection In monitoring mode: drift rejection on/off and AC filter on/off are available
Frequency response	AC-800P: 0.05 to 100 Hz (diagnosis) 0.3 to 40 Hz (monitoring) Transmitter: 0.4 to 40 Hz
External output sensitivity	1 V/mV ±5%
Heart rate counting range	12 to 300 bpm
Alarm limits	High limit: 10 to 300 bpm Low limit: 5 to 295 bpm Asystole time: selection

◆ Respiration measurement

Measuring method	Impedance method or thermistor method
Respiration rate counting range	0 to 150 bpm
Alarm limits	High: 2 to 150 bpm Low: 0 to 148 bpm Apnea time: 10 to 40 seconds in 5 second steps

◆ Blood pressure measurement (invasive method)

Measuring range	−50 to +300 mmHg
Input sensitivity	50 μV/V/10 mmHg
BP waveform display scale	Common scale for BP1 to BP4 Separate scale: 2 scale for BP1 and BP2 to BP4 4 scale for BP1 to BP4 respectively
Display value	Systolic/diastolic/mean pressure of each BP channel
Alarm limits	Available for each pressure High: 2 to 300 mmHg Low: 0 to 298 mmHg
External output sensitivity	1 V/100 mmHg (BP1 only)
BP site label	AP, LAP, PAP, CVP, and ICP

◆ Temperature measurement

Thermistor probe	YSI-400 series
Measuring range	0 to 45 °C (hardwire system) 5 to 45 °C (telemetry system ZB-860P)
Number of channels	2
Alarm limits	High: 0.5 to 45.0 °C Low: 0 to 44.5 °C

◆ Cardiac output measurement

Measuring method	Thermodilution method
Measuring range	0.5 to 20 L/min
Measuring condition	Injection temperature: 0 to 25 °C Blood temperature: 15 to 45 °C Catheter size: 5F or 7F Injection volume: 3 cc, 5 cc, 10 cc (7F) 1 cc, 2 cc, 3 cc, 4 cc, 5 cc (5F) Catheter coefficient can be used
Injection temperature measurement method	Temperature probe or inline sensor
Alarm limits (Tb)	High: 15.5 to 45.0 °C Low: 15.0 to 44.5 °C

◆ EEG measurement

Number of channels	2
Display sensitivity	10 mm/100 μV ±10 % (×1) ×0.5, ×1, ×2, ×4
Defibrillator discharge protection	Provided
Frequency response	0.5 to 20 Hz

◆ SpO_2 measurement

Measuring range	50 to 100 %, in 1 % step
Measuring accuracy	$80\% \leqq SpO_2 \leqq 100\%$: ±2 % $50\% \leqq SpO_2 < 80\%$: ±3 %
Alarm limits	High: 51 to 100 % Low: 50 to 99 %

◆ Non-invasive blood pressure measurement

Measuring method	Oscillometric
Display value	Systolic, diastolic, mean pressure
Pressure display range	AP-851PA (adults/children): 10 to 300 mmHg AP-851PA (neonates): 5 to 200 mmHg AP-860PA: 0 to 290 mmHg
Accuracy	AP-851PA: ±4 mmHg AP-860PA: ±3 mmHg (0 to 150 mmHg) ±2 mmHg (150 to 290 mmHg)
Measuring range	AP-851PA (adults/children) Systolic: 60 to 260 mmHg Mean: 45 to 235 mmHg Diastolic: 40 to 220 mmHg AP-851PA (neonates) Systolic: 40 to 180 mmHg Mean: 35 to 155 mmHg Diastolic: 20 to 140 mmHg AP-860PA Systolic: 50 to 260 mmHg Mean: 40 to 240 mmHg Diastolic: 20 to 220 mmHg
Activation of measurement	Manual Continuous: 5 minutes Automatic: 1, 2.5, 5, 10, 15, 30, 60 minute interval, OFF
Safety	Cuff pressure limiter: >301 mmHg (AP-851PA) >300 mmHg (AP-860PA) Rapid deflation in case of power failure
Alarm limits	High: 15 to 260 mmHg Low: 10 to 255 mmHg

◆ CO$_2$ measurement

Measuring range	0 to 100 mmHg, in 1 mmHg step
Accuracy	$0\ \text{mmHg} \leqq \text{CO}_2 \leqq 70\ \text{mmHg}$: ±2 mmHg $70\ \text{mmHg} < \text{CO}_2 \leqq 100\ \text{mmHg}$: ±5 mmHg
CO$_2$ curve display scale	20 mmHg, 40 mmHg, 80 mmHg
Alarm limits	High: 12 to 100 mmHg Low: 10 to 98 mmHg

◆ O$_2$ measurement

Measuring range	0 to 100 %, in 1 % step
Accuracy	±3 % (when calibrated with air) ±2 % (when calibrated with 100 % O$_2$ gas)
Alarm limits	High: 1 to 100 % Low: 0 to 99 %

◆ Arrhythmia recall

VPC detection method	Software algorithm (template matching method)
VPC counting range	0 to 99 beats/minute 0 to 9999 beats/hour
Arrhythmia alarm	Asystole, V.Fib, V.Tachy, VPC run, couplet, bigeminy, early VPC, and Freq.VPC
Recall display mode	Recall waveform with event history, HR trend or VPC rate trend
Number of recall files	32 (ECG1 only) 16 (ECG1 + ECG2 or ECG1 + P1)
Storage time per file	8 seconds

◆ Interbed function

Review of another patient for alarm contents, waveform and vital signs

◆ ST level

Number of recall files	7 files (8 waveforms/file)
Trend time	8+1 hours, 24+1 hours 1 hour, 2 hour, 4 hour

◆ Vital signs list

Items	Heart rate, VPC rate, respiration rate BP1, BP2 (systolic, diastolic and mean) BP3, BP4 (mean) NIBP (systolic, diastolic and mean) SpO$_2$, ETCO$_2$, T1, T2, Tb
Number of lists	120

◆ Hemodynamics list

Items	HR, CO, CI, ASP, ADP, AMP, PASP, PADP, PAMP, PCWP, CVP, SVI, LSWI, SVRI, PVRI, RSWI, RPP, CPP
Number of lists	16

◆ External output

Analog output	ECG connector (front panel): ECG1 BP1 connector (front panel): BP1 CNS or WS connector (rear panel): ECG1, ECG2, BP1, BP2, BP3, BP4, respiration, EEG1, EEG2, CO_2, external input (8 channels are available)
Logic output	CNS connector (rear panel): Alarm, ECG measure ON/OFF
RS-232C interface	RS232C connector (rear panel): Output to the personal computer

◆ Power requirement

Line voltage	MU-881RA, VD-881RA: 117 V AC, 60 Hz MU-881RJ, VD-881RJ: 110, 117, 125 V AC, 50/60 Hz MU-881RK, VD-881RK: 220, 240 V AC, 50/60 Hz
Power consumption	MU-881R: 120 VA (max.) VD-881R: 170 VA (max.)

◆ Environment

Operating temperature	5 – 40 °C 10 – 35 °C (CO_2 sensor)
Operating humidity	30 – 90 % RH

◆ Safety standard

MU	IEC601-1, class I, type BF (AG-800PA, AG-820PA, AP-851PA, AL-800PA), type CF (others)
VD	IEC601-1, class I, type B
Transmitter	IEC601-1, type CF

◆ Dimensions and weight

MU	361 W × 200 H × 400 D mm, 18 kg
VD	370 W × 350 H × 430 D mm, 25 kg
RY	320 W × 50 H × 85 D mm, 0.8 kg

◆ Transmitter

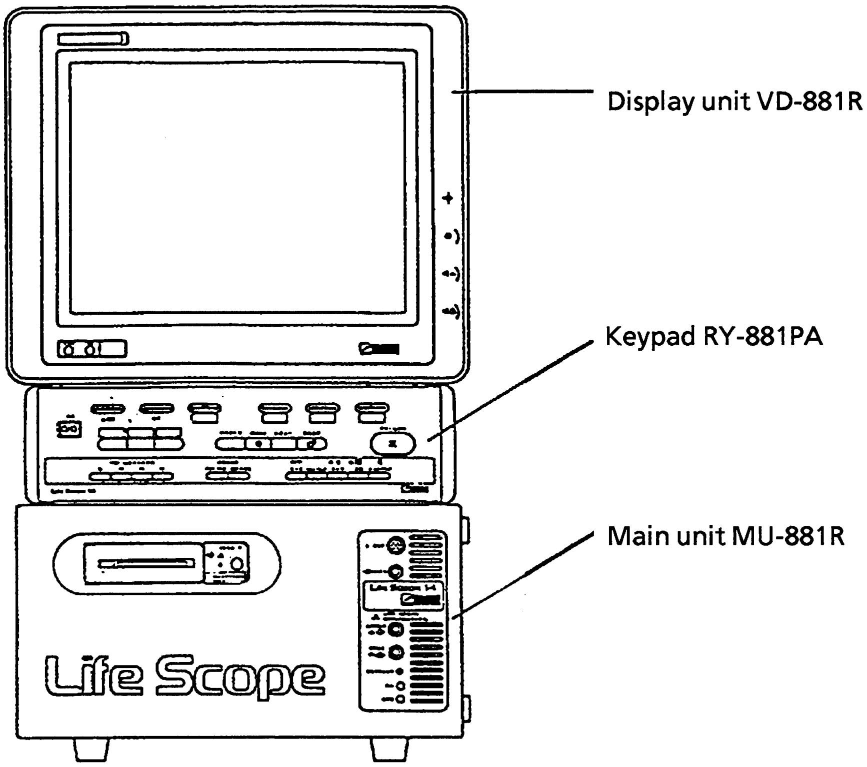
Transmitter frequency	420 to 450 MHz, 12.5 kHz step
	Group J1: 420.0500 to 421.0375 (80 ch)
	Group J2: 424.4875 to 425.9750 (120 ch)
	Group J3: 429.2500 to 429.7375 (40 ch)
	Group J4: 440.5625 to 441.5500 (80 ch)
	Group J5: 444.5125 to 445.5000 (80 ch)
	Group J6: 448.6750 to 449.6625 (80 ch)
Transmission power	0.3 mW (ZB-810P, ZB-820P)
	0.4 mW (ZB-860P)
Modulation method	FSK

◆ Receiver

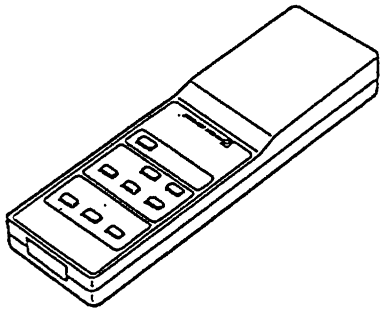
Antenna	Space diversity
Reception frequency	Synthesizer method
	420 to 450 MHz
EMI radiation	4 nW max.

1-3 Panel Explanation

1-3-1 Bedside Monitor, BSM8800

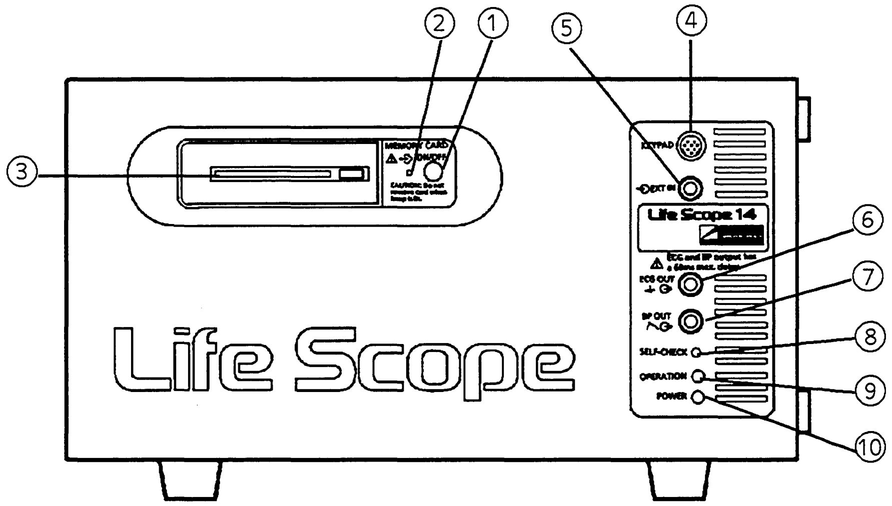

Display unit VD-881R
Keypad RY-881PA
Main unit MU-881R
Life Scope

Remote controller RY-001PK

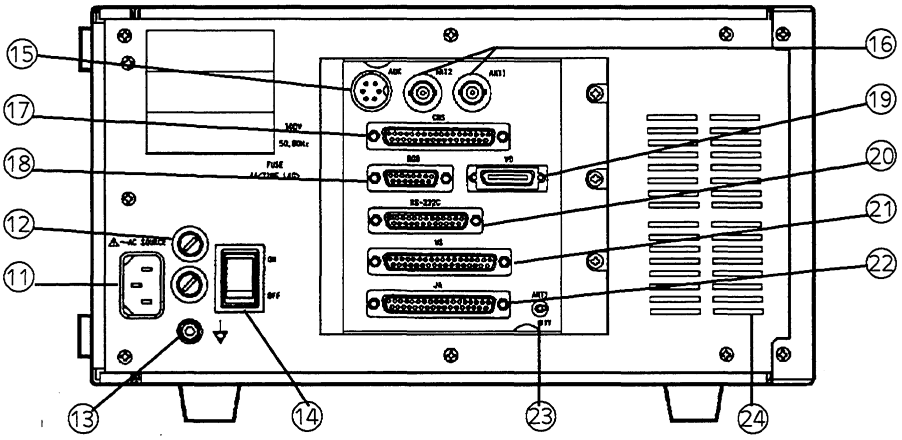


1-3-2 Main Unit, MU-881R

Front

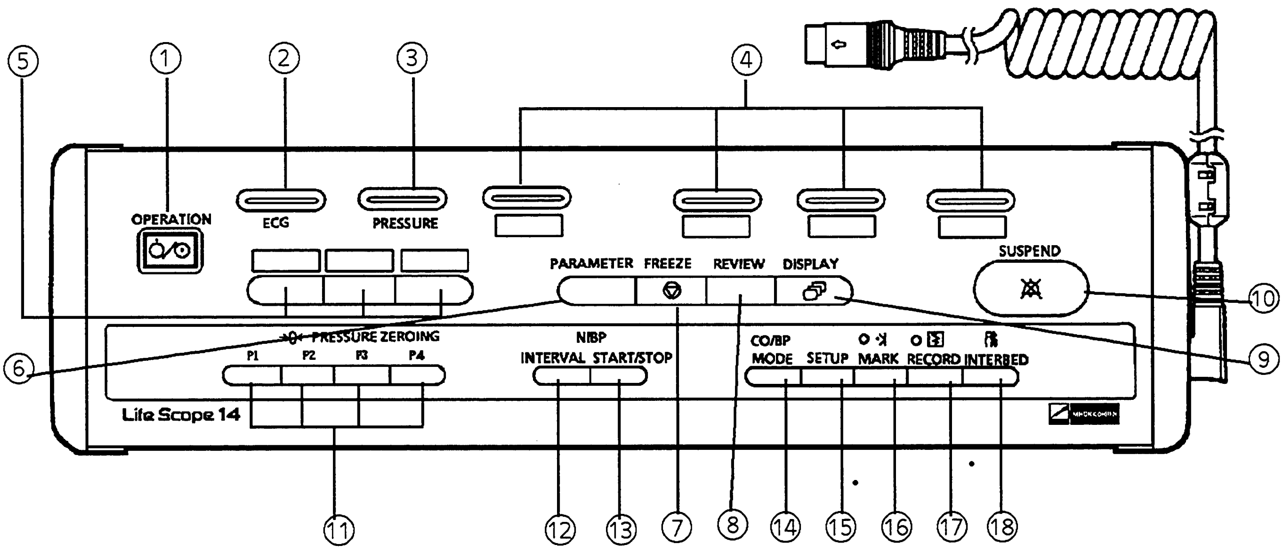

②
①
⑤
④
③
MEMORY CARD
ON/OFF
KEYPAD
EXT IN
Life Scope 14
⑥
ECG OUT
⑦
BP OUT
⑧
SELF-CHECK
OPERATION
⑨
POWER
⑩
Life Scope

Rear


⑮
⑯
AUX
ANT2
ANT1
⑰
CNS
⑲
⑱
RGB
VD
⑳
RS-232C
⑫
㉑
WS
⑪
㉒
JA
ON
OFF
⑬
⑭
㉓
㉔

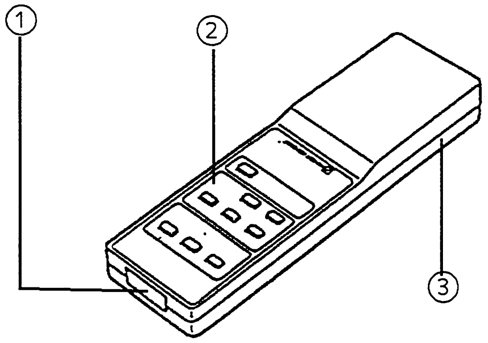
Name	Name
① Memory card switch*	⑬ Equipotential
② Memory card lamp*	⑭ Power switch
③ Memory card slot*	⑮ AUX connector
④ Keypad connector	⑯ ANT1, ANT2 connector
⑤ EXT INPUT connector	⑰ CNS connector
⑥ ECG1 output connector	⑱ RGB output connector
⑦ BP1 output connector	⑲ VD connector
⑧ Self check key	⑳ RS-232C connector
⑨ Power indication lamp	㉑ WS connector
⑩ Main power indication lamp	㉒ JA connector
⑪ AC inlet	㉓ DIV/ANT selection switch
⑫ Fuse holder	㉔ Ventilator

1-3-3 Keypad, RY-881PA

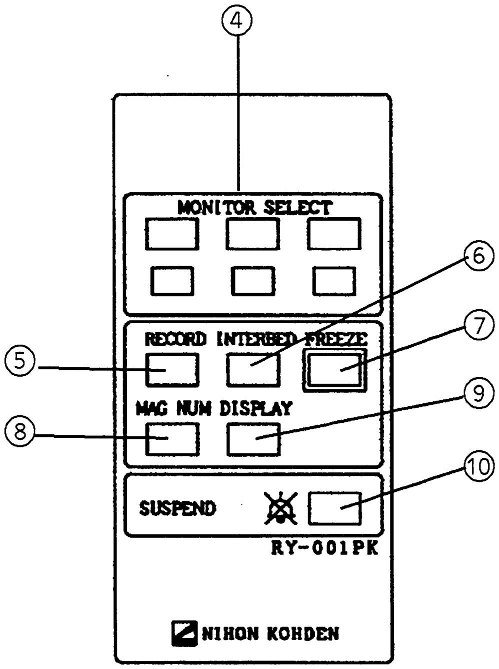

⑤
①
②
③
④
OPERATION
ECG
PRESSURE
SUSPEND
PARAMETER
FREEZE
REVIEW
DISPLAY
⑩
⑥
PRESSURE ZEROING
P1
P2
P3
P4
NIBP
INTERVAL
START/STOP
CO/BP
MODE
SETUP
MARK
RECORD
INTERBED
⑨
Life Scope 14
⑪
⑫
⑬
⑦
⑧
⑭
⑮
⑯
⑰
⑱

Name	Name
① Power switch	⑩ SUSPEND key
② ECG key (Multi-function key)	⑪ PRESSURE ZEROING keys
③ BP key (Multi-function key)	⑫ NIBP INTERVAL key
④ Multi-function keys 3 to 6	⑬ NIBP START/STOP key
⑤ Universal keys	⑭ CO/BP MODE key
⑥ PARAMETER key	⑮ SETUP key
⑦ FREEZE key	⑯ MARK key
⑧ REVIEW key	⑰ RECORD key
⑨ DISPLAY key	⑱ INTERBED key

1-3-4 Remote Control, RY-001PK

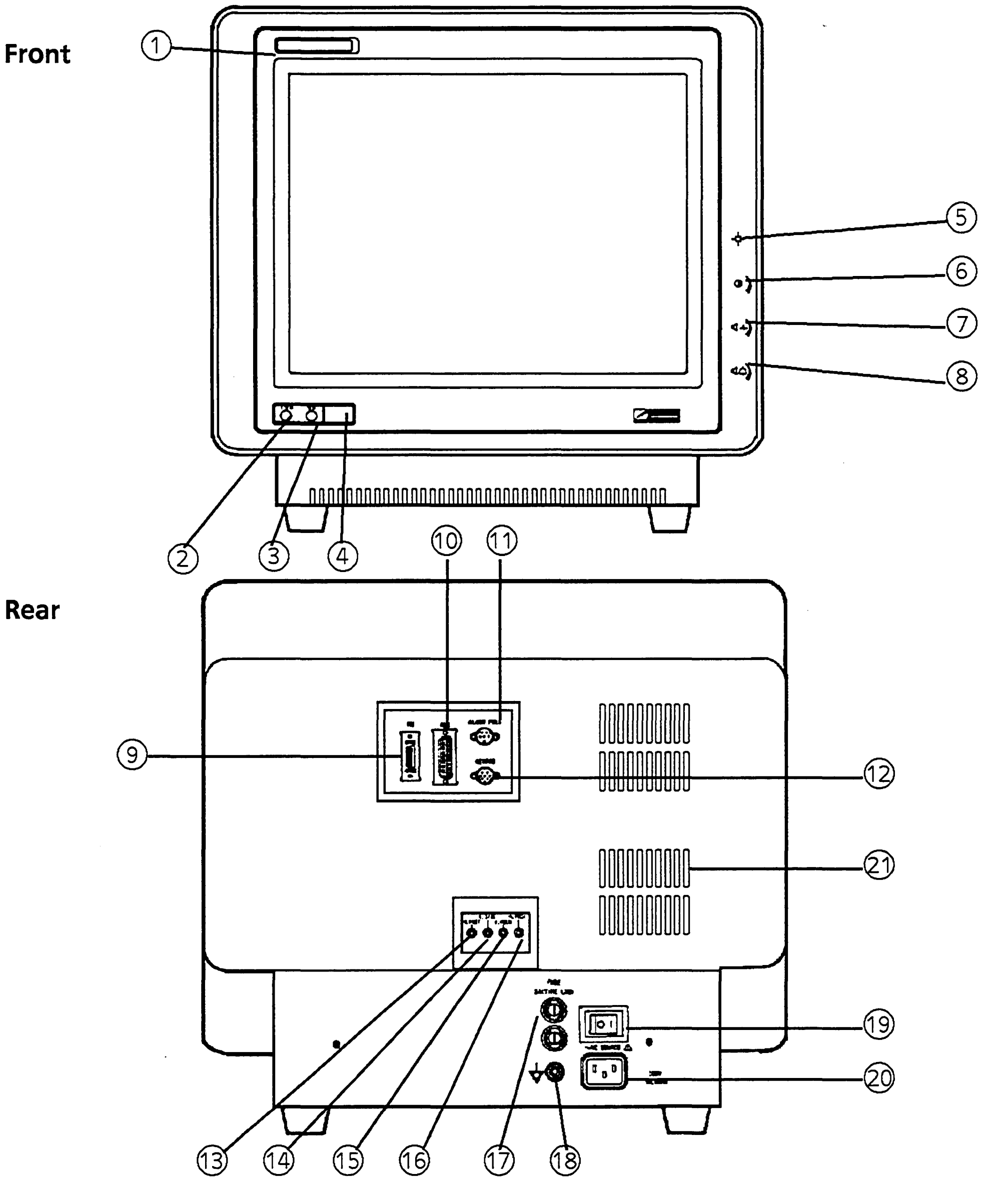


Operation panel


④
MONITOR SELECT
⑥
RECORD INTERBED FREEZE
⑦
⑤
MAG NUM DISPLAY
⑨
⑧
⑩
SUSPEND
RY-001PK
NIHON KOHDEN

Name
① Signal emitter
② Operation panel
③ Battery cover
④ Monitor select key
⑤ RECORD key
⑥ INTERBED key
⑦ FREEZE key
⑧ Large measurement data display key
⑨ DISPLAY key
⑩ SUSPEND key

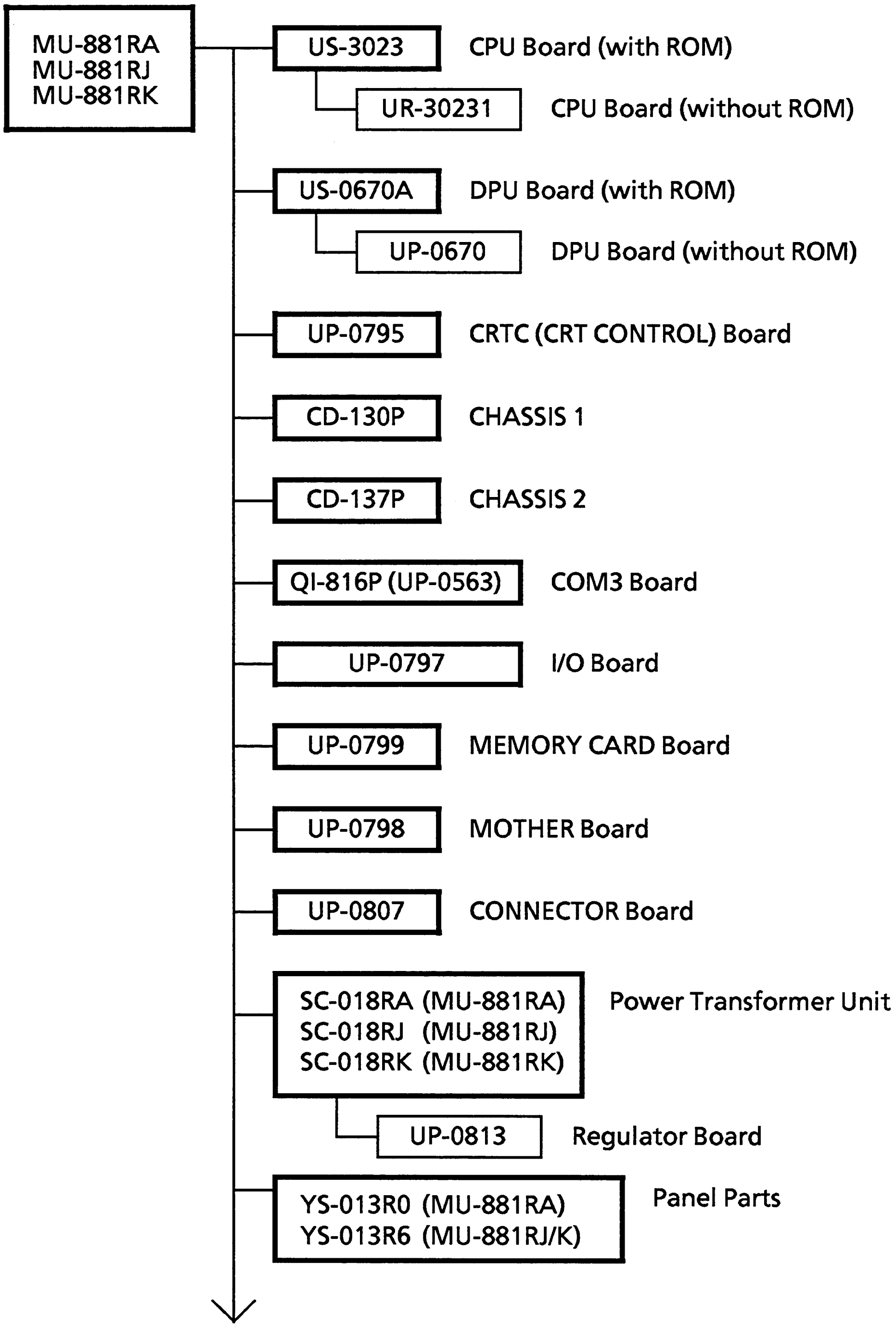
1-3-5 Display Unit, VD-881R

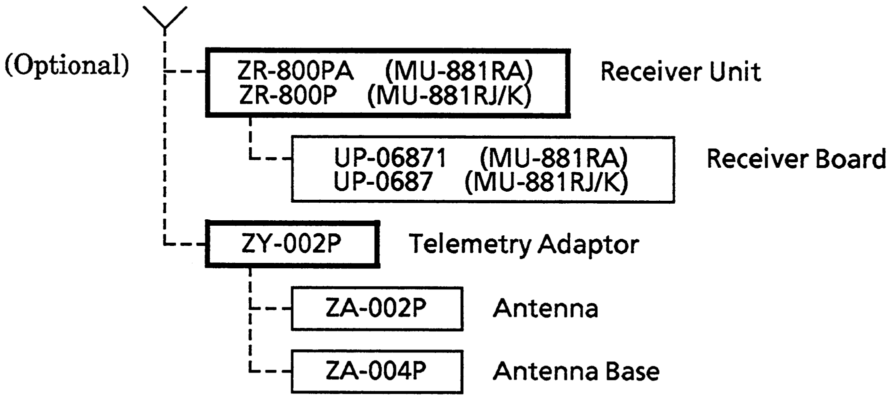


Name	Name
① Remote controller label position	⑫ Keypad connector
② Main power indication lamp	⑬ Vertical position control setting
③ Power indication lamp	⑭ Vertical amplitude control setting
④ Remote control sensor	⑮ Vertical synchronism control setting
⑤ Brightness control setting	⑯ Horizontal position control setting
⑥ Contrast control setting	⑰ Fuse holder
⑦ Synchronous sound control setting	⑱ Equipotential
⑧ Alarm volume control setting	⑲ Power switch
⑨ VD connector	⑳ AC inlet
⑩ VIDEO connector	㉑ Speaker
⑪ Alarm pole connector	

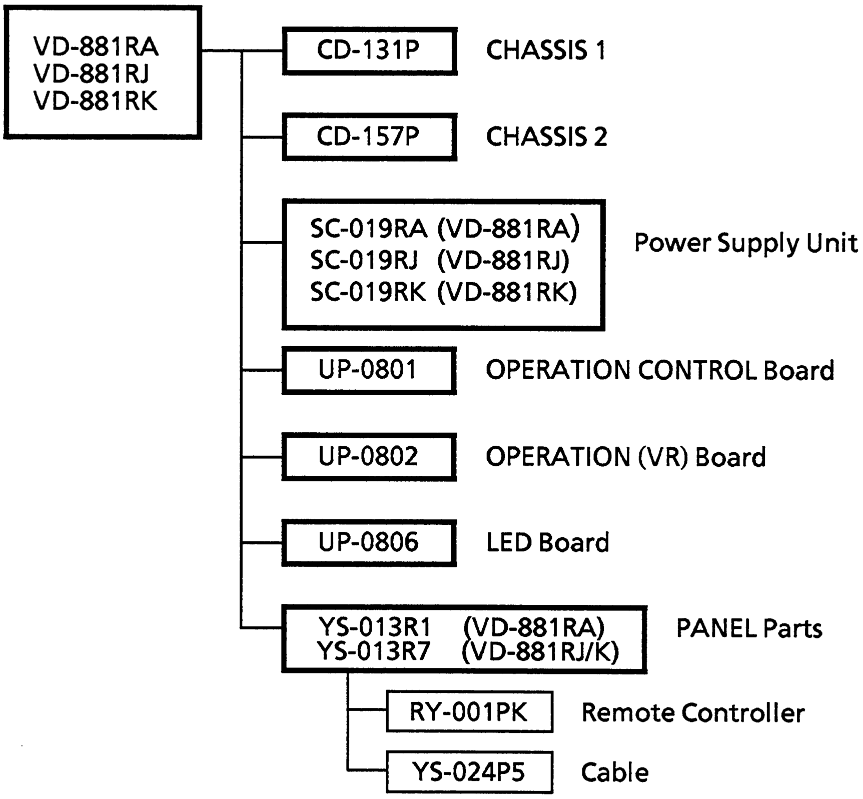
1-4 Composition

1-4-1 Main Unit

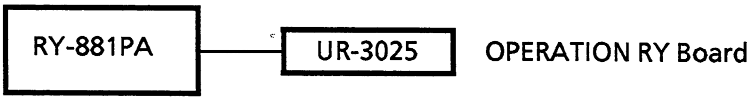

MU-881RA
MU-881RJ
MU-881RK
US-3023
CPU Board (with ROM)
UR-30231
CPU Board (without ROM)
US-0670A
DPU Board (with ROM)
UP-0670
DPU Board (without ROM)
UP-0795
CRTC (CRT CONTROL) Board
CD-130P
CHASSIS 1
CD-137P
CHASSIS 2
QI-816P (UP-0563)
COM3 Board
UP-0797
I/O Board
UP-0799
MEMORY CARD Board
UP-0798
MOTHER Board
UP-0807
CONNECTOR Board
SC-018RA (MU-881RA)
SC-018RJ (MU-881RJ)
SC-018RK (MU-881RK)
Power Transformer Unit
UP-0813
Regulator Board
YS-013R0 (MU-881RA)
YS-013R6 (MU-881RJ/K)
Panel Parts


(Optional)
ZR-800PA (MU-881RA)
ZR-800P (MU-881RJ/K)
Receiver Unit
UP-06871 (MU-881RA)
UP-0687 (MU-881RJ/K)
Receiver Board
ZY-002P
Telemetry Adaptor
ZA-002P
Antenna
ZA-004P
Antenna Base

1-4-2 Display Unit

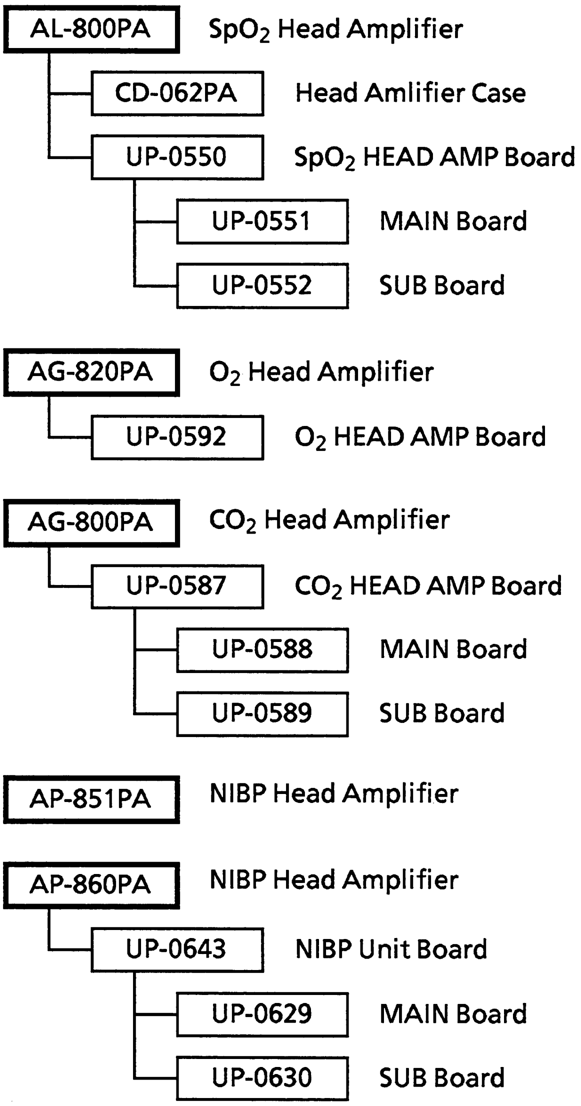

VD-881RA
VD-881RJ
VD-881RK
CD-131P
CHASSIS 1
CD-157P
CHASSIS 2
SC-019RA (VD-881RA)
SC-019RJ (VD-881RJ)
SC-019RK (VD-881RK)
Power Supply Unit
UP-0801
OPERATION CONTROL Board
UP-0802
OPERATION (VR) Board
UP-0806
LED Board
YS-013R1 (VD-881RA)
YS-013R7 (VD-881RJ/K)
PANEL Parts
RY-001PK
Remote Controller
YS-024P5
Cable

1-4-3 Keypad


RY-881PA
UR-3025
OPERATION RY Board

1-4-4 Head Amplifiers

- AC-800P ECG/Respiration Head Amplifier
  - Chassis parts
  - UP-0272 ECG HEAD AMP Board
- AE-800PA EEG Head Amplifier
  - CD-050PA Head Amlifier Case
  - UP-0420 EEG HEAD AMP Board
    - UP-0421 MAIN Board
    - UP-0422 SUB Board
- AH-800PA Cardiac Output Head Amplifier
  - Head Amlifier Case
  - UP-0318 CO HEAD AMP Board
- AP-800PA Blood Pressure Head Amplifier
  - Head Amlifier Case
  - UP-0369 PRESS HEAD AMP Board
- AR-800PA Respiration Head Amplifier
  - CD-063PA Head Amlifier Case
  - UP-0548 THERMISTOR RESP HEAD AMP Board
- AW-800PA Temperature Head Amplifier
  - Chassis parts
  - UP-0319 TEMP HEAD AMP Board



- AL-800PA SpO$_2$ Head Amplifier
  - CD-062PA Head Amlifier Case
  - UP-0550 SpO$_2$ HEAD AMP Board
    - UP-0551 MAIN Board
    - UP-0552 SUB Board

- AG-820PA O$_2$ Head Amplifier
  - UP-0592 O$_2$ HEAD AMP Board

- AG-800PA CO$_2$ Head Amplifier
  - UP-0587 CO$_2$ HEAD AMP Board
    - UP-0588 MAIN Board
    - UP-0589 SUB Board

- AP-851PA NIBP Head Amplifier

- AP-860PA NIBP Head Amplifier
  - UP-0643 NIBP Unit Board
    - UP-0629 MAIN Board
    - UP-0630 SUB Board

1-4-5 Blank Unit

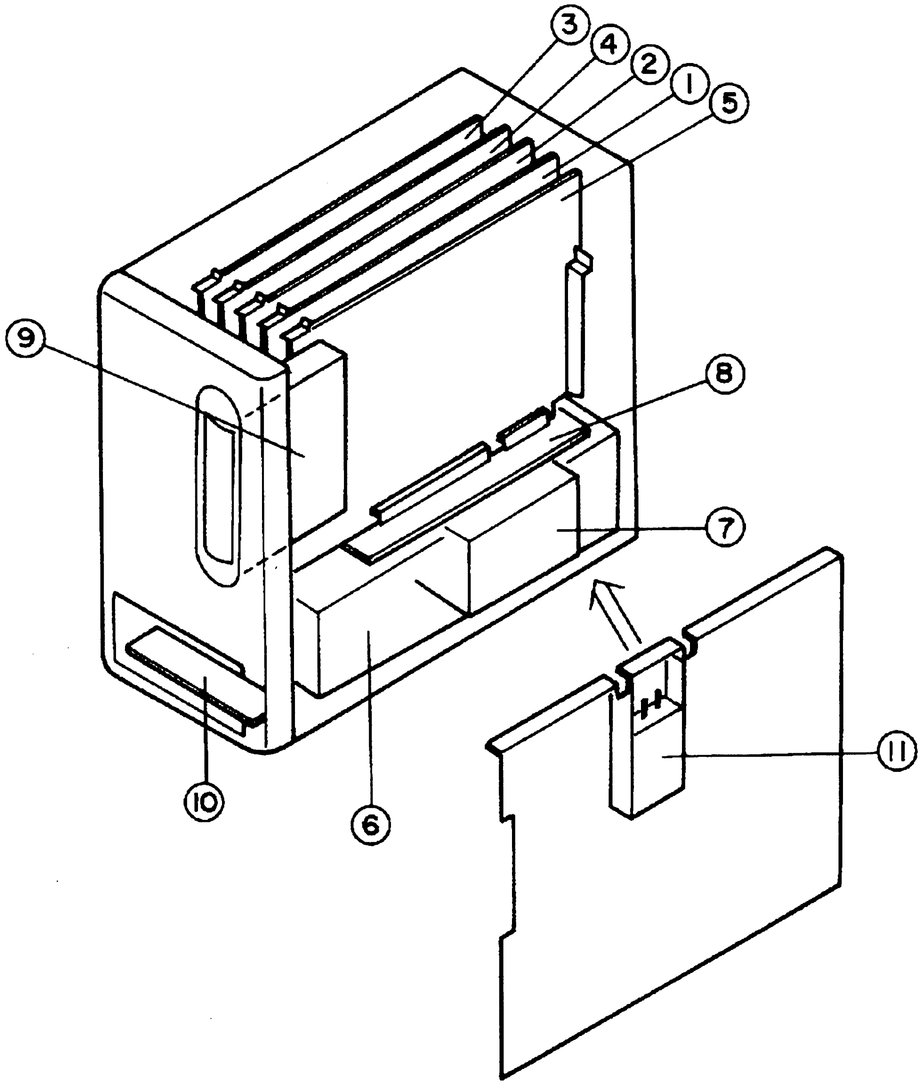
EK-800P

1-4-6 Extension Board

UP-0278 (for UP-0563/0670/0795/0797, UR-3027 in main unit, MU-881R)

1-5 Location

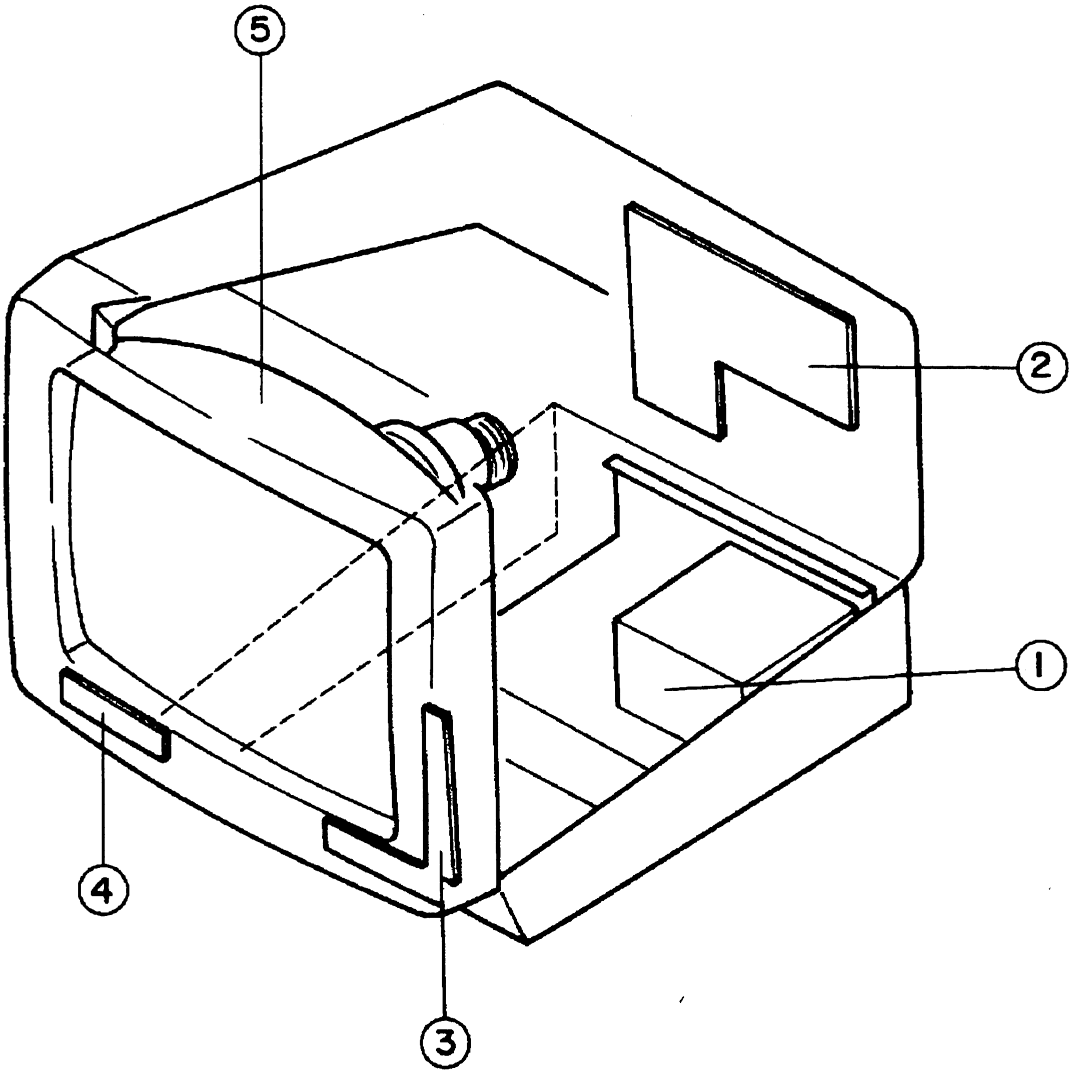
1-5-1 Main Unit, MU-881R



No.	Description	Model
①	CRTC BD (Red ejector)	UP-0795
②	CPU BD (Yellow ejector)	UR-3027
③	DPU BD (Green ejector)	UP-0670
④	COM3 BD (Black ejector)	QI-816P (UP-0563)
⑤	I/O BD (White ejector)	UP-0797
⑥	REGULATOR UNIT	UP-0813

No.	Description	Model
⑦	P.TRANSFORMER UNIT	SC-018R
⑧	MOTHER BD	UP-0798
⑨	MEMORY CARD BD	UP-0799
⑩	FRONT CONNECTOR BD	UP-0807
⑪	RF RECEIVER UNIT (Optional)	ZR-800P

1-5-2 Display Unit, VD-881R



No.	Description	Model
①	POWER SUPPLY UNIT	SC-019R
②	OPERATION CONT. BD	UP-0801
③	VR BD	UP-0802
④	LED BD	UP-0806
⑤	CRT UNIT	

1-6 System Block

The bedside monitor main unit consists mainly of the following boards and units.

- **CPU Board, UR-3027**

The master micro processing unit 68000 is responsible for the whole operation of the bedside monitor. The CPU board not only controls communication with the external units, such as, SOUND (SpO_2 tone) and RS-232C, but also, controls the BSM DPU board and the COM 3 board through their global memory. The CPU board controls the Recorder Unit through the dual-port RAM on the COM 3 board.

- **COM 3 Board, UP-0563**

The slave micro processing unit 8085 on this board controls the communication with the Central Monitor.

- **DPU Board, UP-0670**

The slave micro processing unit 68000 controls the conversion of vital-sign information received from the Input Box, Receiver Unit, and Signal Exchanger, to digital format data for the master micro processing unit. It also converts the digital waveform data to analog waveform data in real time processing.

- **I/O Board, UP-0797**

The single chip CPU on the I/O board controls the generation of the SpO_2 tone, and the Power Supply Unit. The I/O boards also controls the communication with the Display Unit and the Keypad. The Memory Card Interface unit in the I/O board allows communication between the bedside monitor and the memory card. The I/O board provides the communication port for the Signal Exchanger and Central Monitor.

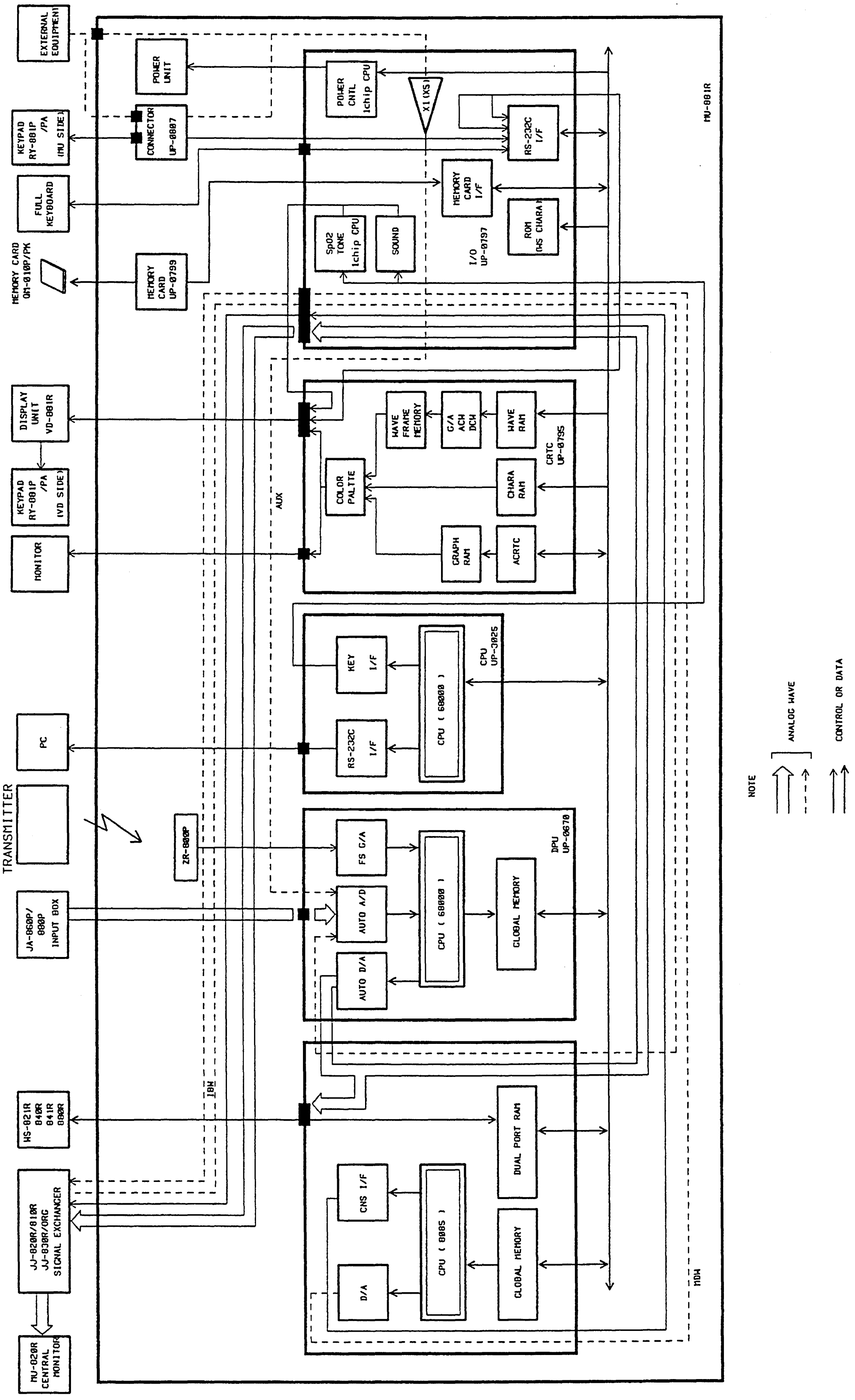
- **CRTC Board, UP-0795**

The CRTC board converts the waveform data, graphic data and character data into video image signals for the Display Unit.

- **Power Transformer Unit, SC-018R**

This unit supplies the power for the individual boards and the fan in the Main Unit, Receiver Unit, Input Box, and Keypad.

System Block Diagram


EXTERNAL EQUIPMENT
POWER UNIT
CONNECTOR UP-0807
KEYPAD RY-001P /PA (MU SIDE)
FULL KEYBOARD
MEMORY CARD QM-010P/PK
MEMORY CARD UP-0799
POWER CNTL 1chip CPU
X1(XS)
RS-232C I/F
MEMORY CARD I/F
ROM (WS CHARA)
Sp02 TONE 1chip CPU
SOUND
I/O UP-0797
MU-001R
DISPLAY UNIT VD-001R
KEYPAD RY-001P /PA (VD SIDE)
MONITOR
WAVE FRAME MEMORY
G/A ACH DCH
WAVE RAM
CRTC UP-0795
COLOR PALITE
CHARA RAM
GRAPH RAM
ACRTC
AUX
KEY I/F
CPU (68000)
CPU UP-3025
PC
RS-232C I/F
TRANSMITTER
ZR-000P
FS G/A
AUTO A/D
AUTO D/A
CPU (68000)
GLOBAL MEMORY
DPU UP-0670
JA-060P/ 080P INPUT BOX
WS-021R 040R 041R 080R
IBW
DUAL PORT RAM
CNS I/F
CPU (8085)
D/A
GLOBAL MEMORY
MDW
JJ-020R/010R JJ-030R/ORG SIGNAL EXCHANGER
MU-020R CENTRAL MONITOR
NOTE
ANALOG WAVE
CONTROL OR DATA

1-7 Signal Flow

1-7-1 General

The bedside monitor is divided into three major categories, of which they are further sub–divided as follow :

1) Analog Signal Flow

- Input Waveform

Analog signals (ECG, respiration, blood pressure, etc) from the Input Box are converted to digital signals. These digital signals are stored in the DPU board.

- Real-time waveform

The digital waveform signal is converted to analog waveform signal in real-time on the DPU board. The waveform analog signal is then sent to the Central Monitor.

- Delayed ECG Waveform

The ECG waveform for the Central Monitor for remote recording is not done on real-time. There is a delay for the COM 3 board to process the digital ECG signals for the Central Monitor.

- Interbed Waveform

The interbed waveform is the selected ECG waveform of the selected bed. The interbed waveform is then processed in the DPU board.

- Auxiliary Unit

The analog signal from auxiliary unit can be connected to the Main Unit with some changes to the configuration of the Setup.

2) Telemetry Signal Flow

The telemetry serial signal received through the Receiver Unit (optional) is converted to parallel signal by the frame sync gate array on the DPU board.

3) Display Data Signal Flow

- Waveform Data

The CPU board selects the waveform data for display from the processed waveform data received from the DPU board. The selected waveform data is loaded to the WAVE RAM on the CRTC board. The selected waveform data read out by the WAVE RAM is gated by the gate array ACW,DCW to the WAVE FRAME MEMORY for conversion to dot image signals. These dot image signals are color palette coded to form R, G, B signals.

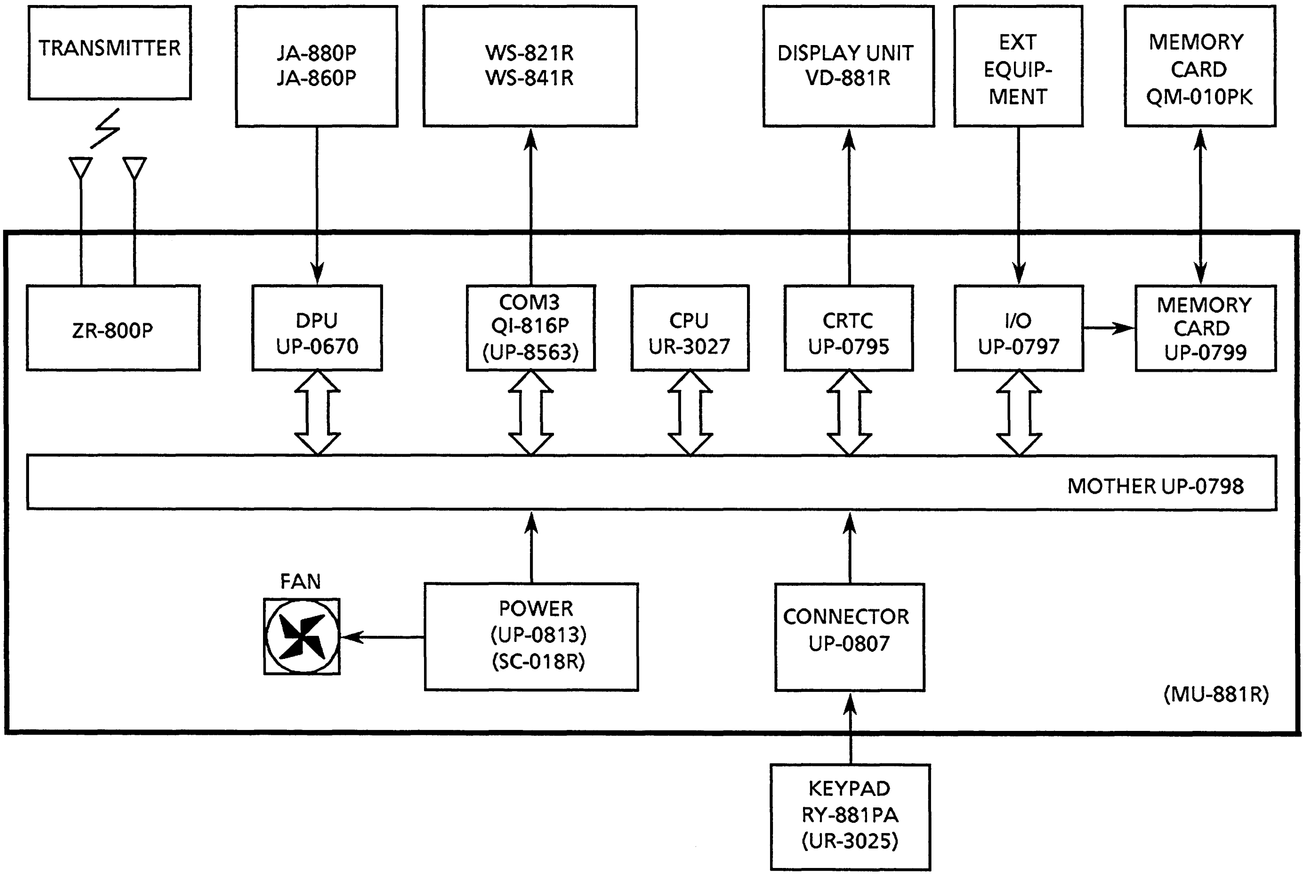
- Graphic Data

The graphic data is loaded to the Graphic RAM through the ACRTC on the CRTC board. The graphic data is read out from the GRAPHIC RAM as dot image signals which are then color palette coded to form R, G, B signals.

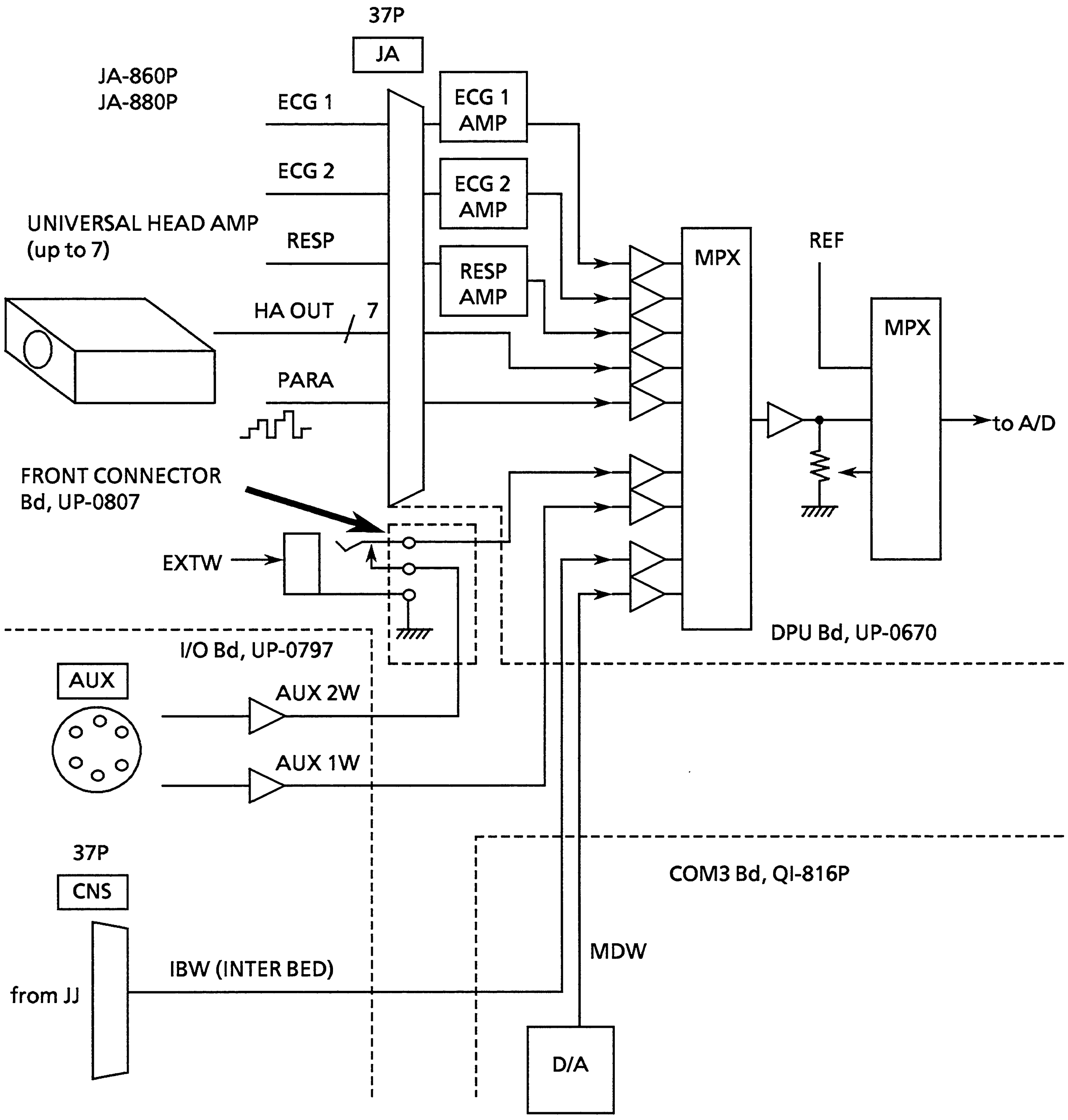
- Character Data

The character is loaded to the CHARACTER RAM on the CRTC board. The character data is read out from the CHARACTER RAM as dot image signals which are then color palette code to form R, G, B signals

System Signal Flow

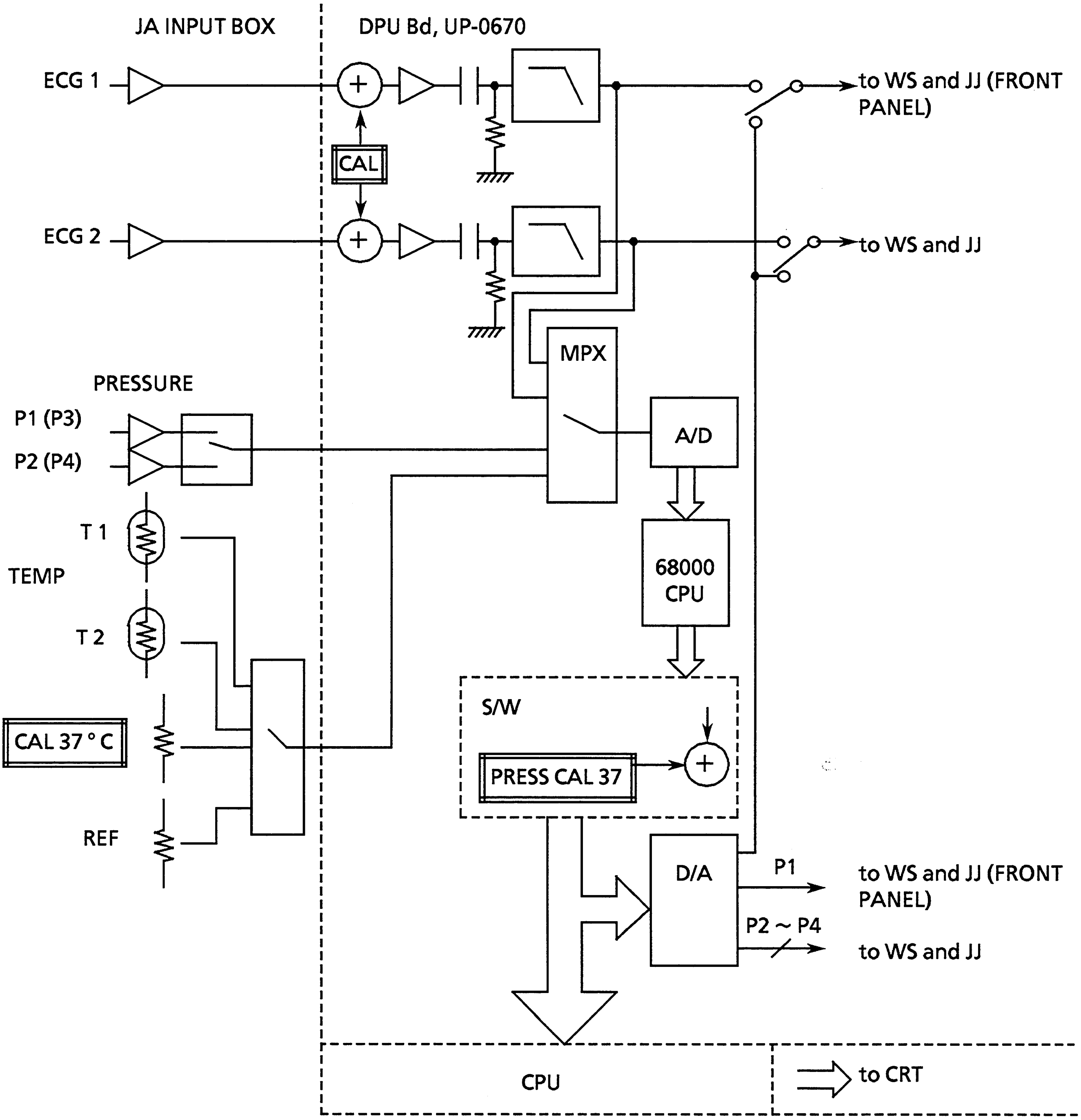

TRANSMITTER
JA-880P
JA-860P
WS-821R
WS-841R
DISPLAY UNIT
VD-881R
EXT
EQUIP-
MENT
MEMORY
CARD
QM-010PK
ZR-800P
DPU
UP-0670
COM3
QI-816P
(UP-8563)
CPU
UR-3027
CRTC
UP-0795
I/O
UP-0797
MEMORY
CARD
UP-0799
MOTHER UP-0798
FAN
POWER
(UP-0813)
(SC-018R)
CONNECTOR
UP-0807
(MU-881R)
KEYPAD
RY-881PA
(UR-3025)

1-7-2 Input Signal Flow


37P
JA
JA-860P
JA-880P
ECG 1
ECG 2
RESP
HA OUT
7
PARA
UNIVERSAL HEAD AMP
(up to 7)
ECG 1 AMP
ECG 2 AMP
RESP AMP
MPX
REF
MPX
to A/D
FRONT CONNECTOR Bd, UP-0807
EXTW
DPU Bd, UP-0670
I/O Bd, UP-0797
AUX
AUX 2W
AUX 1W
37P
CNS
COM3 Bd, QI-816P
MDW
from JJ
IBW (INTER BED)
D/A

1-7-3 Calibration Signal Flow

[Hardwire system]


JA INPUT BOX
DPU Bd, UP-0670
ECG 1
ECG 2
CAL
to WS and JJ (FRONT PANEL)
to WS and JJ
MPX
PRESSURE
P1 (P3)
P2 (P4)
A/D
68000 CPU
T 1
TEMP
T 2
CAL 37 ° C
REF
S/W
PRESS CAL 37
D/A
P1
P2 ~ P4
to WS and JJ (FRONT PANEL)
to WS and JJ
CPU
to CRT

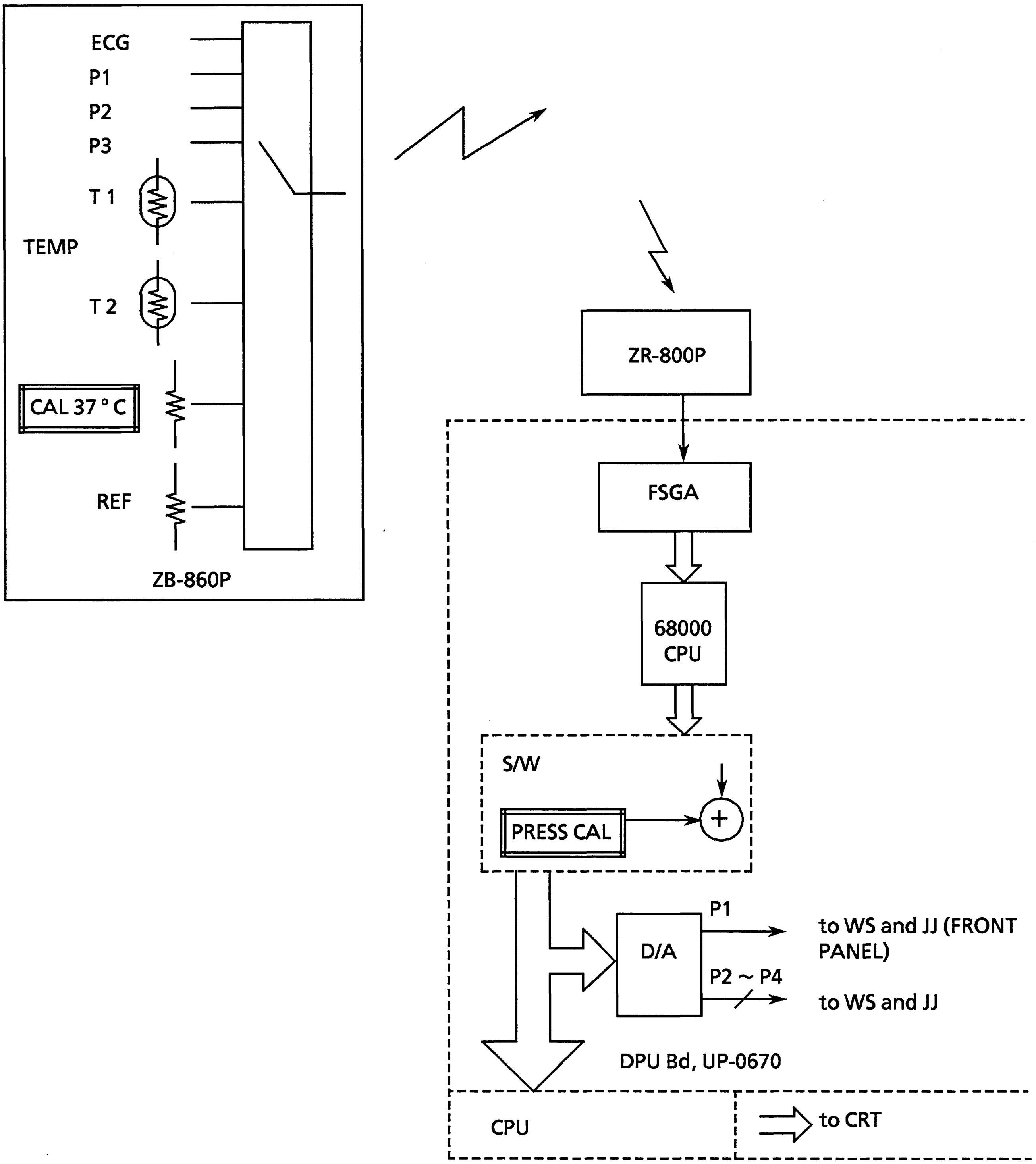
NOTE

1) ECG CAL CHECK : Effective from ECG time constant circuit on DPU board.

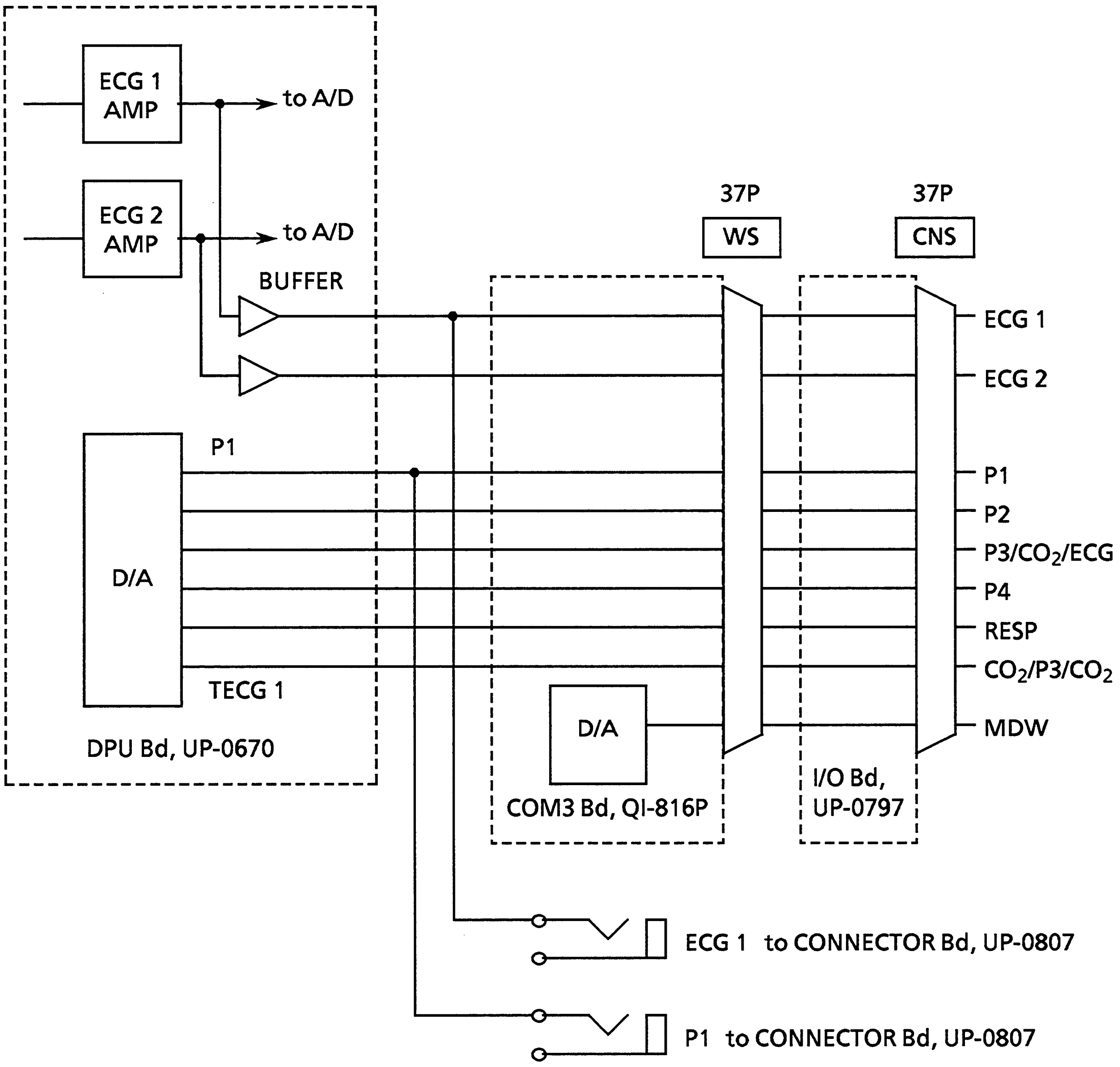
2) PRESSURE CAL CHECK : Effective from D/A convertor on DPU board.

3) TEMPERATURE CAL CHECK : Effective from AW-800PA.

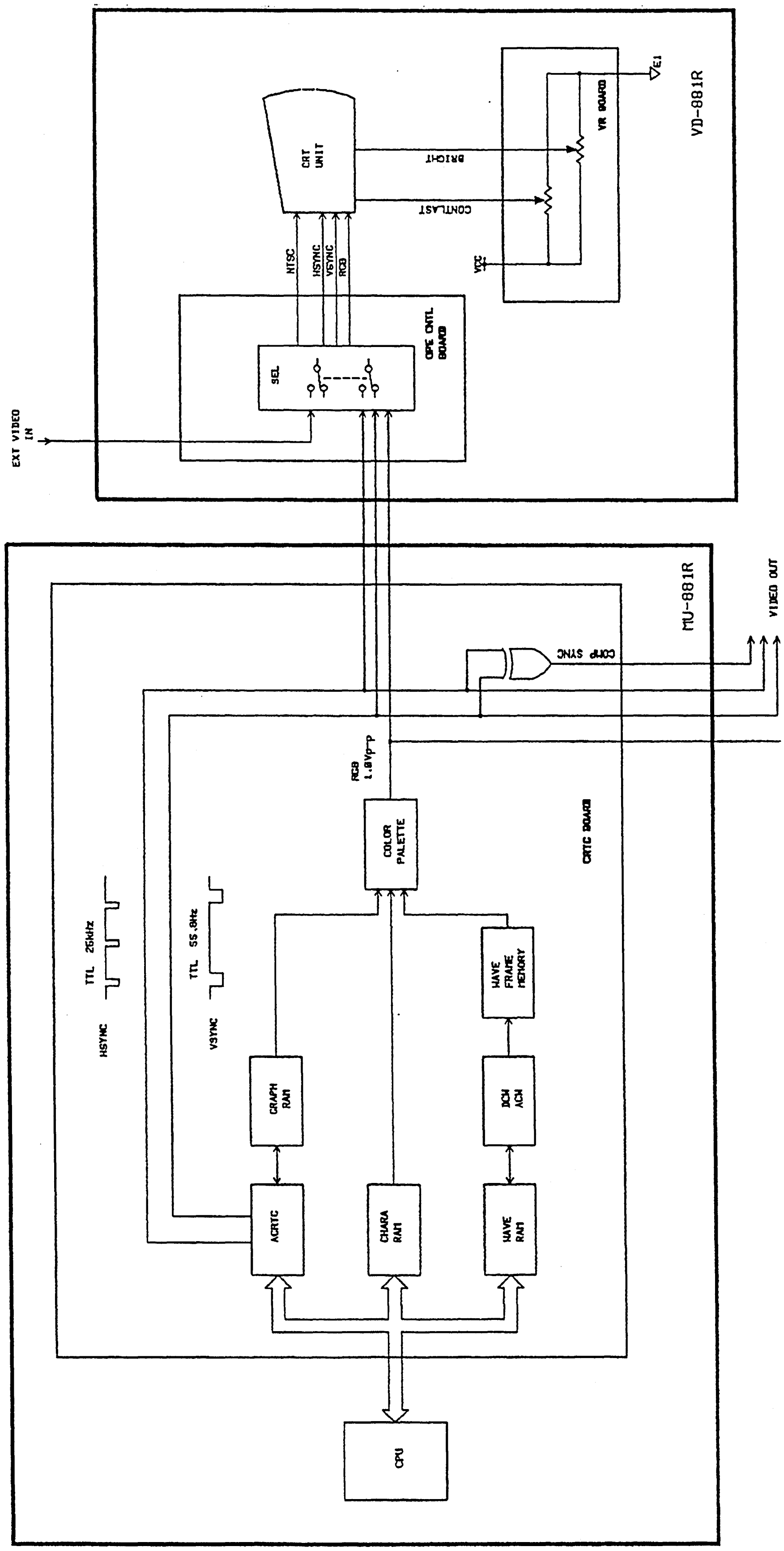
[Telemetry system]


ECG
P1
P2
P3
T 1
TEMP
T 2
CAL 37 ° C
REF
ZB-860P
ZR-800P
FSGA
68000
CPU
S/W
PRESS CAL
+
D/A
P1
to WS and JJ (FRONT PANEL)
P2 ~ P4
to WS and JJ
DPU Bd, UP-0670
CPU
to CRT

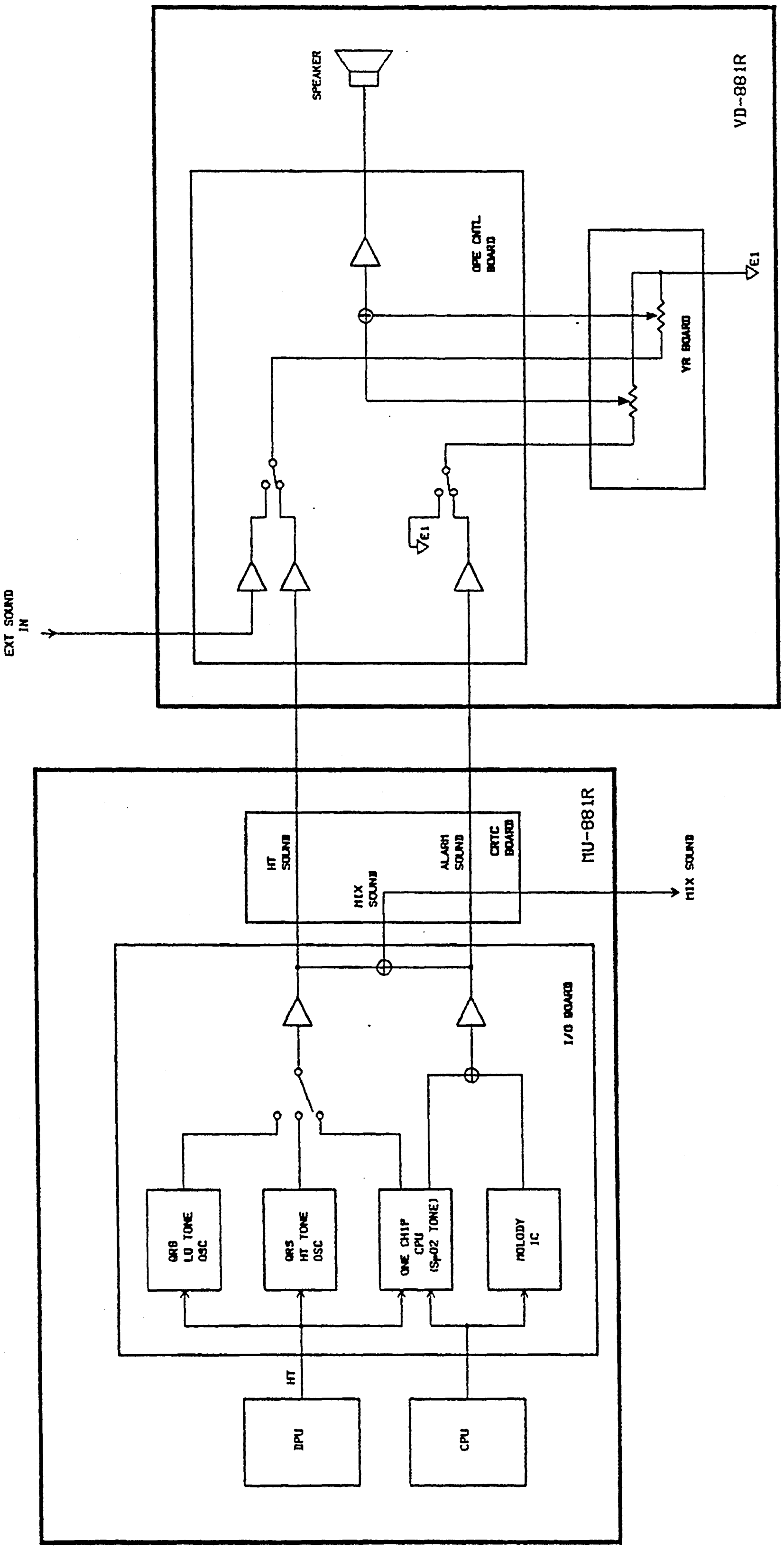
1-7-4 Output Signal Flow


ECG 1 AMP
to A/D
ECG 2 AMP
to A/D
BUFFER
P1
D/A
TECG 1
DPU Bd, UP-0670
37P
WS
37P
CNS
D/A
COM3 Bd, QI-816P
I/O Bd, UP-0797
ECG 1
ECG 2
P1
P2
P3/CO2/ECG
P4
RESP
CO2/P3/CO2
MDW
ECG 1 to CONNECTOR Bd, UP-0807
P1 to CONNECTOR Bd, UP-0807

1-7-5 Video Signal Flow

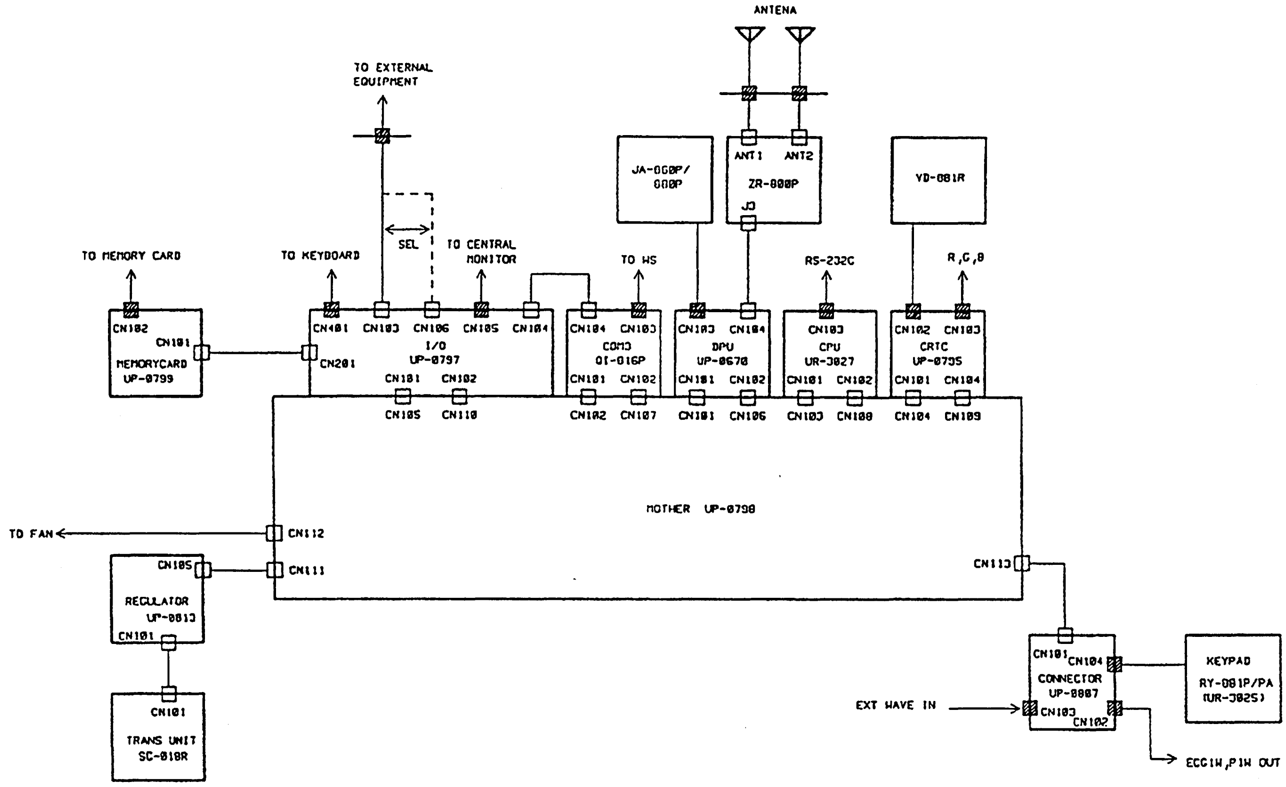

VD-881R
CRT UNIT
BRIGHT
CONTLAST
VR BOARD
E1
VCC
NTSC
HSYNC
VSYNC
RGB
OPE CNTL BOARD
SEL
EXT VIDEO IN
MU-881R
VIDEO OUT
COMP SYNC
RGB 1.0Vp-p
CRTC BOARD
COLOR PALETTE
HSYNC
TTL 25kHz
VSYNC
TTL 55.8Hz
WAVE FRAME MEMORY
DCM ACM
GRAPH RAM
ACRTC
CHARA RAM
WAVE RAM
CPU

1-7-6 Sound Signal Flow

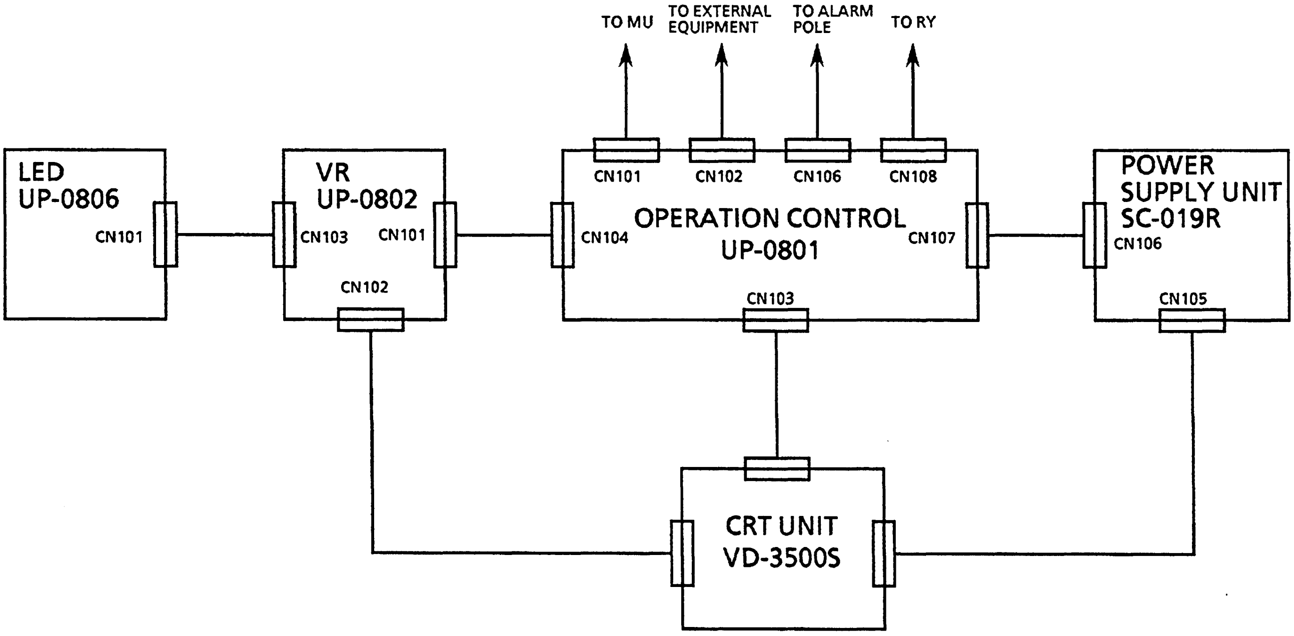

SPEAKER
VD-881R
OPE CNTL BOARD
VR BOARD
E1
E1
EXT SOUND IN
MU-881R
HT SOUND
MIX SOUND
ALARM SOUND
CRTC BOARD
MIX SOUND
I/O BOARD
QR8 LO TONE OSC
QR5 HT TONE OSC
ONE CHIP CPU (S-02 TONE)
MOLODY IC
HT
DPU
CPU

1-8 Connection Diagram

1-8-1 Main Unit, MU-881R

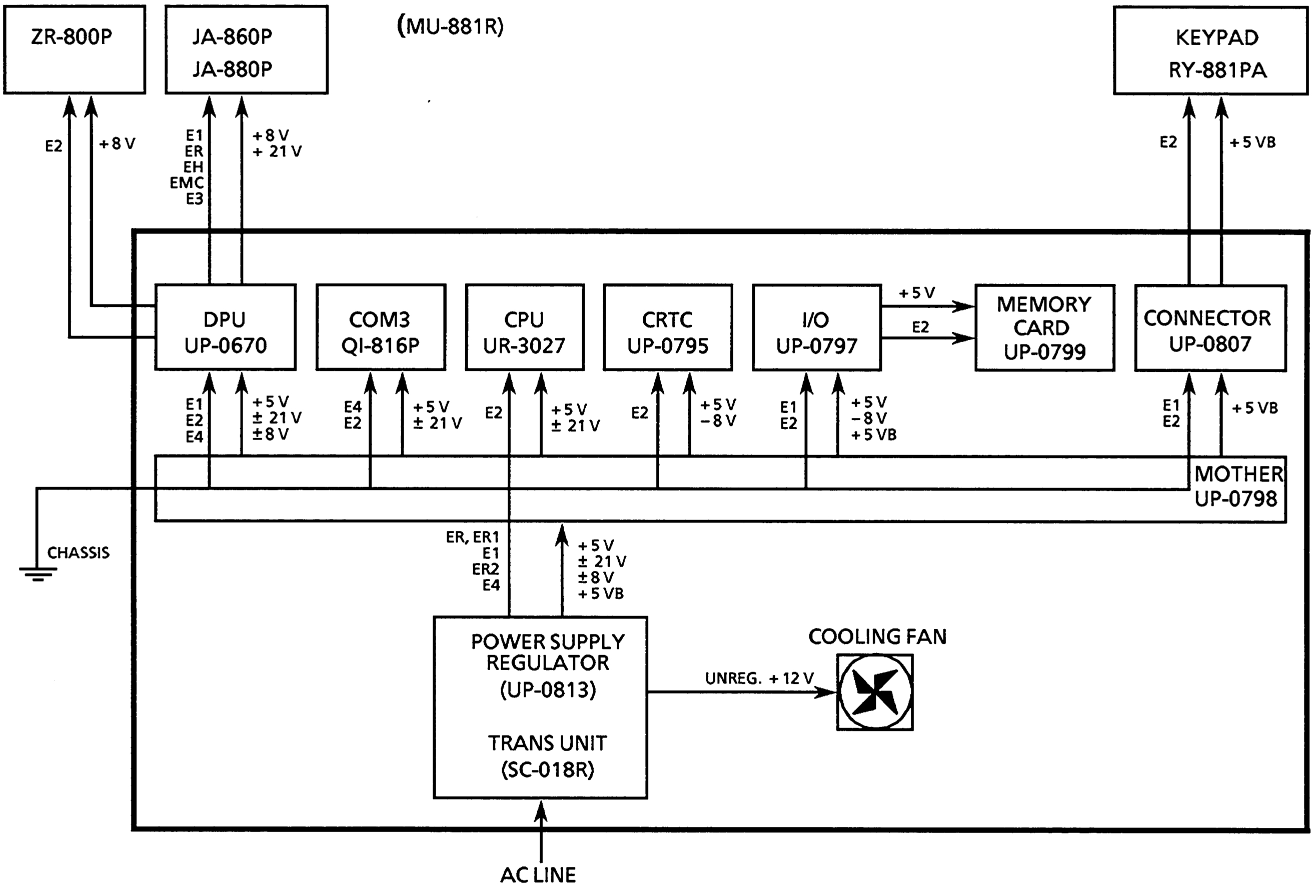

ANTENA
TO EXTERNAL EQUIPMENT
ANT1
ANT2
JA-060P/
080P
ZR-800P
J3
VD-081R
SEL
TO MEMORY CARD
TO KEYBOARD
TO CENTRAL MONITOR
TO WS
RS-232C
R,G,B
CN102
CN101
MEMORYCARD
UP-0799
CN401
CN103
CN106
CN105
CN104
I/O
UP-0797
CN201
CN101
CN102
CN104
CN103
COM3
OI-016P
CN101
CN102
CN103
CN104
DPU
UP-0670
CN101
CN102
CN103
CPU
UR-3027
CN101
CN102
CN102
CN103
CRTC
UP-0735
CN101
CN104
CN105
CN110
CN102
CN107
CN101
CN106
CN103
CN108
CN104
CN109
MOTHER UP-0798
TO FAN
CN112
CN111
CN105
REGULATOR
UP-0813
CN101
CN101
TRANS UNIT
SC-010R
CN113
CN101
CN104
CONNECTOR
UP-0807
CN103
CN102
EXT WAVE IN
KEYPAD
RY-081P/PA
(UR-3025)
ECGIN,PIN OUT

1-8-2 Display Unit, VD-881R

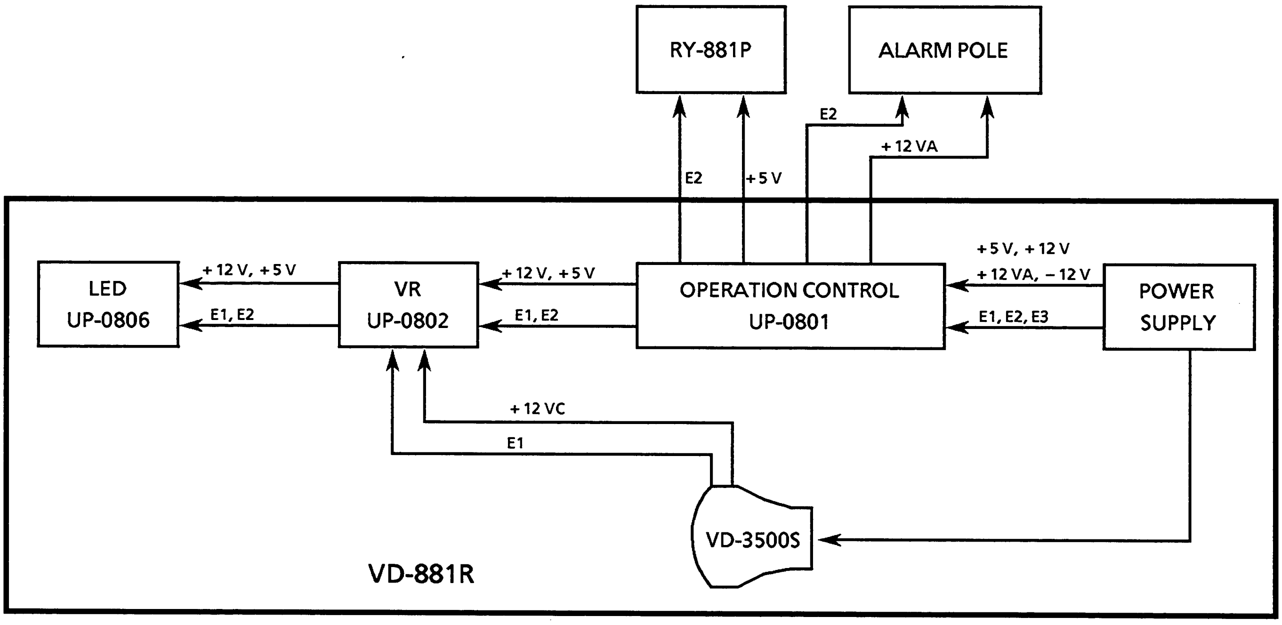

TO MU
TO EXTERNAL EQUIPMENT
TO ALARM POLE
TO RY
LED
UP-0806
CN101
VR
UP-0802
CN103
CN101
CN102
CN101
CN102
CN106
CN108
OPERATION CONTROL
UP-0801
CN104
CN107
CN103
POWER SUPPLY UNIT
SC-019R
CN106
CN105
CRT UNIT
VD-3500S

1-9 Power System Diagram

1-9-1 Main Unit, MU-881R


ZR-800P
JA-860P
JA-880P
(MU-881R)
KEYPAD
RY-881PA
E2
+8 V
E1
ER
EH
EMC
E3
+8 V
+ 21 V
E2
+5 VB
DPU
UP-0670
COM3
QI-816P
CPU
UR-3027
CRTC
UP-0795
I/O
UP-0797
+5 V
E2
MEMORY
CARD
UP-0799
CONNECTOR
UP-0807
E1
E2
E4
+5 V
± 21 V
±8 V
E4
E2
+5 V
± 21 V
E2
+5 V
± 21 V
E2
+5 V
−8 V
E1
E2
+5 V
−8 V
+5 VB
E1
E2
+5 VB
MOTHER
UP-0798
CHASSIS
ER, ER1
E1
ER2
E4
+5 V
± 21 V
±8 V
+5 VB
POWER SUPPLY
REGULATOR
(UP-0813)
TRANS UNIT
(SC-018R)
COOLING FAN
UNREG. + 12 V
AC LINE

1-9-2 Display Unit, VD-881R


RY-881P
ALARM POLE
E2
+ 12 VA
E2
+5 V
LED
UP-0806
+ 12 V, +5 V
E1, E2
VR
UP-0802
+ 12 V, +5 V
E1, E2
OPERATION CONTROL
UP-0801
+5 V, + 12 V
+ 12 VA, − 12 V
E1, E2, E3
POWER
SUPPLY
+ 12 VC
E1
VD-3500S
VD-881R

1-10 Related Instruments Connection

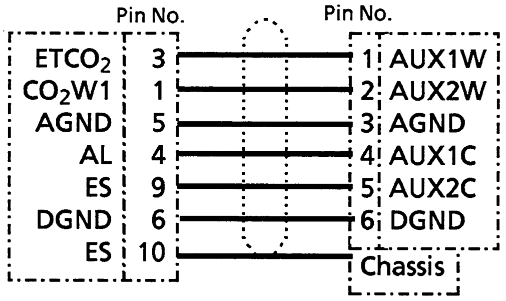
Firstly, select one of the following instruments on the SETUP display.

Related Instruments	Input signal			
	AUX1W	AUX2W	AUX1C (Active-low)	AUX2C (Active-low)
CO_2 Monitor (OIR-7101)	$ETCO_2$ (20 mmHg/V)	CO_2 Waveform (20 mmHg/V)	$ETCO_2$ Alarm Signal	CO_2 Measure Signal
External Alarm Signal	——	——	——	Alarm (Error) Indication Signal
External Analog Signal	——	External Waveform	——	——

——: Don't care

[OIR-7101]
Connector
: S-1628G
: P-1628A-CA(20)
: P-1628A-STA(01)

Connection cable: YS-005P8


Pin No.
Pin No.
$ETCO_2$ 3
CO_2W1 1
AGND 5
AL 4
ES 9
DGND 6
ES 10
1 AUX1W
2 AUX2W
3 AGND
4 AUX1C
5 AUX2C
6 DGND
Chassis

[BSM-8800]
Connector
: RM12BPG-6P
Parts No. 078541

Section 2 SIGNAL LIST

2-1 Main Unit, MU-881R 2.1

  2-1-1 COM 3 Board, UP-0563 .... 2.1

  2-1-2 DPU Board, UP-0670 .... 2.3

  2-1-3 CRTC Board, UP-0795 .... 2.7

  2-1-4 I/O Board, UP-0797 .... 2.13

  2-1-5 UR-3027, CPU Board 2.16

2-2 Keypad, RY-881PA 2.19

  2-2-1 CONSOLE Board, UR-3025 .... 2.19

2-3 Display Unit, VD-881R 2.20

  2-3-1 OPERATION CONTROL Board, UP-0801 .... 2.20

  2-3-2 OPERATION (VR) Board, UP-0802 .... 2.21

2-1 Main Unit, MU-881R

2-1-1 COM 3 Board, UP-0563

Prefix "X" means negative logic.
For example: A/XM
High level (5V): Address recognition signal (active-high)
Low level (0V) : Message recognition signal (active-low)
If a signal is not found, search the symbol from "X + signal name" lists.
If a signal "X + symbol" is not found, search the symbol from "signal name-X".

Symbol	Function	Part
ALE 85	8085 address latch enable signal from 8085	4/10
A0L-A10L	Recorder CPU address bus	9/10
AX0-12	Global memory address bus	3/10
CLK 3M	8085 clock (3MHz)	4/10
CLK 96	Transmitting/receiving clock	7/10
CS	COM3 Board select signal	1/10
DOL-D7L	Dual port RAM data bus	9/10
DX0-7	Global memory data bus	3/10
DX85 0-15	8085 data bus	4/10
DX85 0-7	8085 data bus	4/10
IO0-7	Recorder CPU data bus	9/10
MDW	Delayed ECG waveform	6/10
MSK 7.5	RST 7.5 interrupt request signal mask signal	5/10
RD	CNS data reception signal	5/10
RD RET	CNS data reception return signal	5/10
RES 85	8085 external unit reset signal from 8085	4/10
RST 6.5	CNS data reception interrupt request signal	5/10
RST 7.5	Watch dog timer periodic interrupt request signal	7/10
RSTIN	8085 reset signal for CPU (CPU Board) from 8085	7/10
SD	Data transmit signal for CNS	5/10
SD RET	Data transmit return signal for CNS	5/10
SEL85	Global memory bus select signal	2/10
WDT	Software watch dog timer control signal	4/10
WDTINT	Watch dog timer interrupt request signal	7/10

2. SIGNAL LIST

Symbol	Function	Part
X6.5CLR	RST6.5CLR output flip-flop clear	4/10
X8251S	8251 select signal	4/10
XAL	Alarm signal	5/10
XBUSY2	BSM busy line signal for CNS	5/10
XBUSY2 RET	BSM busy line return signal for CNS	5/10
XBUSYL	Dual port RAM wait request signal for recorder CPU	9/10
XBUSYR	Dual port RAM wait request signal for CPU (CPU Board)	9/10
XCOMW	Recorder CPU memory write control signal	9/10
XCS0	WS reset port select signal	1/10
XCS1	8085 dual port RAM select signal	1/10
XCS3	CG ROM select signal	1/10
XCS4, 5	Printer buffer RAM select signal	1/10
XCSRST85	8085 reset port select signal from CPU (CPU Board)	2/10
XD/ASEL	DA port select signal	4/10
XDOS	Output port (IC146) select signal	4/10
XGLS 68	Global memory access request signal from CPU (CPU Board)	2/10
XGLS 68A	Global memory select signal from CPU (CPU Board)	2/10
XGLS85	Global memory select signal from 8085	4/10
XINT11	Interrupt request signal for CPU (CPU Board) from CPU (WS)	9/10
XINT16	Interrupt request signal for CPU (CPU Board) from 8085	5/10
XINTL	CPU (CPU Board) interrupt request signal for recorder signal	9/10
XIORD	8085 read control signal for output port	4/10
XIORST85	CPU (CPU Board) 8085 reset signal	2/10
XIOWR	8085 write control signal for output port	4/10
XLEDS	LED port select signal	4/10
XMRD	8085 read control signal for global memory	4/10
XMWR	8085 write control signal for global memory	4/10
XRAMC	Recorder CPU memory read	9/10
XRDL	Lower 8 bit data read	2/10
XRDU	Upper 8 bit data read	2/10
XRESET	CPU (CPU Board) reset request signal	9/10
XSWS	Dip switch port select signal	4/10
XWRL	Lower 8 bit data write	2/10
XWRU	Upper 8 bit data write	2/10

2-1-2 DPU Board, UP-0670

Symbol	Function	Part
*MA6	A/D RAM memory address	8/19
16M	16MHz clock	1/19
A1-23	Address bus lines 1-23	1/19
ADINT	AD interrupt (every 2msec)	6/19
ADSFT	A/D convertor shift voltage	15/19
ANT11	Diversity switching	10/19
AUX1C, AUX2C	External unit's waveform input control	10/19
AUX1W, AUX2W	Auxialiary input analog waveform signal	12/19
BERR	Bus error	1/19
CA0	A/D convertor data width control	7/19
CE	A/D convertor chip enable	8/19
CH1W/P1W	Channel-3 waveform/blood pressure 1 waveform	16/19
CH4W/P2W	Channel-4 waveform/blood pressure 2 waveform	16/19
CH5W/P3W	Channel-5 waveform/blood pressure 3 waveform	16/19
CH6W/P4W	Channel-6 waveform/blood pressure 4 waveform	16/19
CH7W/RW	Channel-7 waveform/respiration waveform	16/19
CH8W/EXTAUX	Channel-8 waveform or external input unit	16/19
CH9W	Channel-9 waveform	16/19
CLK	RF unit clock	10/19
CLK16M	16MHz system clock	3/19
CLK16MC	16MHz clock	3/19
CLK500K	500kHz	2/19
CLKSAMPL	8msec clock	3/19
D/A	D/A cconverted waveform signal	15/19
D0-15	Data bus lines 0-15	1/19
DATA	RF unit setting data	11/19
DTACK1	Data acknowledge 1	3/19
DTACK2	Data acknowledge 2	4/19
ECG, ECG2	2ch ECG regenerated ECG signal	11/19
ECG1AD, ECG2AD	Processed ECG amplifier output signal	13/19
EN1	Peak hold enable signal	8/19
FC0-2	Function code	1/19
FSSTS	Frame shift gate array status signal	8/19
G1-2	Gain select signal	14/19

2. SIGNAL LIST

Symbol	Function	Part
GMSLC	Global memory select signal	3/19
HA2-8	Individual head amplifier output signal	11/19
HAECG1	ECG1 signal	17/19
HAECG2	ECG2 signal (fixed lead II ECG)	17/19
HARESP	Respiration waveform	18/19
HICUT	ECG high cut filter select signal	11/19
HUM	ECG hum filter	11/19
IBW	Interbed waveform signal	12/19
INST	ECG instantaneous short circuit signal	11/19
INT1	Interrupt request signal from CPU to DPU	3/19
JACLK	JA communication clock	7/19
JACNTL	JA control signal	9/19
JADLWL	JA lower byte write	2/19
JAFCLK	JA floating clock	7/19
JARCLK	Respiration detection carrier generator clock	7/19
JASTS	JA status signal	9/19
L1	Auto D/A lower byte data latch signal	8/19
L2	Auto D/A upper byte data latch signal	8/19
LE	RF unit data latch enable signal	10/19
LMA2-4	Multiplexer switching control signal	8/19
LMA6	Analog input multiplexer inhibit control signal	8/19
MA0	Auto A/D or D/A memory address 0	7/19
MA1	A/D RAM memory address control (or select) signal	8/19
MDW	Delayed ECG waveform	12/19
MPX	Multiplexed waveform	11/19
PARA	Head amplifier recognition or measure status signal for input box	12/19
QB	256 kHz clock	7/19
R/XC	A/D convertor read/convert control (or select) signal	8/19
R/XW	Read/write control (or select) signal	1/19
R/XWB	System read/write control (or select) signal	3/19
R/XWC	System read/write control (or select) signal	3/19
RCT8MS	125Hz (8msec) clock	3/19
REF10V	+10V reference voltage	14/19
RESPAD	Respiration waveform signal for A/D convertor	11/19
RINST	Respiration wave instantaneous short circuit signal	11/19

Symbol	Function	Part
RSSI	Receiver field strength signal	15/19
RTC	ECG high cut filter control (or select) signal	11/19
S0	Hardwire or telemetry switching control signal	10/19
TC3.2	ECG time constant control signal (H:3.2sec;L:0.5sec)	11/19
TECG1W, TECG2W	Telemetry analog ECG waveform	15/19
TEST	1mV calibration control signal	11/19
TST	AD RAM test	8/19
W/XR	Write/read control (or select) signal	1/19
XADDR1-13	System address bus A1-13	5/19
XADDR17-23	System address bus A17-23	3/19
XADRCS	A/D RAM chip select signal	2/19
XADWR	AD RAM memory write	8/19
XAS	Address strobe signal	1/19
XASB	System address strobe signal	3/19
XCLK0	8MHz clock	4/19
XCNT	Counter status read	2/19
XCPUINT	Interrupt request for CPU board	2/19
XCS	A/D RAM memory write control signal	8/19
XDIPSW	Dip switch read	2/19
XDTACK	Data acknowledgement signal	1/19
XDTACK	System data acknowledgement signal	3/19
XE0	A/D RAM memory read	8/19
XFSCLR	Frame sync clear	2/19
XGARD	FS Gate array read	2/19
XGMCS	Global memory chip select signal	4/19
XGMCSC	System global memory chip select signal	4/19
XGMRL	Global memory lower byte read	4/19
XGMRU	Global memory upper byte read	4/19
XGMSL	Global memory select	2/19
XGMWL	Global memory lower byte write	4/19
XGMWU	Global memory upper byte write	4/19
XHALT	Halt	1/19
XHIFCM	ECG write control signal	2/19
XHO	ECG measure signal	10/19
XHT	ECG synchronizing signal	10/19
XIA	Interrupt request signal acknowledge	2/19

2. SIGNAL LIST

Symbol	Function	Part
XINT13	Interrupt request signal from DPU to CPU	3/19
XIORST	I/O port reset signal (SYSTEM)	3/19
XIORSTC	I/O reset signal	2/19
XIPL0-2	Interrupt request priority level	1/19
XJADLR	JA lower 16 bits status read	2/19
XJADLWU	JA lower upper byte write	2/19
XJADUR	JA upper 16 bits status read	2/19
XJADUWL	JA upper byte write	2/19
XJADUWU	JA upper upper byte write	2/19
XLDS	Lower byte data strobe signal	1/19
XLDSB	System lower byte data strobe signal	3/19
XLDSC	System lower byte data strobe signal	3/19
XLED	LED write output port	2/19
XLEN2	D/A multiplexer inhibit control signal	8/19
XRAMCS	RAM chip select signal	1/19
XRDLS	Lower byte read	1/19
XRESET	Reset signal	1/19
XRESTS	RF status read	2/19
XRFCNTL	RF write	2/19
XRO	JARCLK preset signal	7/19
XROMCS	ROM chip select signal	1/19
XSATA0-15	System data bus D0-15	5/19
XSTR	Pacing pulse strobe signal	8/19
XSYNC2	Frame shift gate array SYNC	8/19
XUDS	Upper byte data strobe signal	1/19
XUDSB	System upper byte data strobe signal	3/19
XUDSC	System upper byte data strobe signal	3/19
XVPA	Valid peripheral address	1/19
XWDLS	Lower byte write	1/19

2-1-3 CRTC Board, UP-0795

Symbol	Function	Part
16MHz	16MHz clock	8/20
16MHzC	16MHz clock	7/20
2MHz	ACW Synchronizing clock	8/20
32MHz	32MHz clock for graphic processing	2/20
32MHzG	32MHz clock	8/20
64MHz	Clock for palette code	18/20
A1D0-3	Latched individual signal A1SD0-3	6/20
A1SD0-3	Waveform serial data A 1,3,5,7 trace EVEN	6/20
A2D0-3	Latched individual signal A2SD0-3	6/20
A2SD0-3	Waveform serial data A 2,4,6,8 trace EVEN	6/20
A3D0-3	Latched individual signal A3SD0-3	6/20
A3SD0-3	Waveform serial data A 1,3,5,7 trace ODD	6/20
A4D0-3	Latched individual signal A4SD0-3	6/20
A4SD0-3	Waveform serial data A 2,4,6,8 trace ODD	6/20
AA00-07	Upper screen frame memory address	8/20
ADDL	Character ROM address latch	16/20
ALSND	Alarm sound signal	19/20
AREA	ACW setting signal (Input port signal)	8/20
ASD0-3	Waveform serial data A EVEN	7/20
ATR B	Character attribute (B) select signal	16/20
ATR BL	Character attribute blink select signal	16/20
ATR G	Character attribute (G) select signal	16/20
ATR I	Character attribute (I) select signal	16/20
ATR R	Character attribute (R) select signal	16/20
ATR RV	Character attribute reverse signal	16/20
ATRL	Character attribute signal latch	16/20
B1D0-3	Latched individual signal B1SD0-3	6/20
B1SD0-3	Waveform serial data B 1,3,5,7 trace EVEN	6/20
B2D0-3	Latched individual signal B2SD0-3	6/20
B2SD0-3	Waveform serial data B 2,4,6,8 trace EVEN	6/20
B3D0-3	Latched individual signal B3SD0-3	6/20
B3SD0-3	Waveform serial data B 1,3,5,7 trace ODD	6/20
B4D0-3	Latched individual signal B4SD0-3	6/20
B4SD0-3	Waveform serial data B 2,4,6,8 trace ODD	6/20

2. SIGNAL LIST

Symbol	Function	Part
BA00-07	Lower screen frame memory address	8/20
BAM00-15	Waveform data (B)	14/20
BBM00-15	Delayed waveform data (B)	15/20
BCONT	CPU bus control	5/20
BSD0-3	Waveform serial data B EVEN	7/20
C1D0-3	Latched individual signal C1SD0-3	6/20
C1SD0-3	Waveform serial data C 1,3,5,7 trace EVEN	6/20
C2D0-3	Latched individual signal C2SD0-3	6/20
C2SD0-3	Waveform serial data C 2,4,6,8 trace EVEN	6/20
C3D0-3	Latched individual signal C3SD0-3	6/20
C3SD0-3	Waveform serial data C 1,3,5,7 trace ODD	6/20
C4D0-3	Latched individual signal C4SD0-3	6/20
C4SD0-3	Waveform serial data C 2,4,6,8 trace ODD	6/20
CHA0-12	Character ROM address	16/20
CHD0-7	Character ROM output data	17/20
CHRA0-3	Character ROM address	17/20
CK2M	Character 2MHz clock	16/20
CK4M	Character 4MHz clock	16/20
CMA0-12	Character RAM address	16/20
CMD0-15	Character RAM output data	16/20
CSD0-3	Waveform serial data C EVEN	7/20
CUD CD	Character delayed timing signal	16/20
DASD0-3	Waveform serial data A ODD	7/20
DBSD0-3	Waveform serial data B ODD	7/20
DCSD0-3	Waveform serial data C ODD	7/20
DDISP1	Displayed timing 1 (delayed) signal	8/20
DISP B	Character display timing (delayed 2 clock) signal	16/20
DISP F	Character display timing (delayed 4 clock) signal	16/20
DSLD	Waveform data change start signal (delayed)	8/20
ESND	Ground for sound	19/20
EXTRDY	Ready signal	19/20
G.CHVB	Graphic and character composite video (B) signal	17/20
G.CHVG	Graphic and character composite video (G) signal	17/20
G.CHVI	Graphic and character composite video (I) signal	17/20
G.CHVR	Graphic and character composite video (R) signal	17/20
GA0-8	Graphic RAM address	2/20

Symbol	Function	Part
GAM00-15	Waveform data (G)	12/20
GBM00-15	Delayed waveform data (G)	13/20
GSD0-15	Graphic serial data	3/20
GVB	Graphic video (B) signal	3/20
GVG	Graphic video (G) signal	3/20
GVI	Graphic video (I) signal	3/20
GVR	Graphic video (R) signal	3/20
H.C.	Color hardcopying signal	18/20
HSYNC	Horizintal synchronizing signal	2/20
HTSND	QRS synchronized pulse sound signal	19/20
LCK	Gate array space control (ACW-DCW) signal	6/20
LDP1, 2	Shift register load 1,2	8/20
M/XS SEL	Master/slave select signal	19/20
MA16-19	Memory address select signal (GRAPHIC)	2/20
MAA00-07	Upper screen latched frame memory address	8/20
MAD0-15	Memory address/data (GRAPHIC)	2/20
MBA00-07	Lower screen latched frame memory address	8/20
MCYC	Memory cycle	2/20
MIXSND	Alarm sound signal mixed with QRS sycnchronized pulse sound signal	19/20
PLOL3	Palette overwrite input signal	18/20
PLPT7	Palette pixel input signal	18/20
R,G,B	RGB signal	19/20
R/XWC	Read/write control (or select) signal	1/20
RAM00-15	Waveform data (R)	10/20
RBM00-15	Delayed waveform data (R)	11/20
RxD1	Main unit inputted data for Display	19/20
RxD2	Main unit inputted data for keypad	19/20
SAS	Frame memory serial shift signal	8/20
SAS0, 1	Frame memory serial shift 0, 1 signal	8/20
SCLK	Change waveform clock	6/20
TxD1	Main unit outputted data for Display	19/20
TxD2	Main unit outputted data for keypad	19/20
VSYNC	Vertical synchronizing (every one frame) signal	2/20
W SC	Graphic RAM data transmission serial clock	2/20
WA1-16	Waveform RAM address	4/20

Symbol	Function	Part
WBVA	Waveform video (B) data	14/20
WBVB	Delayed waveform video (B) data	15/20
WD0A-15A	Waveform data 1,3,5,7 trace EVEN	4/20
WD0B-15B	Waveform data 2,4,6,8 trace EVEN	4/20
WD0C-15C	Waveform data 1,3,5,7 trace ODD	5/20
WD0D-15D	Waveform data 2,4,6,8 trace ODD	5/20
WD08-15	ACW setting data	8/20
WDISP	Waveform display timing	8/20
WGVA	Waveform video (G) data	12/20
WGVB	Delayed waveform video (G) data	13/20
WRVA	Waveform video (R) data	10/20
WRVB	Delayed waveform video (R) data	11/20
X16MHzC	16MHz clock (reverse shaded)	7/20
X32MHz	32MHz clock	8/20
X8MHz	8MHz clock	2/20
XACRTCIRQ	Interrupt request signal from ACRTC	1/20
XACRTCSL	ACRTC select signal	1/20
XASC	Address strobe signal	1/20
XC LOAD	Character load timing control signal	16/20
XCAS	Graphic RAM column address strobe signal	2/20
XCASA	Upper screen frame memory column address strobe signal	8/20
XCASB	Lower screen frame memory column address strobe signal	8/20
XCHOEH	Upper byte character RAM read	1/20
XCHOEL	Lower byte character RAM read	1/20
XCHRDAK	Character data acknowledge signal	1/20
XCHRSL	Character RAM select signal	1/20
XCHWEH	Upper byte character RAM write	1/20
XCHWEL	Lower byte character RAM write	1/20
XCRDTAK	ACRTC data acknowledge signal	1/20
XCS0, 1	Waveform RAM select 0, 1 (delayed) signal	4/20
XCS2	Gate array space control (ACW-DCW) signal	6/20
XCSJ	Gate array space control (ACW-DCW) signal	6/20
XCSYNC	Composite synchronizing signal	17/20
XCUD D	Delayed display timing 1 (XCUD1) control signal	2/20
XCUD1	Display timing 2 control signal	2/20
XDAT	Gate array space control (ACW-DCW) control signal	6/20

Symbol	Function	Part
XDG0-3	Waveform data buffer enable	4/20
XDG0-3	Waveform data buffer enable	5/20
XDISP1	Display timing 1 signal	2/20
XEXSYNC	Auxiliary unit synchronizing signal	2/20
XGDTAK	Waveform data acknowledge (from gate array) signal	1/20
XHSYNC	Horizontal synchronizing (reverse shaded) signal	2/20
XHSYNCD	Delayed horizontal synchronizing signal	8/20
XHT	QRS synchronized pulse for alarm pole	19/20
XIORD	I/O port read	1/20
XIOWR	I/O port write	1/20
XIRQ	Interrupt request signal from ACW	1/20
XKEYRST1	VD reset signal	19/20
XKEYRST2	Keypad reset signal	19/20
XLDSC	Lower byte data strobe signal	1/20
XMD0	Gate array space control (ACW-DCW) signal	6/20
XOE0, 1	Graphic RAM read	2/20
XOEA	Upper screen frame memory read	8/20
XOEB	Lower screen frame memory read	8/20
XOEH	Waveform RAM upper byte data read	5/20
XOEH	Waveform RAM upper byte data read	4/20
XOEL	Waveform RAM lower byte data read	5/20
XOEL	Waveform RAM lower byte data read	4/20
XPALRD	Read palette code	1/20
XPALWR	Write palette code	1/20
XPS.CTL2	Power state status signal	19/20
XRAS	Graphic RAM row address strobe signal	2/20
XRASA	Upper screen frame memory row address strobe signal	8/20
XRASB	Lower screen frame memory row address strobe signal	8/20
XRST	System reset signal	1/20
XS0G, 1G	Graphic RAM serial enable signal	2/20
XSE0-7	Frame memory serial enable signal	8/20
XSLD	Waveform data change start signal	6/20
XUDSC	Upper byte data strobe signal	1/20
XVSYNC	Vertical synchronizing (reverse shaded) signal	2/20
XWARSL	Waveform RAM select signal	1/20
XWE0, 1	Graphic RAM write	2/20

2. SIGNAL LIST

Symbol	Function	Part
XWE0-3H	Waveform RAM upper byte data write 0-3	4/20
XWE0-3H	Waveform RAM upper byte data write 0-3	5/20
XWE0-3L	Waveform RAM lower byte data write 0-3	4/20
XWE0-3L	Waveform RAM lower byte data write 0-3	5/20
XWEA	Upper screen frame memory write	8/20
XWEB	Lower screen frame memory write	8/20

2-1-4 I/O Board, UP-0797

Symbol	Function	Part
ALSND	Alarm sound signal	3/6
AUX1C, AUX2C	Auxiliary input waveform control signal	1/6
AUX1W, AUX2W	Auxiliary input waveform 1 , 2	1/6
BNK0-6	Memory card bank switching signal	2/6
BVD1,2	Memory card battery voltage detection signal	2/6
CH3W/P1W	Channel-3 waveform/blood pressure 1 waveform	1/6
CH4W/P2W	Channel-4 waveform/blood pressure 2 waveform	1/6
CH5W/P3W	Channel-5 waveform/blood pressure 3 waveform	1/6
CH6W/P4W	Channel-6 waveform/blood pressure 4 waveform	1/6
CH7W/RW	Channel-7 waveform/respiration waveform	1/6
CH8W/EXTAUX	Channel-8 waveform/auxiliary unit waveform	1/6
CHRSL1, 2	Character ROM select signal	4/6
DTACKB1, 2	Data acknowledge for internal timing signal	2/6
ECG1W, ECG2W	ECG waveform 1, 2 signal	1/6
ESND	Ground for sound control board	1/6
HI/LO	Synchronized with QRS pulse high/low tone switching signal	3/6
HTLO	Low tone synchronized QRS pulse	3/6
HTSND	Synchronized QRS pulse sound signal	3/6
IB SEL	Interbed select signal	1/6
IBW	Interbed waveform signal	1/6
KD0-7	Character ROM data signal	6/6
LATCHA	Memory card address latch signal	2/6
M/XS SEL	Display unit master/slave select signal	5/6
MA1-18	Memory card address A1-18 control (or select) signal	2/6
MCLED	Memory card indication LED signal	2/6
MD0-15	Memory card data D0-15	2/6
MDW	Delayed ECG waveform	1/6
MIXSND	Mixed sound (alarm and synchronized QRS pulse) signal	3/6
ON/OFF	Synchronized QRS pulse sound on/off switching signal	3/6
OUTB0-3	8279 (CPU Board) output signal B	3/6
RD	CNS data reception signal	1/6
RD RET	CNS data reception return signal	1/6
RDY/XBSY	Ready/busy status signal	2/6
RWRCTL	Power supply control signal	5/6

2. SIGNAL LIST

Symbol	Function	Part
RxD1	Receiving data (for display unit)	4/6
RxD2	Receiving data (for keypad when connected to video display VD)	4/6
RxD3	Receiving data (for keypad when connected to main unit MU)	4/6
RxDF	Receiving data signal (full key board)	4/6
SaO2	SaO2 tone/normal synchronized with QRS pulse sound signal	3/6
SD	Data transmission signal for CNS	1/6
SD RET	Data transmission return signal for CNS	1/6
SL0-3	CPU Board 8279 scan line signal	3/6
SNDINH	Sound inhibit signal	3/6
SRSL1-4	Shift register select signal	4/6
STNBY	Power standby control signal	5/6
TCCLR	Timer condenser clear signal	5/6
TOSC	Tone oscillator signal	3/6
TxD1	Transfering data (for display unit)	4/6
TxD2	Transfering data (for keypad when connected to video display VD)	4/6
TxD3	Transfering data (for keypad when connected to main unit MU)	4/6
TxDF	Transfering data (full key board)	4/6
W/XR	Read/write control (or select) signal	2/6
WP	Memory card write protect signal	2/6
X1CHIPW	Write signal for 1CHIP CPU	4/6
XAL	Alarm signal	1/6
XBUSY2	CNS data transmission interrupt request signal	1/6
XBUSY2 RET	CNS data transmission interrupt request return signal	1/6
XCD1, 2	Memory card detection signal	2/6
XCE1, 2	Memory card enable signal	2/6
XDEL	Lower byte data bus buffer enable signal	2/6
XDEU	Upper byte data bus buffer enable signal	2/6
xDSRF	Data set to ready signal (full key board)	4/6
XERESET	Auxiliary reset signal to CPU board	5/6
XEXTRST	Auxiliary reset (switch) signal	5/6
XHO	ECG measure signal	1/6
XHT	Synchronized QRS pulse signal	3/6
XHTOUT	ECG synchronized signal	1/6
XINTR	Communication interrupt request signal	1/6

Symbol	Function	Part
XINTR RET	Communication interrupt request return signal	1/6
XIOSL1-3	I/O port select signal	2/6
XLEDSEL	LED select signal	4/6
XMCPORTR	Memory card port read	2/6
XMCPORTW	Memory card port write	2/6
XMCSW	Memory card switch status signal	2/6
XOE	Output enable signal	2/6
XRCLK	Clock latch signal	4/6
XRD1, 2	72001 read	4/6
XRDYF	Ready signal (full key board)	4/6
XREG	Attribute memory space select signal	2/6
XRETRN	Retry control port enable signal	4/6
XRSTF	Reset signal (full key board)	4/6
XRTYF	Retry signal (full key board)	4/6
XSRSEL	Serial clock select signal	4/6
XWE	Write enable signal	2/6

2-1-5 UR-3027, CPU Board

Symbol	Function	Part
A01-23	Internal address bus 01-23	1/16
CEXT	RAM's buffer condenser terminal	14/16
CLK16M	16MHz System clock	1/16
CLK2M	2MHz clock	2/16
CLK500K	500kHz clock	2/16
CLKSAMPL	Syncronization signal for copying waveform data	16/16
CNTL/STB	8279 control/strobe signal	13/16
CTS	Clear signal to send from 71051	12/16
D00-15	Internal data bus 00-15	1/16
DSR	71051 data set to ready	12/16
DTR	71051 data terminal ready	12/16
ERESET	External reset signal (positive logic)	4/16
FC0-2	Interrupt request encoding signal	1/16
FG	Ground	12/16
I51TXRDY	Ready to transmit signal from 8251	6/16
I51XRXDY	Ready to receive signal from 8251	6/16
I54OUT2	71054 signal 2 counter	6/16
I6242STD	6242 standard clock	6/16
I79IRQ	Interrupt request signal from 8279	6/16
IACK	Interrupt request acknowledge signal	3/16
INT10-17	Interrupt level 10-17	6/16
LDS	Lower byte data strobe signal on system bus	1/16
OUTA0-3	8279 data output A0-3	13/16
OUTB0-3	8279 data output B0-3	13/16
R/XE	High level read;Low level write	1/16
R/XWB	System read/write control signal	16/16
RL0-7	8279 return lines 0-7	13/16
RTCSL	Real time clock select signal	3/16
RTS	Data request signal for sending data from 71051	12/16
RXD	Receive data	12/16
SG	Ground signal	12/16
SHIFT	8279 shift signal	13/16
SL0-3	8279 scan lines 0-3	13/16
TXD	Transmit data	12/16

Symbol	Function	Part
VB	Battery voltage	11/16
WRDL	Lower byte write signal	2/16
WRDU	Upper byte write signal	2/16
WTDERR	Watch dog timer error signal	4/16
WTDSTOP	Watch dog timer stop control signal	4/16
XADDR01-23	System address bus (negative logic)	15/16
XAS	Address strobe signal	1/16
XASB	System address strobe signal	16/16
XBERR	Bus error	1/16
XDATA00-16	System data bus (negative logic)	15/16
XDRACK	Data acknowledge signal	1/16
XDS/LEDS	Dip switch/LED select signal	3/16
XDTACKB	System data acknowledge signal	16/16
XE2PSL	EEPROM select signal	11/16
XE2PSL	EEPROM select signal	3/16
XEBUS	System bus select signal	3/16
XERESET	External reset signal (negative logic)	4/16
XHALT	Halt signal for CPU	1/16
XI51SL	71051 select signal	3/16
XI54ACK	71054 acknowledge signal	6/16
XI54SL	71054 select signal	3/16
XI62ACK	6242 acknowledge signal	6/16
XI79SL	8279 select signal	3/16
XIACK1-2	Interrupt acknowledge signal 1-2	5/16
XIACK10-17	nterrupt acknowledge 10-17	6/16
XINT10-50	Interrupt signal 10-50	16/16
XINT7	Interrupt level 7	4/16
XIO	I/O port select signal	3/16
XIORD	I/O port read signal	2/16
XIORST	System reset signal	16/16
XIOWR	I/O port write signal	2/16
XIPL0-2	Interrupt request priority level	1/16
XLDSB	System lower byte data strobe signal	16/16
XPDOWN	Power down indication signal (generated in UP-0315)	4/16
XPWDWN	Voltage down indication signal	11/16
XRAM	RAM select signal	3/16

2. SIGNAL LIST

Symbol	Function	Part
XRAM0SL-XRAM3SL	RAM0-3 select signal	3/16
XRDL	Lower byte read signal	2/16
XRDU	Upper byte read signal	2/16
XRESET	Reset signal for CPU	1/16
XROM	ROM select signal	3/16
XROM0SL-XROM3SL	ROM0-3 select signal	3/16
XRTCSL	6264 select signal	11/16
XST/WTDS	Status/watch dog select signal	3/16
XUDS	Upper byte data strobe signal on system bus	1/16
XUDSB	System upper byte data strobe signal	16/16
XVPA	Valid peripheral address	1/16
XWTDLAMP	Watch dog timer lamp control signal	4/16
XWTDSTB	Watch dog timer strobe signal	4/16

2-2 Keypad, RY-881PA

2-2-1 CONSOLE Board, UR-3025

Symbol	Function	Part
READY	Ready	
RxD2	Receiving data signal	
TxD2	Transmit data signal	
XP.SCTL2	Power status control signal	
XRESET	Keypad reset signal	

2-3 Display Unit, VD-881R

2-3-1 OPERATION CONTROL Board, UP-0801

Symbol	Function	Part
ALSND	Alarm sound	3/4
ALSND20	Alarm sound signal amplified 20 times	3/4
ALSNDGND	Ground for alarm sound	3/4
ALSNDOFF	Alarm sound OFF	2/4
CLICK	Key sound	2/4
CMPS	CRT unit NTSC signal	1/4
COMP	NTSC signal input control from auxiliary unit (output port)	1/4
CSND	Composite SND signal	3/4
ECOMPS	NTSC signal from auxiliary unit	1/4
EHSYNC	Horizontal synchronizing signal from auxiliary unit	1/4
ER,EG,EB	RGB signals from auxiliary unit	1/4
ERG,EGG,EBG	Ground for individual RGB signals from auxiliary unit	1/4
EVIDEO	RGB signals input control from auxiliary unit (output port)	1/4
EVSYNC	Vertical synchronizing signal from auxiliary unit	1/4
EXSN	Auxiliary unit input sound	4/4
EXSNDGND	Ground for auxiliary unit input sound	4/4
EXSNDSEL	Auxiliary unit input sound select	2/4
HSYNC	CRT unit horizontal synchronizing signal	1/4
HTSND	QRS synchronized pulse sound	3/4
HTSND25	QRS synchronized pulse sound signal amplified 25 times	3/4
HTSNDGND	Ground QRS synchronized pulse sound	3/4
KREADY	Keypad ready signal	2/4
M/XS SEL	Master/slave select	2/4
MHSYNC	Horizontal synchronizing signal from main unit	1/4
MR,MG,MB	RGB signal from main unit	1/4
MRG,MGG,MBG	Ground for individual RGB signals from main unit	1/4
MVSYNC	Vertical synchronizing signal from main unit	1/4
R,G,B	CRT unit RGB signals	1/4
READY	Ready signal	2/4
REMOTE	Remote control infra-red signal	2/4
RxD1	Receiving data signal to main unit	2/4

Symbol	Function	Part
RxD2	Receiving data signal to keypad	2/4
SALSND20	Select ALSND20 signal	4/4
SCSND	Select CSND signal	3/4
SLEEP	Sleep screen port output	2/4
SPKR+	Speaker signal	3/4
SPKR-	Speaker signal	3/4
TxD1	Transferring data to main unit	2/4
TxD2	Transferring data to keypad	2/4
VALSND	ALSND signalwith volume information added	3/4
VHT/EXSND	HT/EXT SND signal with volume information added	3/4
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WSLEEP	Sleep sound	3/4
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XALPLY	Alarm pole YELLOW output	2/4
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XEVIDEO	RGB signals input control signal from auxiliary unit signal	1/4
XEXCOMP	NTSC signal input control signal from auxiliary unit signal	1/4
XHT	QRS synchronized pulse signal for alarm pole	2/4
XP.SCTL1	Power status control signal to power supply unit signal	2/4
XP.SCTL2	Power status control signal to main unit signal	2/4
XP.SCTLIN	Power status control signal from keypad	2/4
XRESET1	VD reset	2/4
XRESET2	Keypad reset	2/4

2-3-2 OPERATION (VR) Board, UP-0802

Symbol	Function	Part
BRIGHT	Brightness control signal	
CONT	Contrast control signal	

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3-1 JA-DPU Analog Signal Processor

Each head amplifier board amplifies the measuring parameter and transfers the analog signals to the DPU board (UP-0670).

The DPU board time-shares the analog signals with a 16-channel multiplexer and converts the analog signals to digital signals with a 12 bit D/A converter through a d.c. level shift circuit and sample hold circuit according to each specified timing.

The digital signals are displayed on the CRT after being gain-controlled, filtered and formatted by software while the digital signals are converted to analog signals for a recorder or central monitor.

All the signal process timings are synchronized with a SYNC signal (16 msec interval clock)

Each measuring parameter signal is processed as follows.

3-1-1 Electrocardiogram (ECG) Signal

On the ECG Head Amp board (UP-0272), two leads of an ECG signal are pre-amplified and time-shared to be one signal (2ch ECG).

On the JA I/F Main board (UP-0270), a 2ch ECG signal is demultiplexed to be the two leads of an ECG signal (ECG1 & ECG2). The output signal is kept to be 15 times as much as the input signal on UP-0272 so that a polarization voltage (DC component) on a electrode causes saturation since ECG1 and ECG2 signals include a DC component.

On the DPU board (UP-0670), ECG1 and ECG2 from the UP-0270 are amplified to be 1V to 15mV through 15mV calibration, the Pacing pulse limiter circuit, DC eliminator time constant selector and Auto-instantaneous short circuit. ECG1 and ECG2 are converted to digital signals through the HUM filter ON/OFF selector while ECG1 and ECG2 are branched to be ECG1W and ECG2W signals for the recorder (WS) or central monitor (CNS). ECG1W and ECG2W are real-time signals through the Low-pass filter ON/OFF selector since the A-D and D-A converter circuit cannot minutely reproduce the high frequency component (up to 100Hz).

3-1-2 Respiration Signal

On UP-0272, impedance variation(Ω) between electrode “R”(RA) and “F”(LL) led by respiration is transferred to the transformer (T003).

On the RESP Amp board (UP-0271), the impedance variation induces the minute amplitude variation on an 80kHz sine carrier wave. The minute signal is amplified up to 50 mV/Ω, including the DC component.

On UP-0670, the signal is amplified up to 1V/Ω, excluding the DC component, and converted to a digital signal.

3-1-3 Blood Pressure Signal

On the PRESS Head Amp board (UP-0369), Blood pressure signals P1 and P2 are individually amplified, time-shared with the analog switch (IC003A), modulated/demodulated with the 64kHz clock (F-CLK) for floating and outputted to UP-0670 up to 1 V/100 mmHg.

On UP-0670, the signal is inputted to the 16ch multiplexer, doubled by the Gain selector circuit, added to the ADSFT signal to shift DC level in auto-zeroing operation and converted to a digital signal. Blood Pressure signal for WS or CNS is the output signal (P1W to P4W) after D-A converter (8 msec sampling).

3-1-4 Cardiac Output (CO) Signal

On the CO Head Amp board (UP-0318), the following four signals are time-shared during a 16msec interval on a SYNC signal.

1) REF: 0 V Reference voltage for 0 °C in Ti or 27 °C in Tb
2) Ti: Voltage for Injection fluid temperature (1 V/10 °C)
3) Tb: Voltage for Blood temperature (1 V/5 °C)
4) ΔTb: Voltage for Blood temperature variation in fluid injection (1V/0.5 °C)

On UP-0670, the signals are converted to digital signals synchronized with the output from UP-0318.

3-1-5 Temperature Signal

On TEMP Head Amp board (UP-0319), the following four signals are time-shared during a 16 msec interval on a SYNC signal.

1) REF27: Reference voltage for 27 °C in T1 or T2
2) CAL37: Calibration voltage for 37 °C (1V/5 °C)
3) T1: Voltage for Temperature-1 (1 V/5 °C)
4) T2: Voltage for Temperature-2 (1 V/5 °C)

On UP-0670, the signals are converted to digital signals synchronized with the output from UP-0319.

3-2 Main Unit, MU-881R

3-2-1 COM3 Board, UP-0563

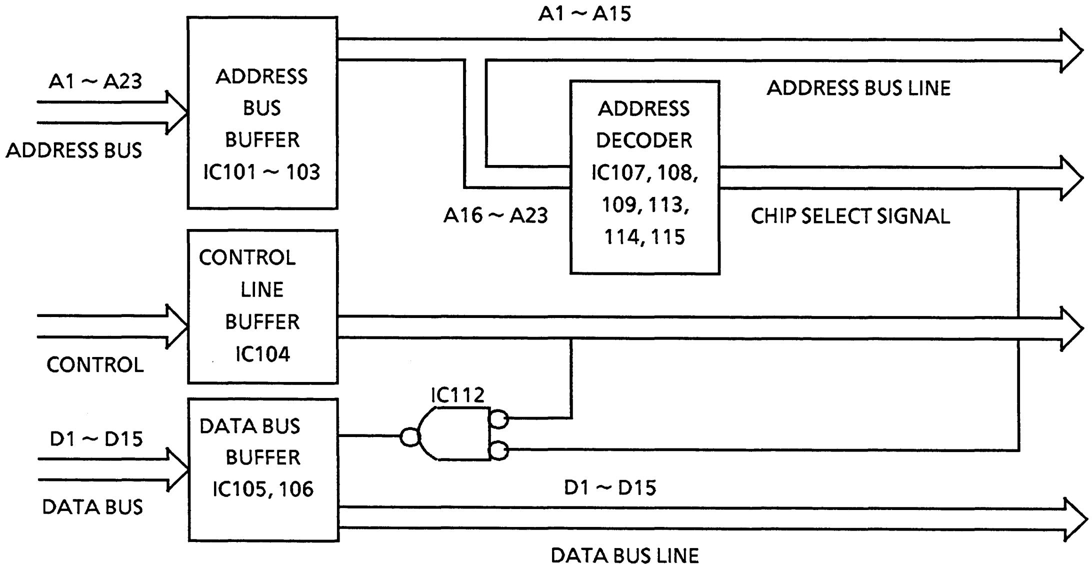
◆ General

The COM3 board mainly functions as CNS interface and WS recorder interface through the dual-port RAM.

◆ Decoder

● Address decoder, Buss buffer
IC101,102 and 103(HCT240) are used for the buffer of address bus.
IC104(HCT244) is used for the buffer of control line.
IC105 and 106 (HCT640) are used for the buffer of data bus.
IC107,108(HC138),IC113(HC130),IC114(F04) and IC115(F20) are used as address decoder.
IC112(HC32) operates as gate opener & closer of data buss buffer.
In decoder part, each chip select signal(CS) is asserted by following devices.

CS	DEVICE
XCS3	ROM 128 KByte
XCS4	SRAM 64 KByte
XCS5	SRAM 64 KByte
XCS1	MB8421(2 port RAM,using lower byte only)
XCS0	WS Recorder RESET port(IC118)

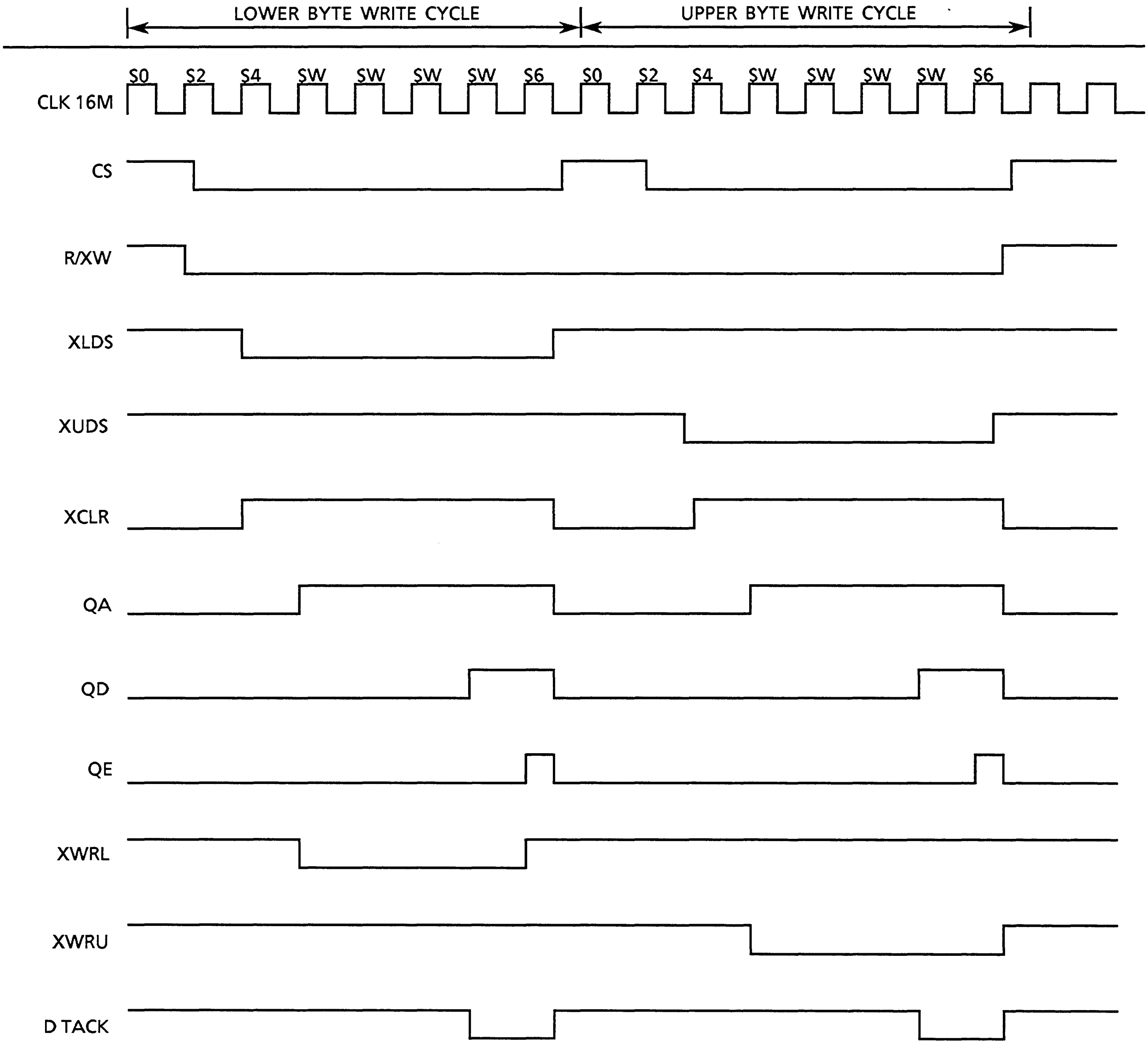

A1 ~ A15
A1 ~ A23
ADDRESS BUS
ADDRESS BUS BUFFER IC101 ~ 103
ADDRESS BUS LINE
ADDRESS DECODER IC107, 108, 109, 113, 114, 115
A16 ~ A23
CHIP SELECT SIGNAL
CONTROL LINE BUFFER IC104
CONTROL
IC112
D1 ~ D15
DATA BUS BUFFER IC105, 106
DATA BUS
D1 ~ D15
DATA BUS LINE

● XWR,XRD,XDTACK Generator

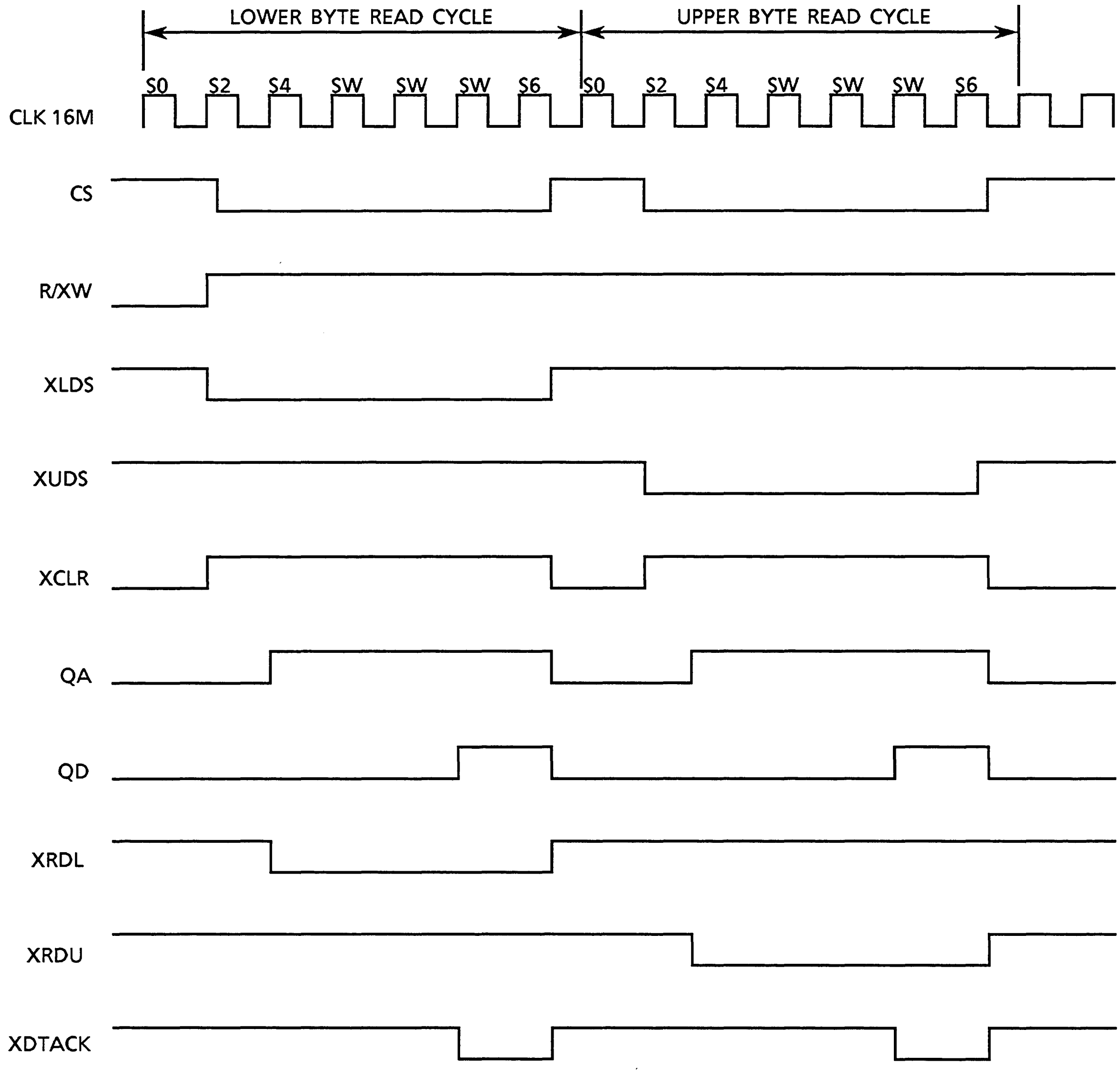
When CPU68000 on the CPU board accesses COM3 board, the decoder operates and the chip select signal on IC116(F164) falls into assert condition "H".

If the request from CPU board comes later than XBUSYR, the CPU request falls into wait condition.

*** WRITE CYCLE TIMING CHART**


LOWER BYTE WRITE CYCLE
UPPER BYTE WRITE CYCLE
S0
S2
S4
SW
SW
SW
SW
S6
S0
S2
S4
SW
SW
SW
SW
S6
CLK 16M
CS
R/XW
XLDS
XUDS
XCLR
QA
QD
QE
XWRL
XWRU
D TACK

* READ CYCLE TIMING CHART

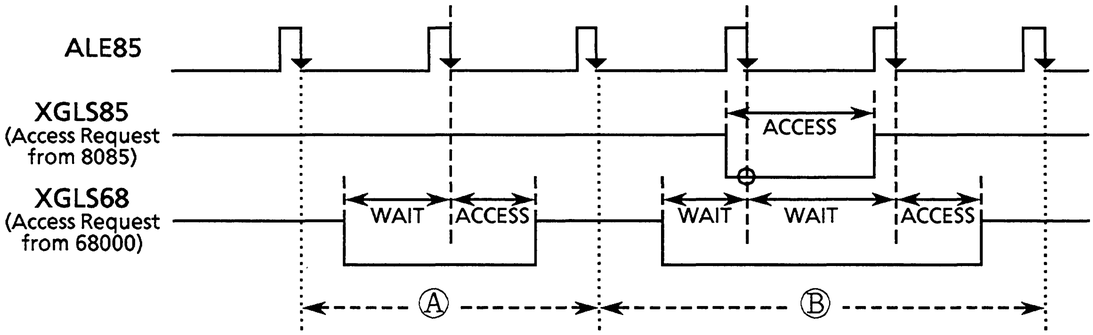

LOWER BYTE READ CYCLE
UPPER BYTE READ CYCLE
S0
S2
S4
SW
SW
SW
S6
S0
S2
S4
SW
SW
SW
S6
CLK 16M
CS
R/XW
XLDS
XUDS
XCLR
QA
QD
XRDL
XRDU
XDTACK

◆ Global Memory & Control Circuit

• Global Memory Control circuit

The circuit controls the access request to the global memory (IC012) RAM from both MPUs (8085 on this board and 68000 on the CPU board).

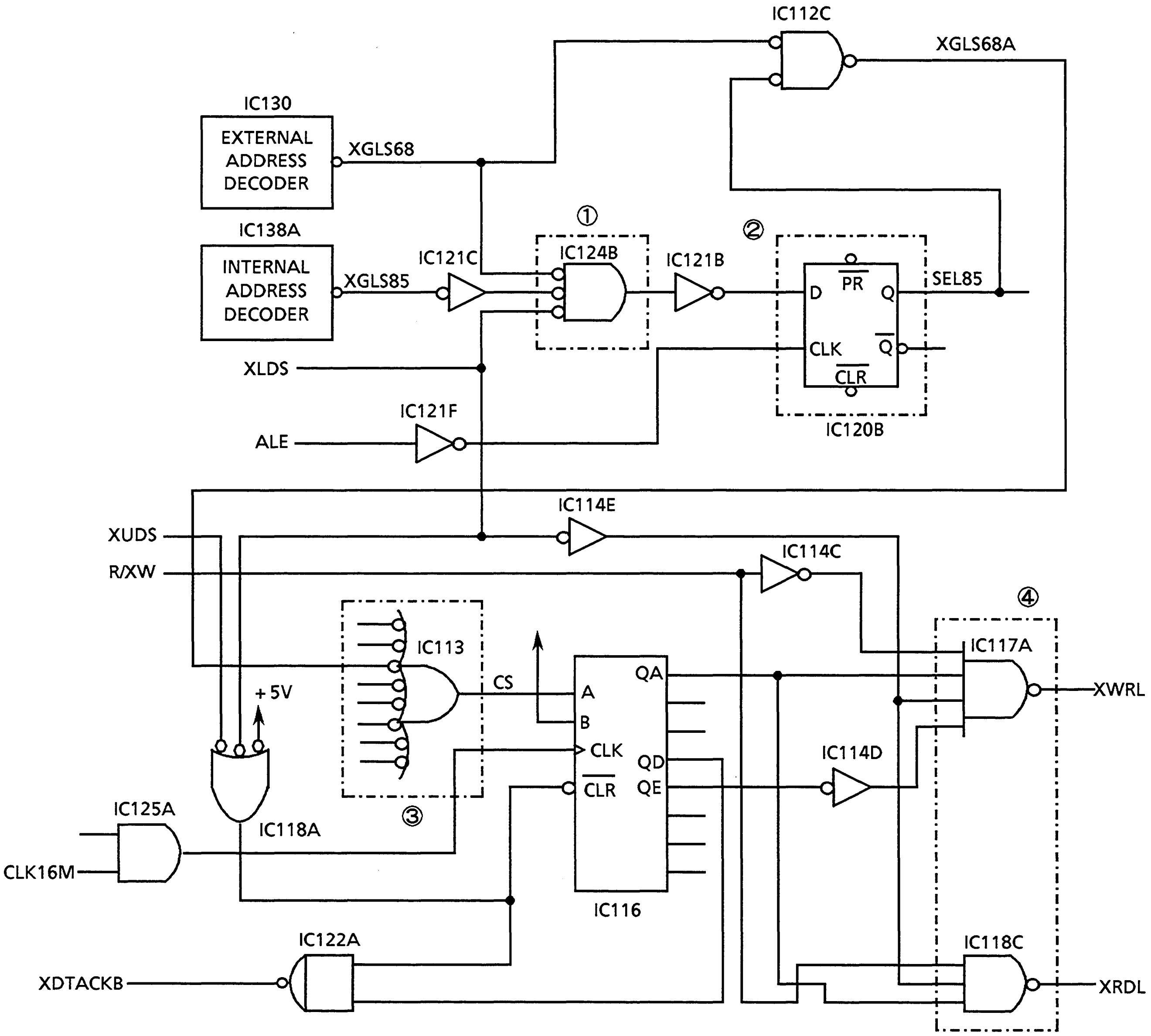
1) Access Priority Timing Chart
   The access to the RAM (IC012) from the MPU8085 always governs.
   The access to the RAM (IC012) from the MPU68000 is done according to the following timing chart.


ALE85
XGLS85
(Access Request from 8085)
ACCESS
XGLS68
(Access Request from 68000)
WAIT
ACCESS
WAIT
WAIT
ACCESS
Ⓐ
Ⓑ

Ⓐ When there is an access request from the MPU68000 only, the circuit accepts the access from the MPU68000 and starts the access with the negative going edge of ALE85 signal.

Ⓑ When there are access requests from both the MPU8085 and 68000, the circuit leads the access from the MPU8085 and starts with the negative going edge of ALE85 signal. After completing the access from the MPU8085, the circuit starts the access from the MPU68000 with the next negative going edge of ALE85 signal.

2) Access Priority Judgment Function


IC112C
XGLS68A
IC130
EXTERNAL ADDRESS DECODER
XGLS68
IC138A
INTERNAL ADDRESS DECODER
XGLS85
IC121C
①
IC124B
IC121B
②
D
PR
Q
CLK
Q
CLR
SEL85
IC120B
XLDS
IC121F
ALE
IC114E
XUDS
R/XW
IC114C
④
IC113
CS
+5V
A
B
CLK
CLR
QA
QD
QE
IC116
IC117A
XWRL
IC114D
IC125A
CLK16M
IC118A
③
IC122A
XDTACKB
IC118C
XRDL

① When there are access requests from both the MPU8085 and 68000, the circuit blocks the access request from the MPU68000.

② The circuit judges whether there is an access request from the MPU8085 at the negative going edges of ALE85 signal.

③ When there is an access request from the MPU8085 (SEL85: High level), the Shift Register (IC006) is not reset and doesn't transfer the XDTACK signal to the MPU68000. Therefore, the MPU68000 keeps on waiting for access to the RAM (IC126) until the access from the MPU8085 is completed.

④ The circuit blocks the control signals to the RAM (IC126) from the MPU68000, XWRL & WRDL, under the above condition ①.

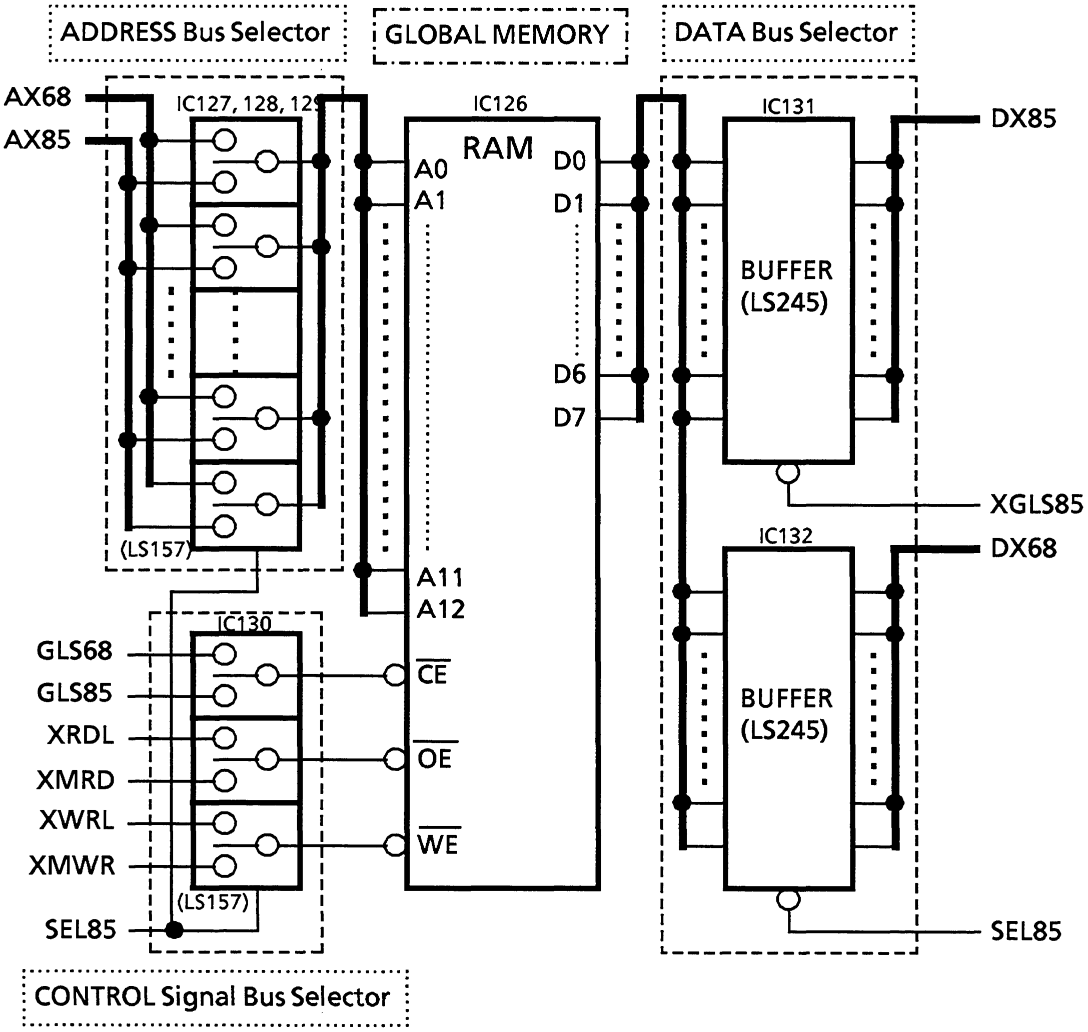
- **Global Memory circuit** (Bus Selector)

The circuit (Bus selector) selects the Internal Bus (from 8085) or System Bus (from 68000) to connect with the global memory RAM (IC126) according to the Global Memory Control circuit.

The bus selector consists of the Address Bus Selector, Control signal Bus Selector and Data Bus Selector.

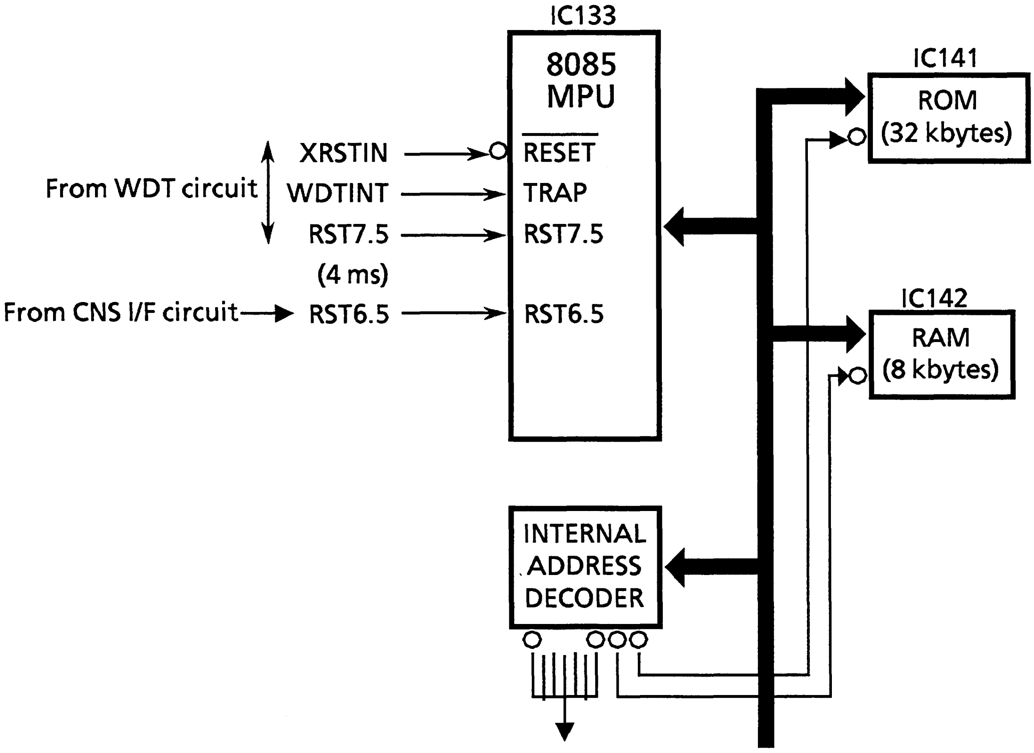
The former two are controlled by the Analog Switches (IC025/039/040, 024), LS157.

The latter one is controlled by the Buffer (IC131, 132), LS245.


ADDRESS Bus Selector
GLOBAL MEMORY
DATA Bus Selector
AX68
AX85
IC127, 128, 129
(LS157)
IC126
RAM
A0
A1
A11
A12
D0
D1
D6
D7
CE
OE
WE
IC131
BUFFER (LS245)
DX85
XGLS85
IC132
BUFFER (LS245)
DX68
SEL85
IC130
GLS68
GLS85
XRDL
XMRD
XWRL
XMWR
(LS157)
SEL85
CONTROL Signal Bus Selector

◆ CNS Interface

• CPU/ROM/RAM circuit

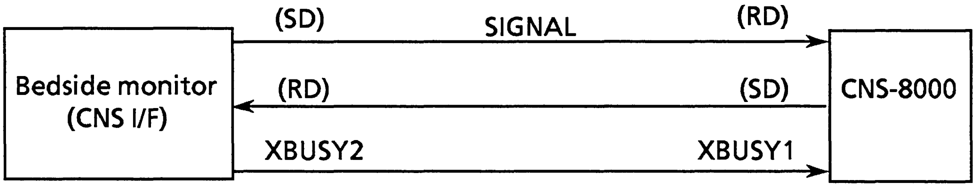

IC133
8085 MPU
RESET
TRAP
RST7.5
RST6.5
XRSTIN
WDTINT
RST7.5
(4 ms)
RST6.5
From WDT circuit
From CNS I/F circuit
IC141
ROM (32 kbytes)
IC142
RAM (8 kbytes)
INTERNAL ADDRESS DECODER

The circuit consists of MPU8085 (IC053), ROM (IC141), RAM (IC142) and the Internal Address Decoder.
The circuit controls the other circuits on the COM3 board.
The MPU8085 on the circuit provides the following Input/Output for Control signals.

Pins	Description
RESET	Reset Input
TRAP	Watch Dog Timer Error Interrupt Request Input
RST7.5	Periodic Interrupt Request Input (every 4msec)
RST6.5	Interrupt Request Input upon receipt of Address/Command signal from CNS (I/F)

• CNS I/F (Interface) circuit

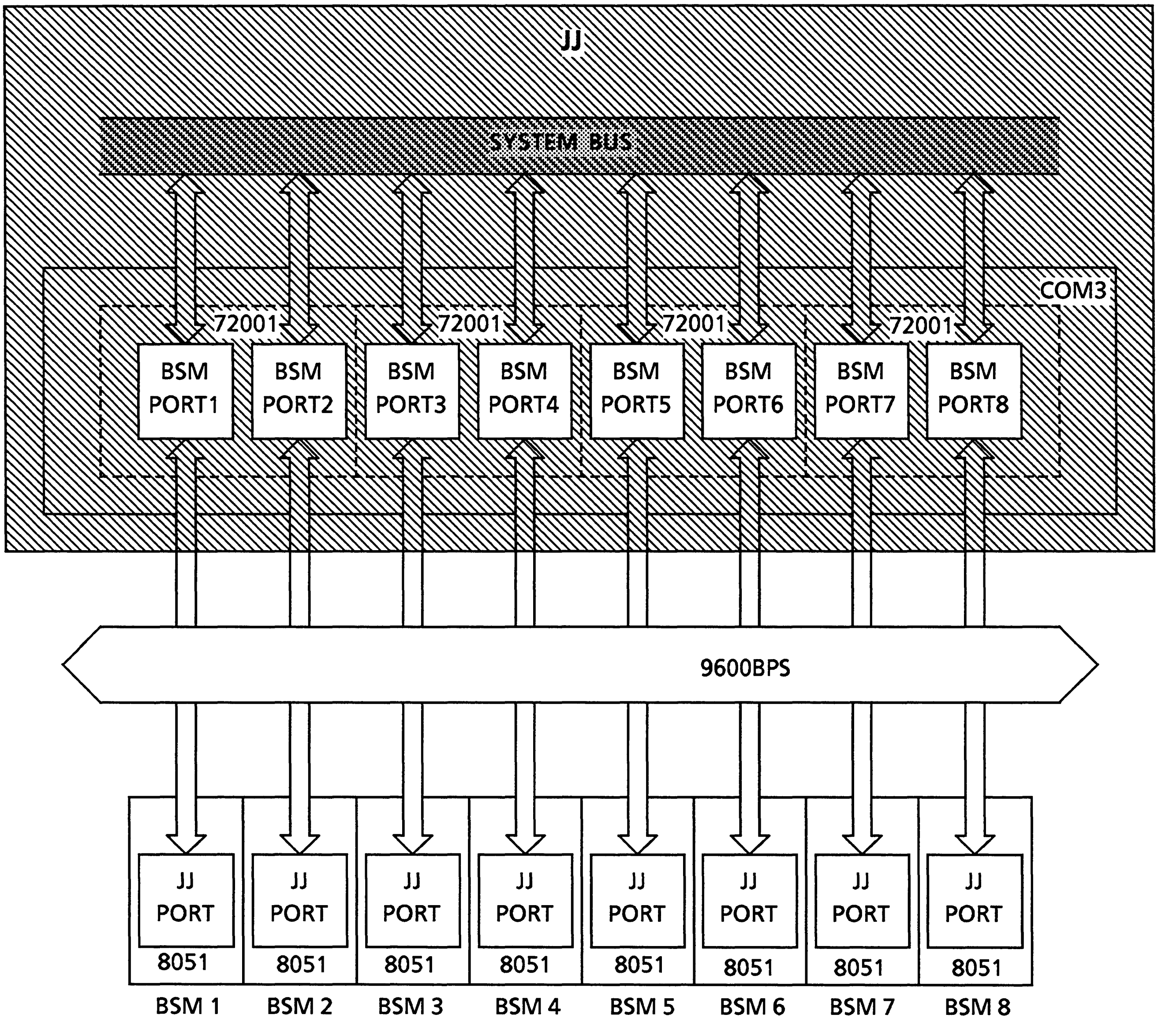
The circuit provides communication functions with the Central Monitor (CNS-8000 series) as follows:


(SD)
SIGNAL
(RD)
Bedside monitor
(CNS I/F)
(RD)
(SD)
CNS-8000
XBUSY2
XBUSY1

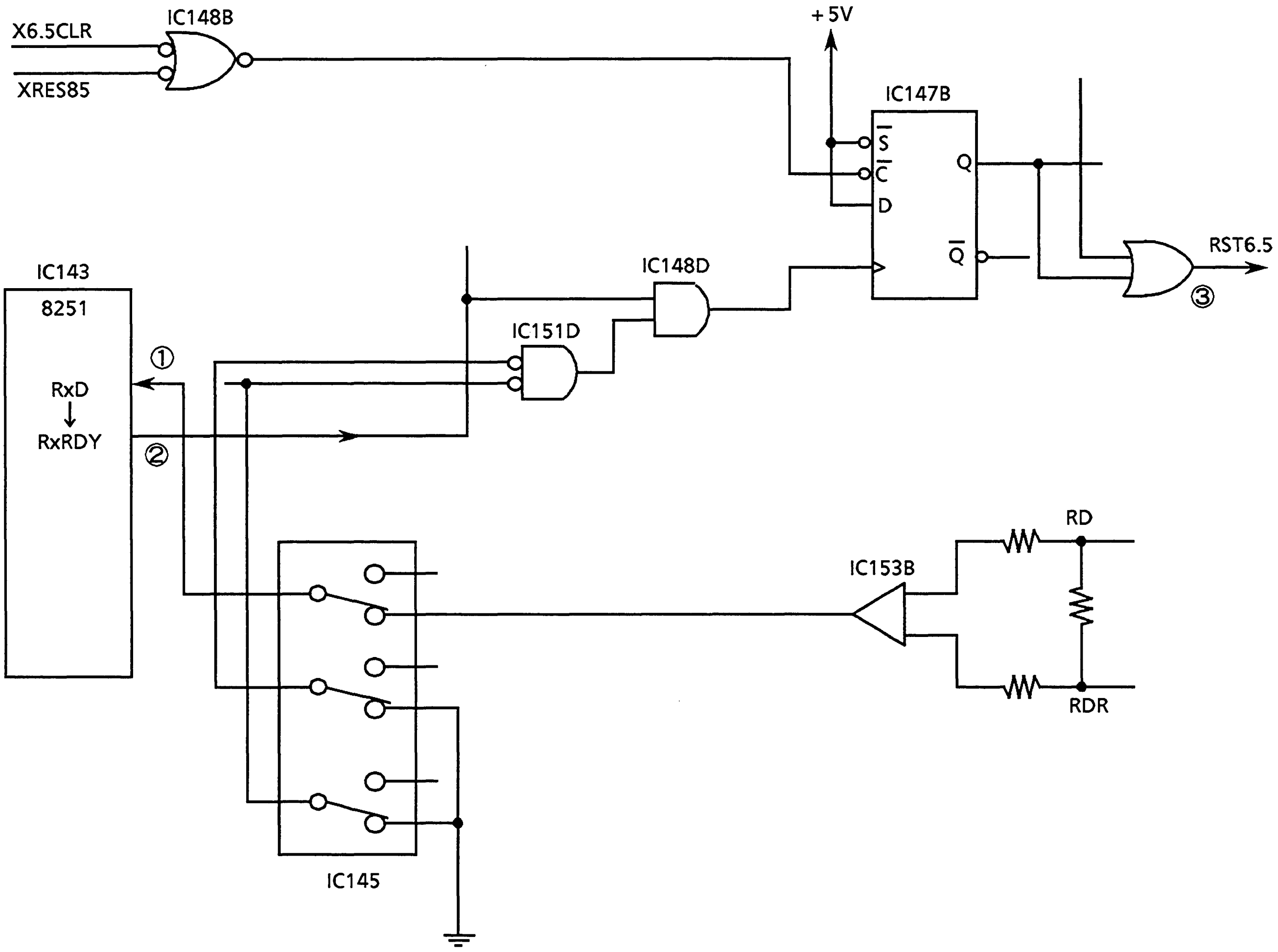
Symbol	Transfer direction	Description
SD	MONO	Send Data (asynchronous, 9600 bps)
RD	MONO	Receive Data
XBUSY2	MONO	Data is transferring to CNS and any request signal is rejected

• BSM-JJ communication sequence

Each bedside monitor communicates independently with the independent port of JJ. The communication method is a double-asynchronous method with baud rate of 96000 bps.


JJ
SYSTEM BUS
COM3
72001
72001
72001
72001
BSM PORT1
BSM PORT2
BSM PORT3
BSM PORT4
BSM PORT5
BSM PORT6
BSM PORT7
BSM PORT8
9600BPS
JJ PORT
8051
BSM 1
BSM 2
BSM 3
BSM 4
BSM 5
BSM 6
BSM 7
BSM 8

● Address Receive operation

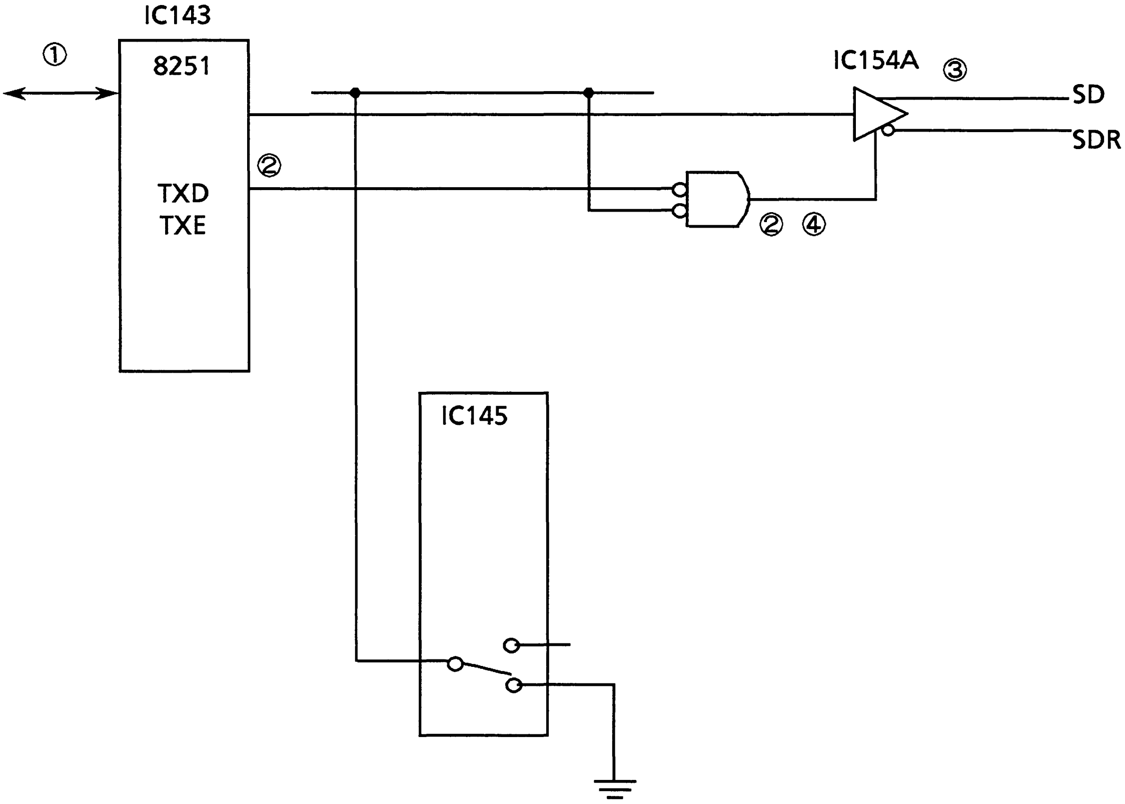

X6.5CLR
XRES85
IC148B
+5V
IC147B
S̄
C̄
D
Q
Q̄
RST6.5
③
IC143
8251
RxD
RxRDY
①
②
IC148D
IC151D
IC153B
RD
RDR
IC145

① A receive data is transferred to the RxD terminal on the IC143 from CNS through the SIGNAL line.
② Receive Interrupt Request signal RxRDY is asserted while the data is set on the Receive Register in the IC143.
③ Interrupt Request signal to the MPU8085, RST6.5, is generated.

When RST6.5 is generated, the MPU8085 reads the data on the Receive Register.

After reading the data, RxRDY is cleared and RST6.5 is also reset.

- **Data Transmit operation**



① A transmit data is set on the Transmit Register in the IC143 (8251) by the MPU8085.

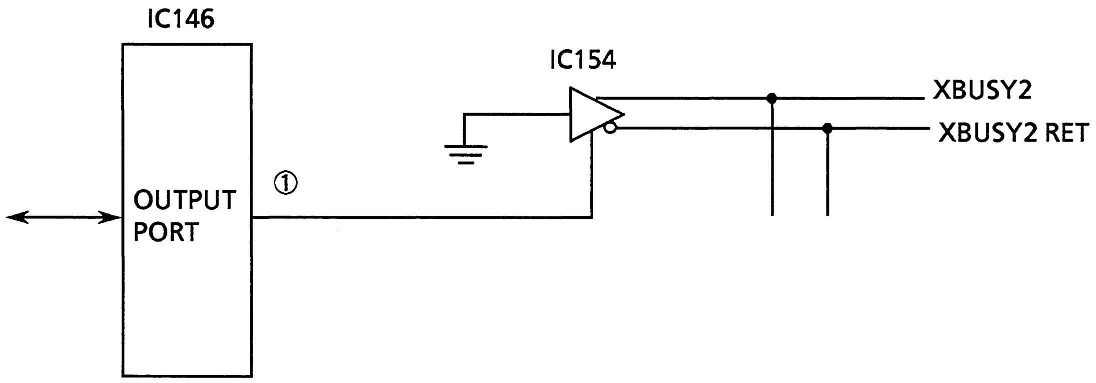
② A receive data is blocked while the Transmit Driver (IC145) is set to enable by setting the TxE signal to be active-low.

③ The transmit data is transferred to the SIGNAL line.

④ When the transmit data is completed to transfer, the Transmit Driver is set to disable by setting the TxE signal to be inactive-high.

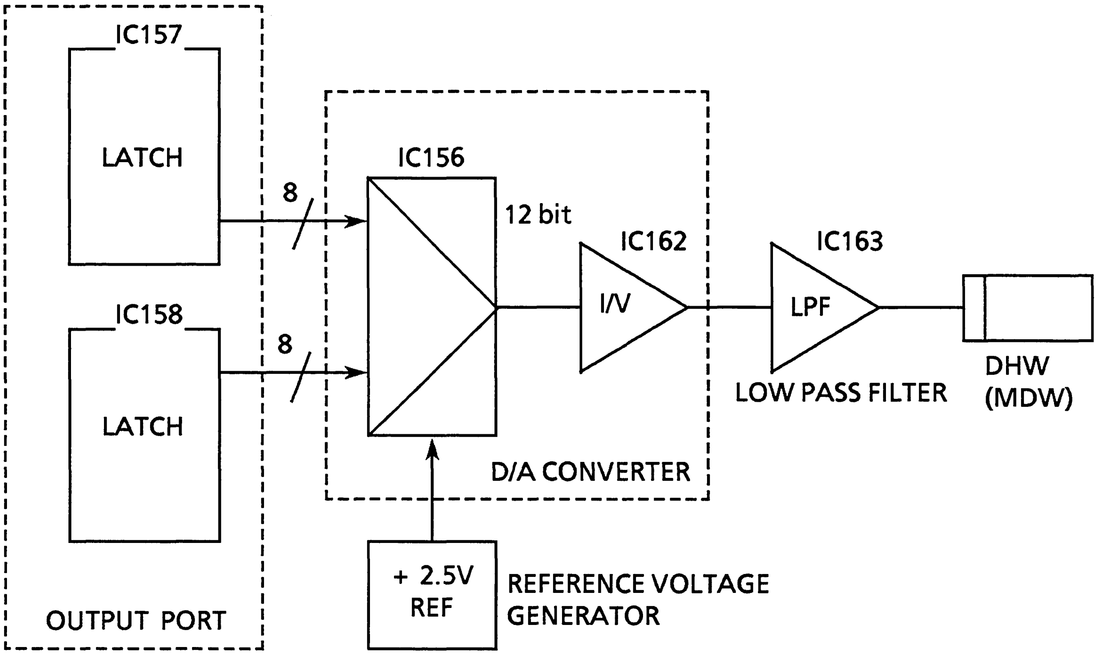
●"BUSY" signal Transmit operation

When the processing work of MPU8085 is going to be overload,XBUSY control signal is set to active in order to let the transmit operation from JJ wait.

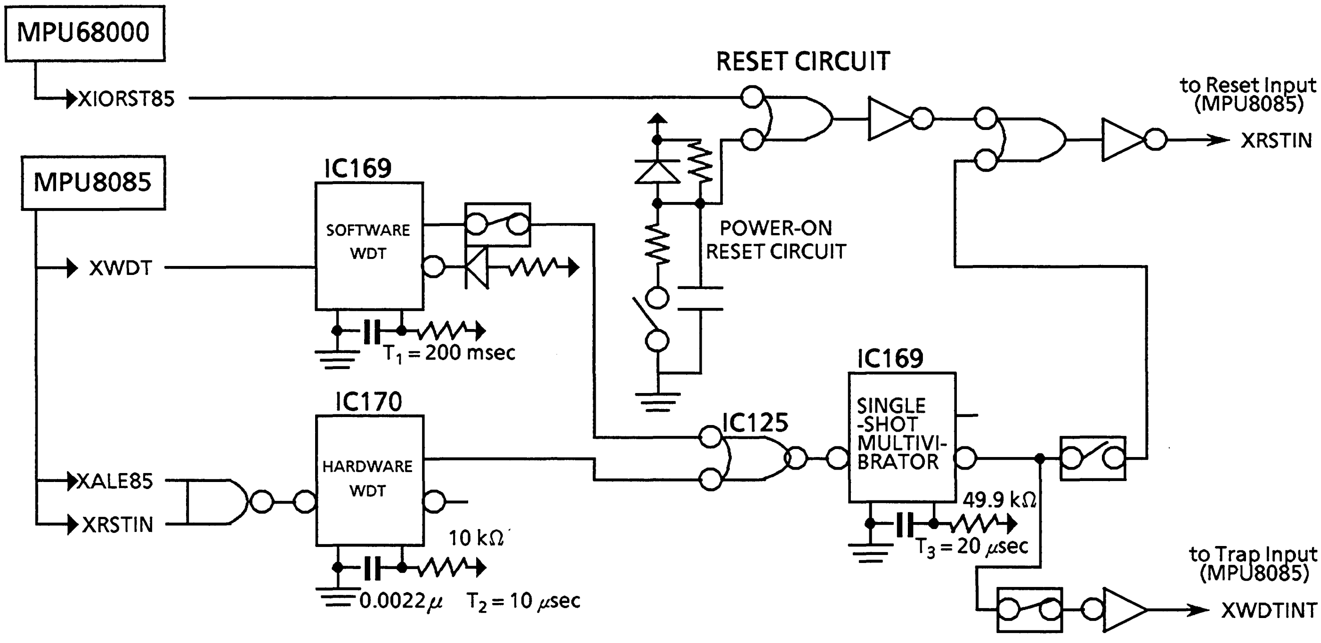

IC146
OUTPUT PORT
①
IC154
XBUSY2
XBUSY2 RET

◆ Delayed ECG Waveform(MDW) Generator

The delayed ECG waveform is generated by this part to transmit them to CNS for remote recording.
The circuit consists of Output port, D/A converter, Low pass filter, and Reference voltage generator.
The delayed ECG waveform,which is obtained CPU board through global memory, is output at every 4ms to output port of IC157/158 by CPU(IC133) of COM3 board.
The reference voltage generator supplies DC + 2.5 V to D/A converter.


IC157
LATCH
IC158
LATCH
OUTPUT PORT
8
8
IC156
12 bit
IC162
I/V
D/A CONVERTER
IC163
LPF
LOW PASS FILTER
DHW
(MDW)
+ 2.5V
REF
REFERENCE VOLTAGE
GENERATOR

◆ WDT/LED/SW Circuit


MPU68000
XIORST85
MPU8085
XWDT
XALE85
XRSTIN
IC169
SOFTWARE WDT
$T_1 = 200$ msec
IC170
HARDWARE WDT
10 kΩ
0.0022μ
$T_2 = 10$ μsec
RESET CIRCUIT
POWER-ON RESET CIRCUIT
IC125
IC169
SINGLE -SHOT MULTIVI-BRATOR
49.9 kΩ
$T_3 = 20$ μsec
to Reset Input (MPU8085)
XRSTIN
to Trap Input (MPU8085)
XWDTINT

- **Watch Dog Timer (W.D.T.) circuit**

If the MPU8085 runs away, the circuit generates a TRAP Interrupt Request signal, WDTINT.
The circuit consists of the Software WDT and Hardware WDT.

*** Software WDT**

The software WDT, Single-shot Multivibrator (IC169), keeps on outputting "High" level by receiving a periodic access signal controlled by software, XWDT. If the XWDT signal is not transferred to the IC169 for 200msec. or more, the IC169 output terminal (Q) is set to "Low" level from "High" level due to the Timeout.

*** Hardware WDT**

The hardware WDT, Single-shot Multivibrator (IC170), keeps on outputting "High" level by receiving an Address Latch Enable signal from the MPU8085, XALE85. If the XALE85 signal is not transferred to the IC170 for 10 μsec or more, the IC170 output terminal (Q) is set to "Low" level from "High" level due to the Timeout.

Both outputs of the IC169 and IC170 are connected to the IC035 (Wired OR).
The output of the IC035 is processed to be 20 μsec width pulse by the single-shot multivibrator (IC169B) if either IC169 or IC170 is set to "Low" level. The 20 μsec width pulse goes to the TRAP terminal of the MPU8085 to interrupt the MPU operation.

● Reset circuit

The circuit generates a Reset signal (XRSTIN) and sends it to the Reset terminal of the MPU8085 in the following cases.

2-1)Power-on Reset circuit

The XRSTIN signal is generated for 100 msec after turning on the power switch.

2-2)Reset Command from CPU board XIORST

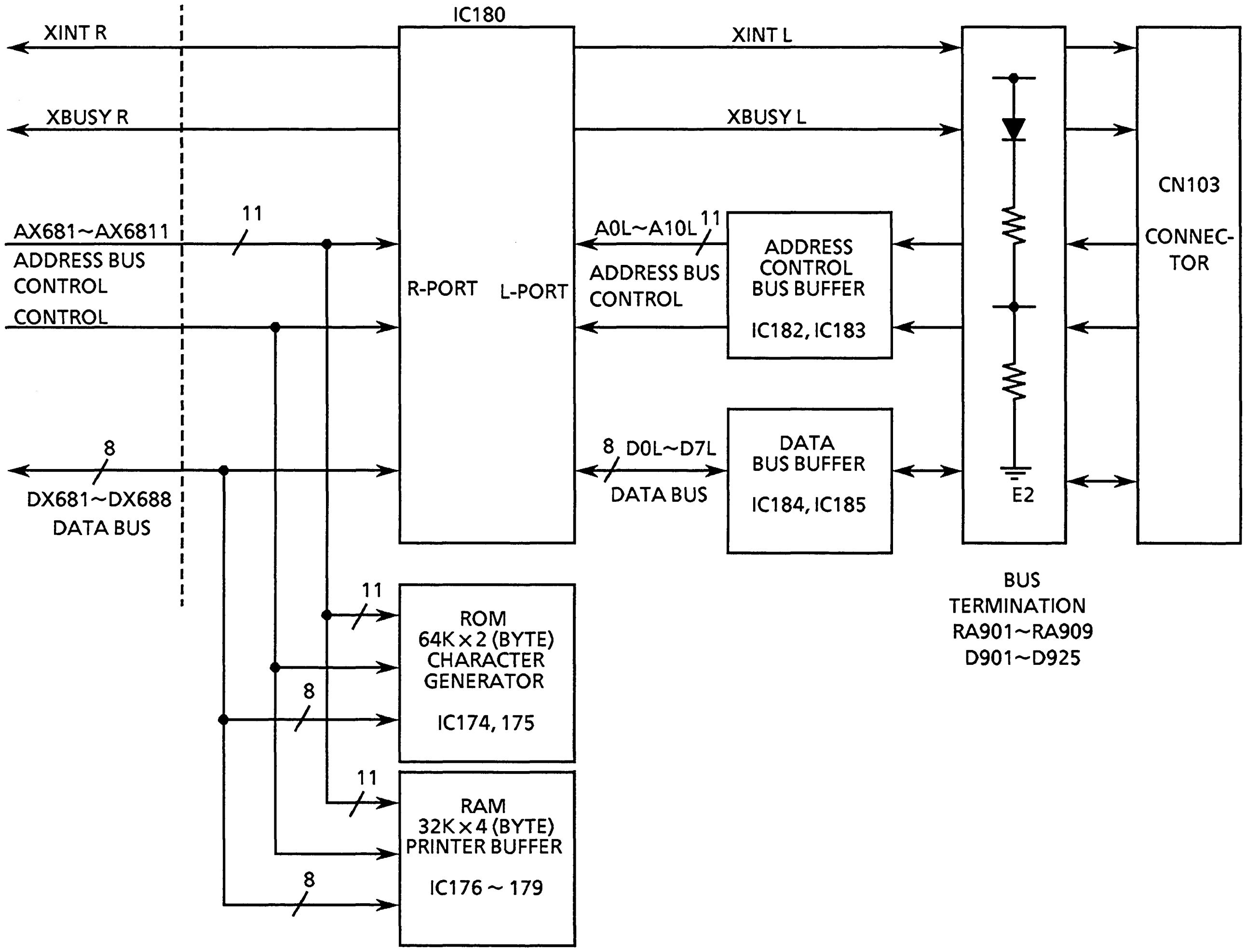
The XRSTIN signal is generated by the XIORST signal through the decoder from the MPU68000 on the CPU board.

2-3)Reset Switch SW103

The XRSTIN signal is generated by depressing the SW103. The SW103 is provided for debugging.

◆WS Interface

● General


IC180
XINT R
XBUSY R
AX681~AX6811
ADDRESS BUS
CONTROL
CONTROL
11
8
DX681~DX688
DATA BUS
R-PORT
L-PORT
XINT L
XBUSY L
A0L~A10L
11
ADDRESS BUS
CONTROL
ADDRESS
CONTROL
BUS BUFFER
IC182, IC183
8
D0L~D7L
DATA BUS
DATA
BUS BUFFER
IC184, IC185
E2
CN103
CONNEC-
TOR
BUS
TERMINATION
RA901~RA909
D901~D925
11
ROM
64K x 2 (BYTE)
CHARACTER
GENERATOR
IC174, 175
8
11
RAM
32K x 4 (BYTE)
PRINTER BUFFER
IC176 ~ 179
8

Dual port RAM IC180 (MB8421) is for receive/transmit data and command between the COM3 board and the externally connected thermal array recorder.

Address bus, data bus and control lines from the CPU that control the COM3 are inputted to the IC180 R (right) port while address bus from the WS-841R is inputted to the IC180 L (left) port. This address bus is inputted from the CN103 connector (WS) on the rear panel of the main unit and connected to the IC180 L port through the terminator composed of resistors and diodes, and address bus buffer composed of IC182 and IC183 (LS244). In the same manner as the address bus lines, control lines are connected to the IC180 L port through the bus terminator and buffer.

Data bus lines from the thermal array recorder are inputted from the CN103 and after bus terminator, the lines are buffered by different buffers during read cycle and write cycle.

- **Write cycle**

  Data is connected to the IC180 data bus through the data bus buffer IC184 (LS244).

- **Read cycle**

  Data is outputted from the IC180 and connected to the WS-841R through the data bus buffer IC185 (LS641). XINT and XBUSY signal from the IC180 L port are inverted by IC186 (LS04) to change the format to open collector output and inverted again by IC187 (LS38). These reinverted lines are also of open collector output format.

  XINT signal from the IC180 R port is buffered twice by IC186 (HC04) and inputted to the XINT11 terminal.

  XINT and XBUSY lines on both R and L ports are pulled up by 4.99kohm resistors to match the signals to the open drain format XBUSY and XINT terminals of the device.

  XINT and XBUSY lines on both R and L ports are open collector outputs to avoid the break down of CPU on WS by power failure during the recording

• Printer Buffer, Character Generator

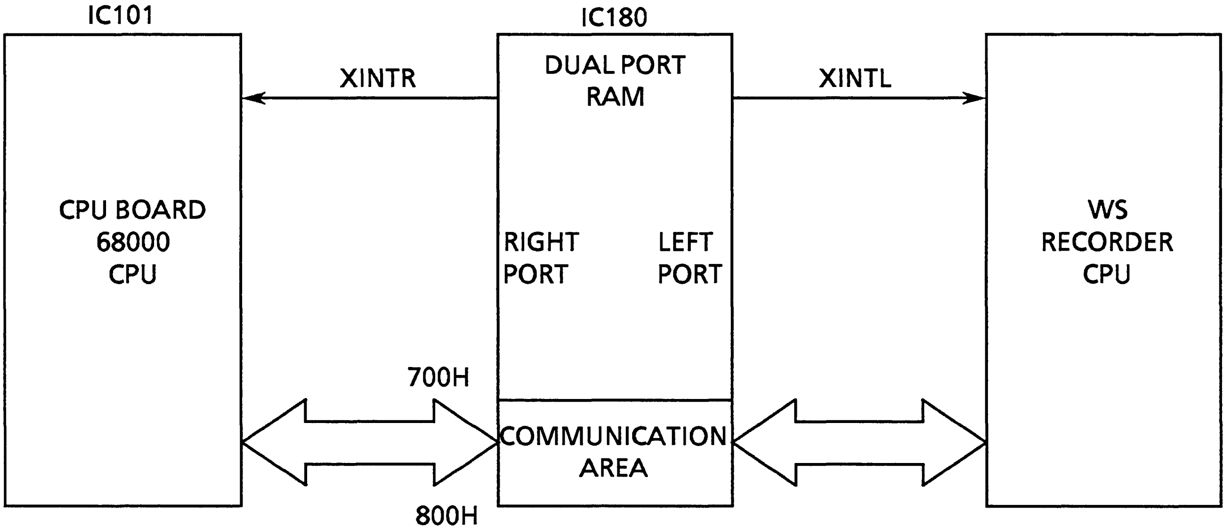
IC174,175 are used as a character generator for WS recorder.

IC176 ~ IC179 are used as a printer buffer for WS recorder.

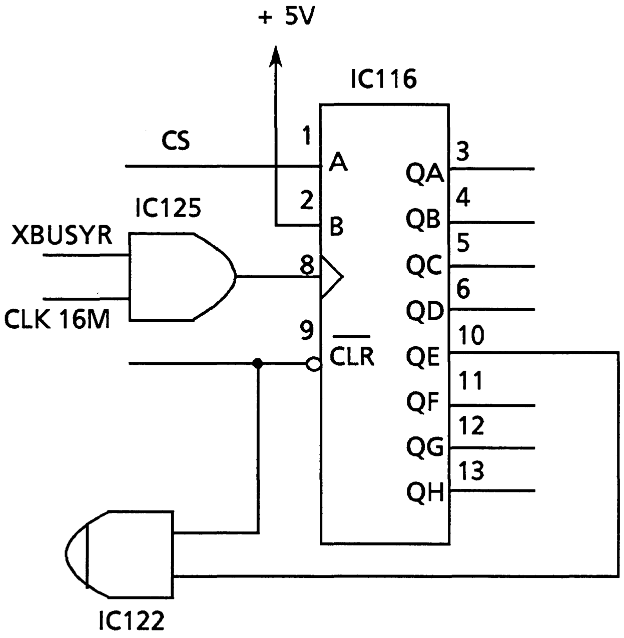
XINT signal is a interrupt signal to CPU on the CPU board and CPU on WS.

For example, when the data is written on address 7FFH of R port of Dual-port RAM from CPU, XINTL is generated.

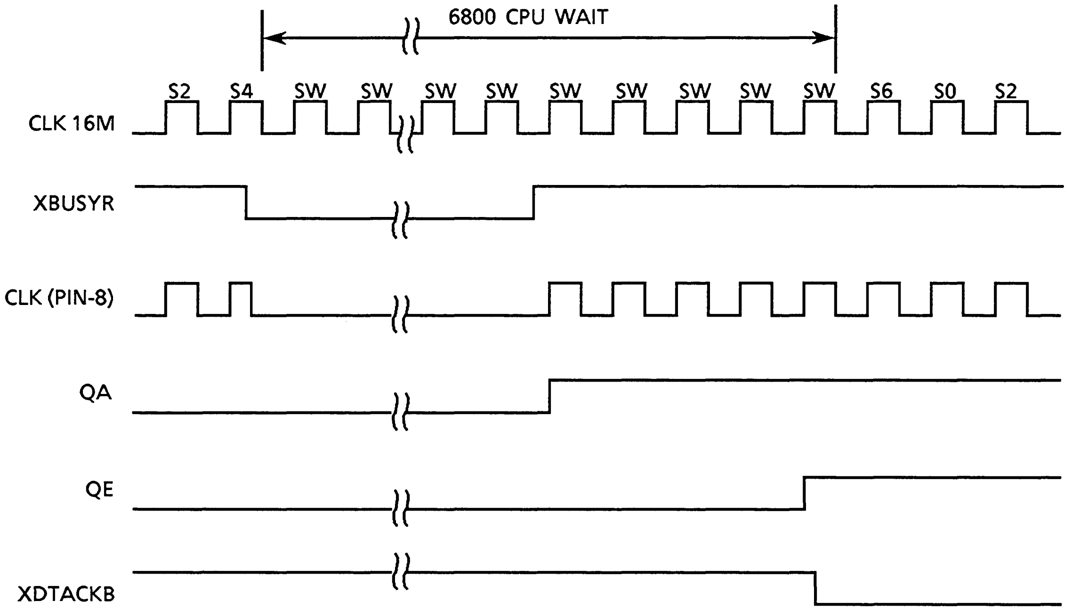
XINTL is used for the direct communication between CPU on the CPU board and WS.


IC101
CPU BOARD
68000
CPU
XINTR
IC180
DUAL PORT
RAM
RIGHT
PORT
LEFT
PORT
700H
COMMUNICATION
AREA
800H
XINTL
WS
RECORDER
CPU

• Access Address Competition Avoidance(XBUSY signal)
On Dual port RAM, when the same address on the both port is accessed by "WRITE" and "READ"signals, the data on "READ" side may be changed during the read cycle.
In order to avoid the above matter, "XBUSY" signal us output from IC180(MB8421).
When the same address is accessed,the latter access signal(from CPU) is rejected and and XBUSY signal is asserted.


+ 5V
IC116
CS
1
A
2
B
IC125
XBUSYR
CLK 16M
8
9
CLR
QA
QB
QC
QD
QE
QF
QG
QH
3
4
5
6
10
11
12
13
IC122

XBUSY Timing Chart

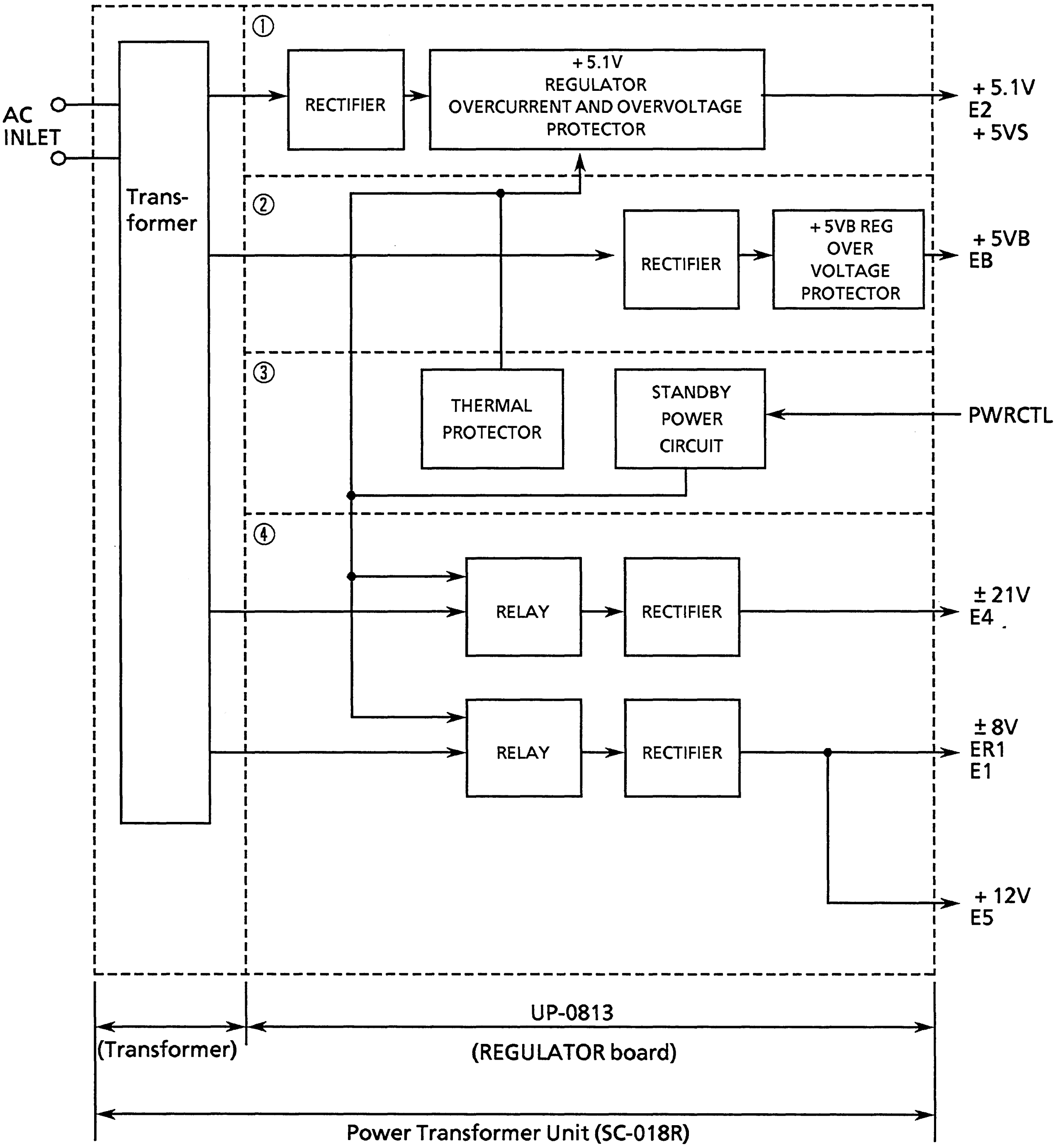

6800 CPU WAIT
S2
S4
SW
SW
SW
SW
SW
SW
SW
SW
SW
S6
S0
S2
CLK 16M
XBUSYR
CLK (PIN-8)
QA
QE
XDTACKB

3-2-2 Power Transformer Unit, SC-018R

The power transformer unit (SC-018R) consists of the transformer and the regulator board.

◆ **General**

Block diagram


AC INLET
Trans-former
①
RECTIFIER
+5.1V REGULATOR OVERCURRENT AND OVERVOLTAGE PROTECTOR
+5.1V
E2
+5VS
②
RECTIFIER
+5VB REG OVER VOLTAGE PROTECTOR
+5VB
EB
③
THERMAL PROTECTOR
STANDBY POWER CIRCUIT
PWRCTL
④
RELAY
RECTIFIER
±21V
E4
RELAY
RECTIFIER
±8V
ER1
E1
+12V
E5
(Transformer)
UP-0813
(REGULATOR board)
Power Transformer Unit (SC-018R)

The regulator consists of the following circuits ;
① +5.1V regulating circuit
② +5VB regulating circuit
③ Overheat protector and standby power circuit (for 5VB)
④ ±21, ±8, ±12V power generating circuit

Each power is processed as follows:

Voltage	Processing Method	Use
+5.1V	Chopper Switching	for digital circuit
+5VB	Dropper	for digital circuit
±21V	Unregulated	for analog circuit
±8V	3 terminal output regulator	for analog circuit
+12V	Unregulated	for fan motor

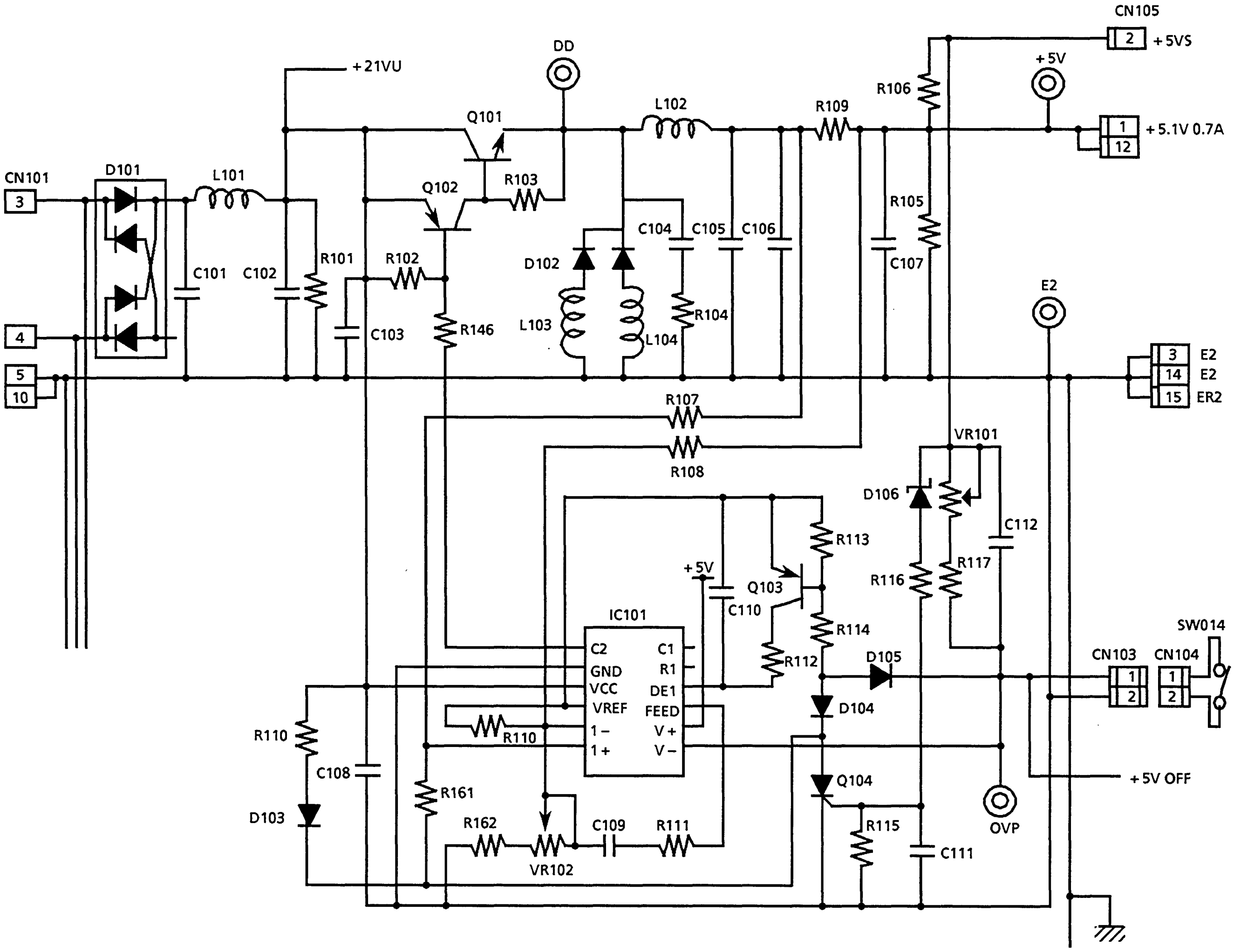
Refer to section 1-9 for the Power System Diagram.

◆ + 5.1V Regulating Circuit

The circuit consists of the rectifier (D111), overvoltage protector, + 5.1V switching regulator with overcurrent protection.

• Overvoltage Protector

The circuit protects all the parts against overvoltage as follows:
When the + 5.1V power supply exceeds + 6V, the Thyristor (Q104) is turned on since a voltage drop across the Zener diode (D106) is more than + 6V of zener voltage. The switching regulator, Q101 is set to off since a heavy current is pulled into the Q104 to stop the + 5V power supply.

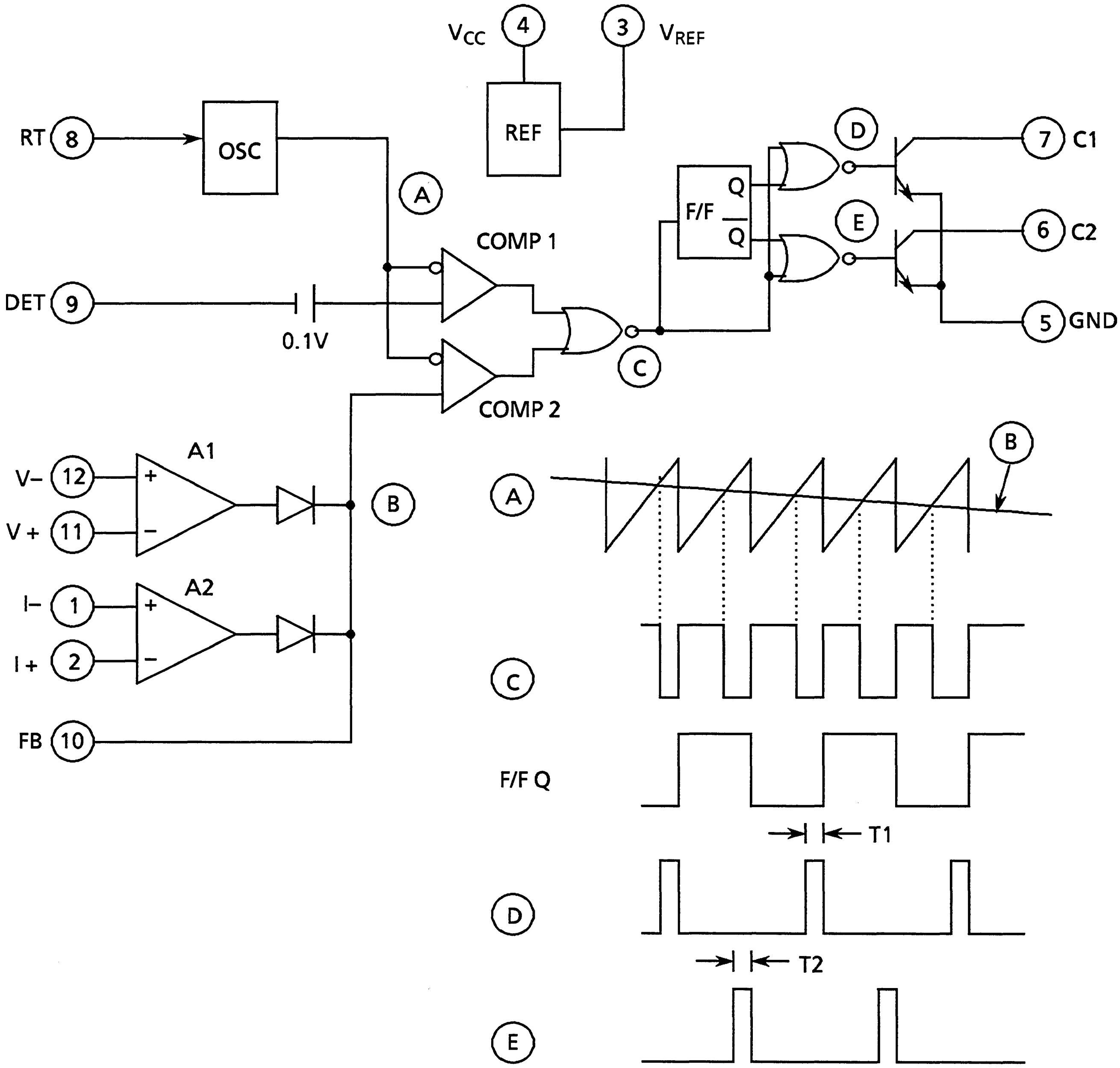

CN105
2
+5VS
DD
+21VU
+5V
R106
L102
R109
Q101
1
12
+5.1V 0.7A
CN101
3
D101
L101
Q102
R103
R105
C104
C105
C106
R101
R102
D102
C101
C102
C107
E2
R104
4
C103
R146
L103
L104
5
10
3
14
15
E2
E2
ER2
R107
R108
VR101
D106
C112
R113
R117
+5V
R116
Q103
C110
IC101
R114
SW014
C2
C1
GND
R1
VCC
DE1
VREF
FEED
1-
V+
1+
V-
R112
D105
CN103
CN104
1
2
1
2
D104
R110
R110
C108
+5V OFF
Q104
R161
D103
R162
C109
R111
R115
C111
OVP
VR102

• +5.1V Switching Regulator with Overcurrent Protection

The circuit generates +5.1V Switching regulated power for the digital circuit with pulse width control.

The pulse width control is executed by SWC-01 (IC101), .

IC101 is a custom hybrid IC composed of a Sawtooth Oscillator (OSC), two Comparators (COMP1 and COMP2), two Amplifiers (A1 and A2), and a +5V Reference Voltage Generator.


VCC
4
3
VREF
REF
RT 8
OSC
A
COMP 1
DET 9
0.1V
COMP 2
C
F/F
Q
Q̄
D
E
7 C1
6 C2
5 GND
V- 12
V+ 11
A1
I- 1
I+ 2
A2
FB 10
B
A
B
C
F/F Q
T1
D
T2
E

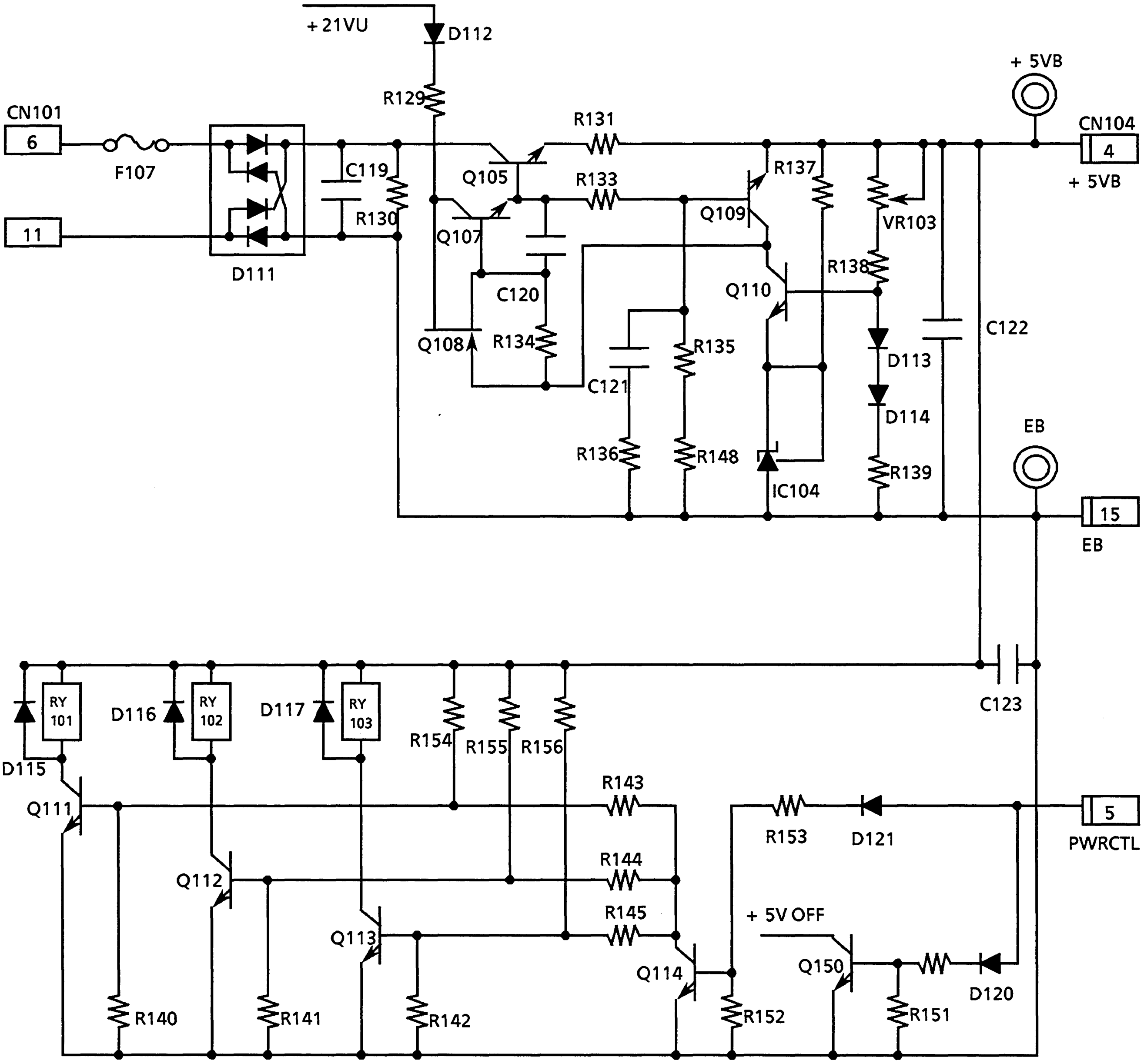
The COMP1 controls the maximum pulse width in low level to obtain the dead time.
The COMP2 controls the pulse width by comparing the output signal from the A1 and A2 with the sawtooth signal from the OSC.
The A1 functions as a feedback amplifier by feeding back +5V Remote Sense Line (5VS).
The A2 functions as an amplifier with overcurrent protection by feeding back the voltage drop across the resistor (R109).

The switching signal from the C2 port of SWC-01, drives Transistors (Q101 & Q102).
The output from the emitter of Q101 is converted to +5V regulated power through the L-C Filter (L102, C105, 106,and 107).

VR101 is an adjustor to set a current value (threshold level) to start the overcurrent protection.
VR102 is an adjustor for the +5.1V regulated power output.

◆ + 5VB Regulating Circuit With Overvoltage Protector

The circuit consists of the rectifier (D111) and a overvoltage Protector. When the +5VB power exceeds +5V, the drop across resistor R131 increases. This switches on the transistor Q109, which in turn, controls the output of the transistor Q105.


+21VU
D112
+ 5VB
R129
CN101
6
11
F107
D111
C119
R130
Q105
Q107
R131
R133
Q109
R137
VR103
CN104
4
+ 5VB
C120
Q108
R134
R138
Q110
C121
R135
D113
D114
C122
EB
R136
R148
IC104
R139
15
EB
C123
RY 101
D115
D116
RY 102
D117
RY 103
R154
R155
R156
Q111
R143
R153
D121
5
PWRCTL
Q112
R144
+ 5V OFF
Q113
R145
Q114
Q150
D120
R140
R141
R142
R152
R151

◆ Overheat Protector & Standby Power Circuit

• Overheat Protector (90°C or more)

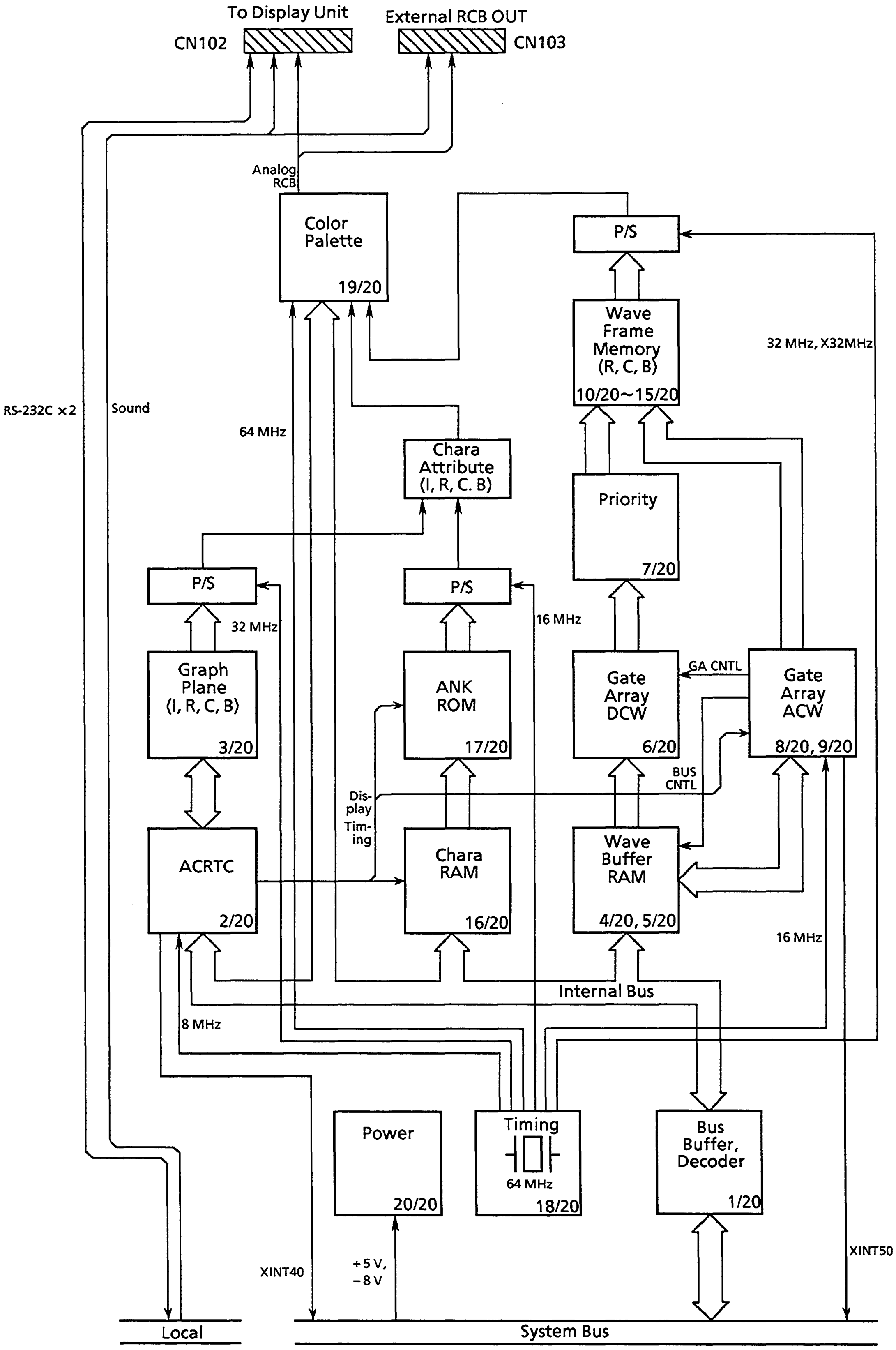
If the main unit warms up to 90°C or more due to a fan motor or other malfunction, the circuit stops the main thermal source, +5.1 V, to protect all the parts against overheating. The thermal switch (SW102) is turned on by overheating (90°C or more) or when the voltage at terminal PWRCTL is +5V. This set the transistor Q101 to off.

• Standby Power

When the voltage at the PWRCTL terminal reads +5 V, the relays RY101 ~ RY103 and transistor Q101 are switched off. This switches off all, except the +5VB power supply

3-2-3 CRTC Board, UP-0795

Block Diagram Description


To Display Unit
External RCB OUT
CN102
CN103
Analog RCB
Color Palette 19/20
P/S
Wave Frame Memory (R, C, B) 10/20~15/20
32 MHz, X32MHz
RS-232C ×2
Sound
64 MHz
Chara Attribute (I, R, C. B)
Priority 7/20
P/S
32 MHz
P/S
16 MHz
Graph Plane (I, R, C, B) 3/20
ANK ROM 17/20
Gate Array DCW 6/20
GA CNTL
Gate Array ACW 8/20, 9/20
BUS CNTL
Dis-play Tim-ing
ACRTC 2/20
Chara RAM 16/20
Wave Buffer RAM 4/20, 5/20
16 MHz
Internal Bus
8 MHz
Power 20/20
Timing 64 MHz 18/20
Bus Buffer, Decoder 1/20
XINT40
+5 V, −8 V
XINT50
Local
System Bus

◆ General

The CRTC board consists of the following circuits.

1) Bus Buffer Decoder Circuit
   This circuit provides the buffer for the system bus as well as generates the bus control signals.

2) Timing Circuit
   The various clock signals used in the CRTC board are derived from a 64MHz oscillator located on this board.

3) ACRTC
   The ACRTC 63484 controls the display timing, and outputs the graphic display control signals to the GRAPHIC RAM.

4) Graph Plane
   The graph plane is used to display up to 4 parameter graphs on the display unit.

5) Character RAM
   This dual-port character RAM contains the character code.

6) Foreign Character ROM and Japanese Character ROM
   There are two character ROMs; one Foreign character ROM and one Japanese character ROM.

7) Wave Buffer RAM
   This RAM stores the waveform data from the CPU board, and the gate array setting data. When the gate array is being accessed, the RAM negates it bus lines to the CPU board.

8) DCW Gate Array
   This circuit interpolates the waveform data before transferring it to the priority circuit.

9) ACW Gate Array
   This controls wave buffer RAM, DCW gate array, and frame memory.

10) Priority Circuit
    This circuit designates the priority level to the various parts of the waveform according to their importance.

11) Wave Frame Memory
    This stores the waveform display data.

12) Parallel/Serial
This shift register converts the parallel video signal to serial video signal.

13) Character Attribute
This supply the display attribute data for the character video signal.

14) Color Palette
The color setting on this circuit is controlled by the CPU board. Then, this circuit adds the color palette code to the video signals to form the R, G, B signals.

◆ Bus Buffer and Decoder Circuit

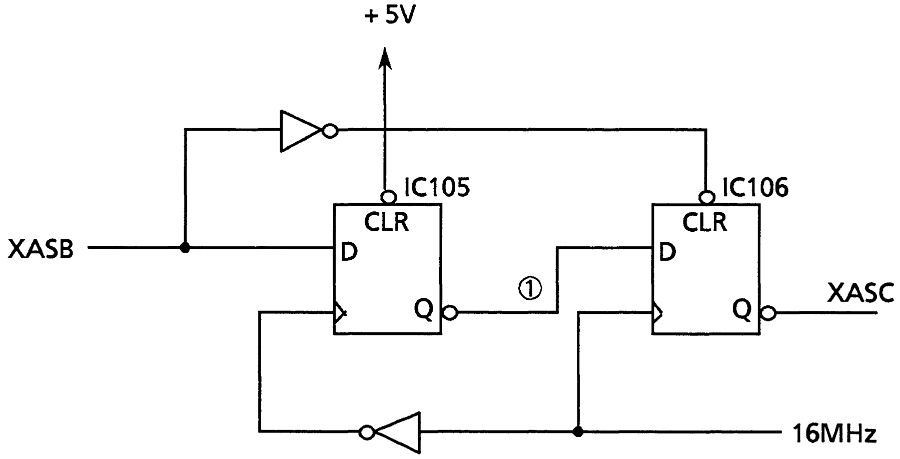
● Data Bus

IC101 and 102 control the input and output of the data according to the commands set by the decoder circuit.

● Address Bus

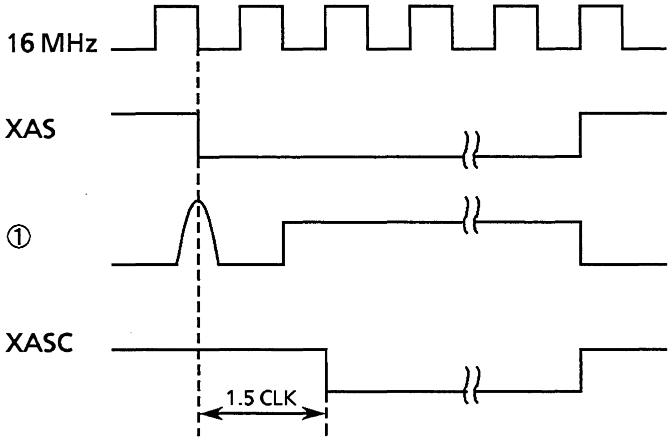
IC103 and 104 is the address bus buffer for waveform data and character data, A1 ~ A16. The address bus A17 ~ A23 go directly to the decoder circuit.

● Control Signal (XAS, XUDS, XLDS, and R/XW)



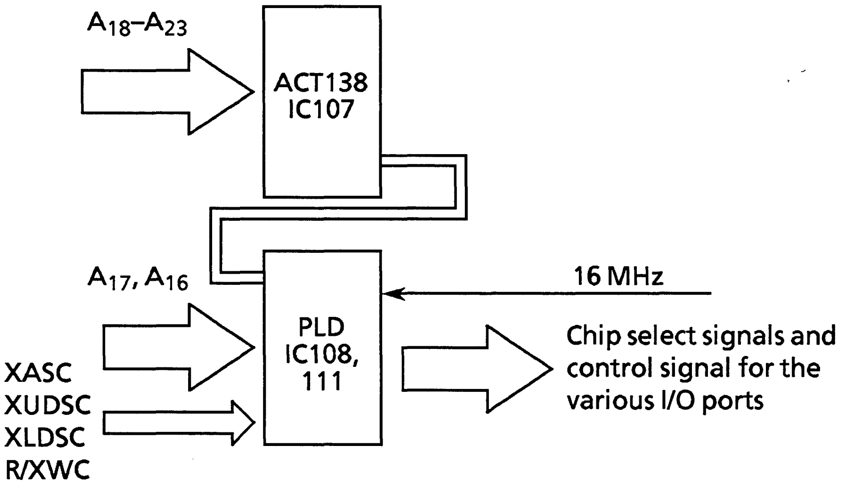
This circuit latches the 16MHz internal clock. The address strobe (XASC) is delayed by 1.5 clock to avoid the metastable condition. The XAS is used to reset the address strobe signal.

The timing chart below shows how the XASC signal is delayed by 1.5 clock.


16 MHz
XAS
①
XASC
1.5 CLK

• Decoder

The IC107, 108 and 111 decodes the address bus A17 ~ A23, and generates the chip select signal and controls signals for the various I/O ports.


A18-A23
ACT138
IC107
A17, A16
XASC
XUDSC
XLDSC
R/XWC
PLD
IC108,
111
16 MHz
Chip select signals and
control signal for the
various I/O ports

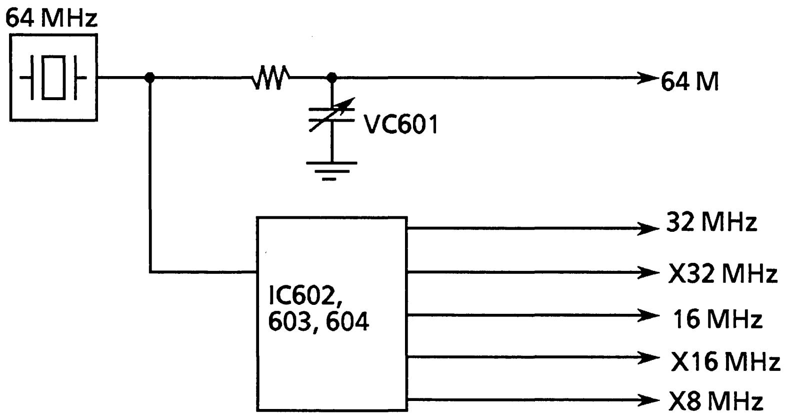
• Data Acknowledge and Interrupt

This circuit informs the CPU when the waveform RAM, ACRTC, CHARA RAM, COLOR PALETTE, AND I/O PORT are accessed. The acknowledge signals passed through a a wired OR circuit (IC109) and outputted as XDTACK signal.

The IC705 separates the interrupt signal from the ACRTC and ACW into the XINT40 and XINT50 signals and outputs them to the CPU.

◆ Timing Generator Circuit

This circuit generates from the 16 MHz system clock the following timing:
* 32 MHz for the waveform display circuit and the graphic display circuit.
* X32 MHz for the waveform display circuit and the graphic display circuit.
* 16 MHz for the waveform display circuit and the character display circuit.
* X16 MHz for the waveform display circuit and the character display circuit.
* X8 MHz for the ARCTC


64 MHz
64 M
VC601
IC602, 603, 604
32 MHz
X32 MHz
16 MHz
X16 MHz
X8 MHz

The VC601 is used for adjusting the latching timing for the waveform, character, and graphic video signals.

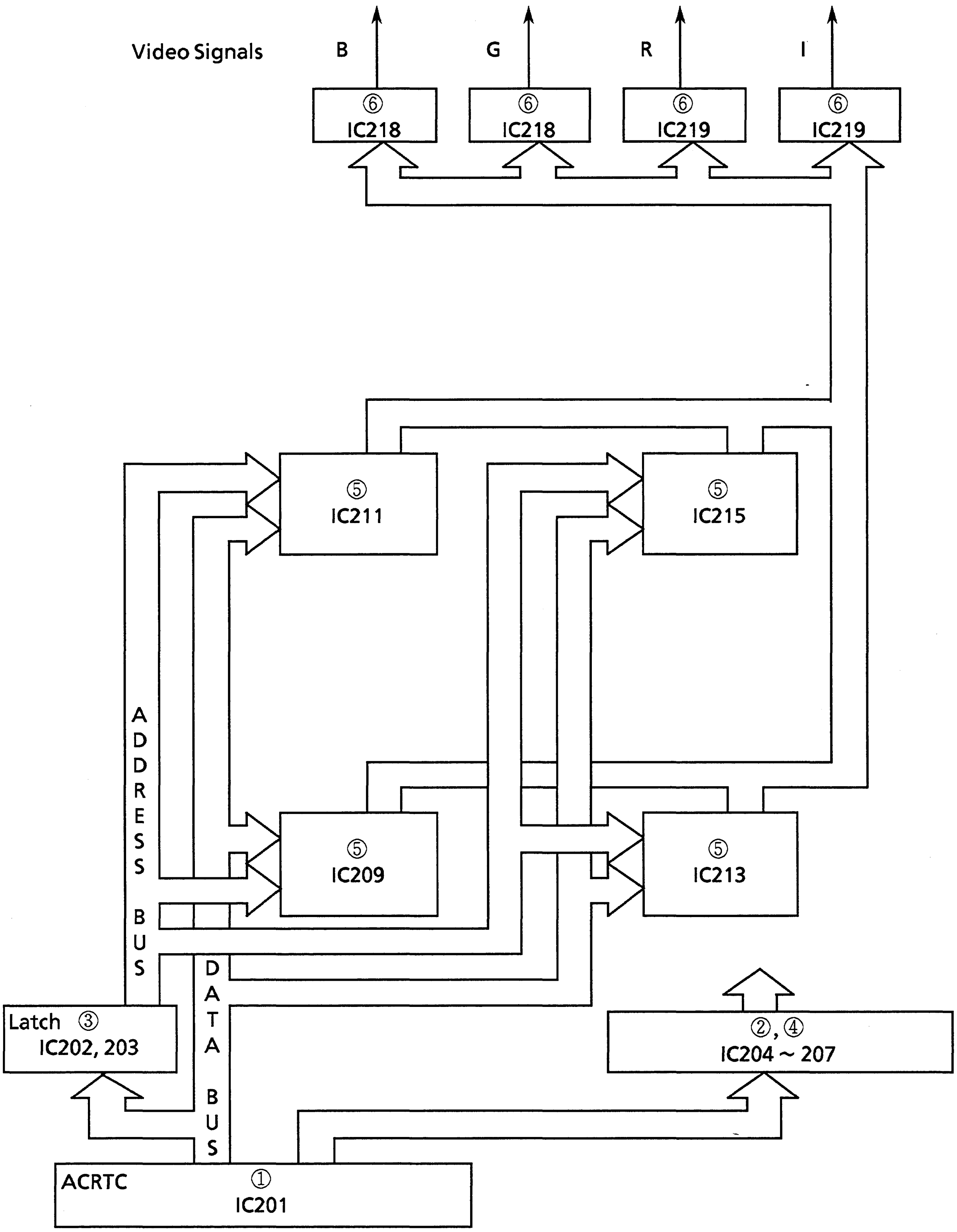
◆ Graphic Display Circuit

This circuit is controlled by the HD63484 ACRTC (Advanced CRT Controller). This controller generates the various timings needed by the CRT unit. It also allows the CPU to access the bitmap memory. The bitmap consist of eight 1M bit multi-port video RAM.

The display screen is made up of 1024 dots on the horizontal plane and 800 lines on the vertical plane.

The bitmap memory consist of 4 planes, that is, I, R, G, and B. This provides a possibility of 16 colors.

● Graphic Display Block Description


Video Signals
B
G
R
I
⑥ IC218
⑥ IC218
⑥ IC219
⑥ IC219
⑤ IC211
⑤ IC215
⑤ IC209
⑤ IC213
ADDRESS BUS
DATA BUS
Latch ③ IC202, 203
②, ④ IC204 ~ 207
ACRTC ① IC201

1) ACRTC (IC201)
   This circuit is control by the CPU. It generates the timing signals for the CRT. It also sends the graphic images to the frame buffer.

2) Multi-port video DRAM Control Circuit (IC204 ~ 207)
   This circuit controls the interface between the ACRTC and the multi-port video DRAM, by providing the timing signals, XCAS and XRAS, and the multi-port DRAM read and write signal.

3) Address Latch and Multiplexer (IC202 and 203)
   This unit modifies the address or data signals from the ACRTC for the multi-port video DRAM.

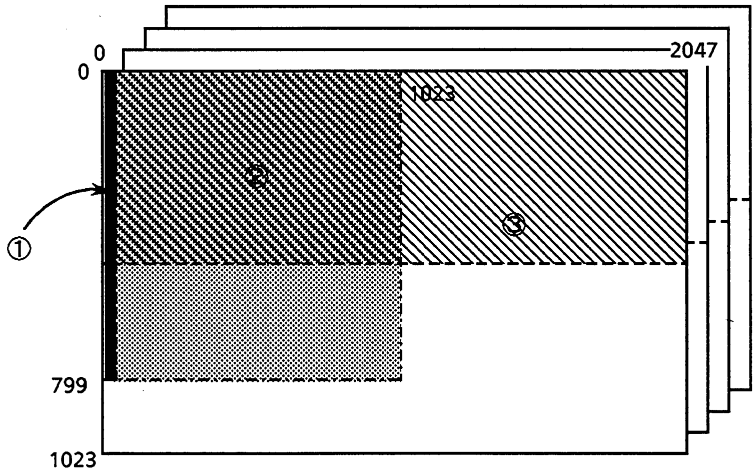
4) SAM Port Control IC218
   This IC218 controls the data input and output of the multi-port video DRAMs.

5) Graphic RAM
   There are eight 2M bit multi-port video DRAM (IC209, 211, 213, 215). The 4 planes on these multi-port video DRAMs make it possible to display up to 16 colors.

6) Shift Register
   The 4 bit shift register latches the parallel data from the SAM port of the multi-port DRAM and converts them into serial data.

● Graphic RAM Memory Area

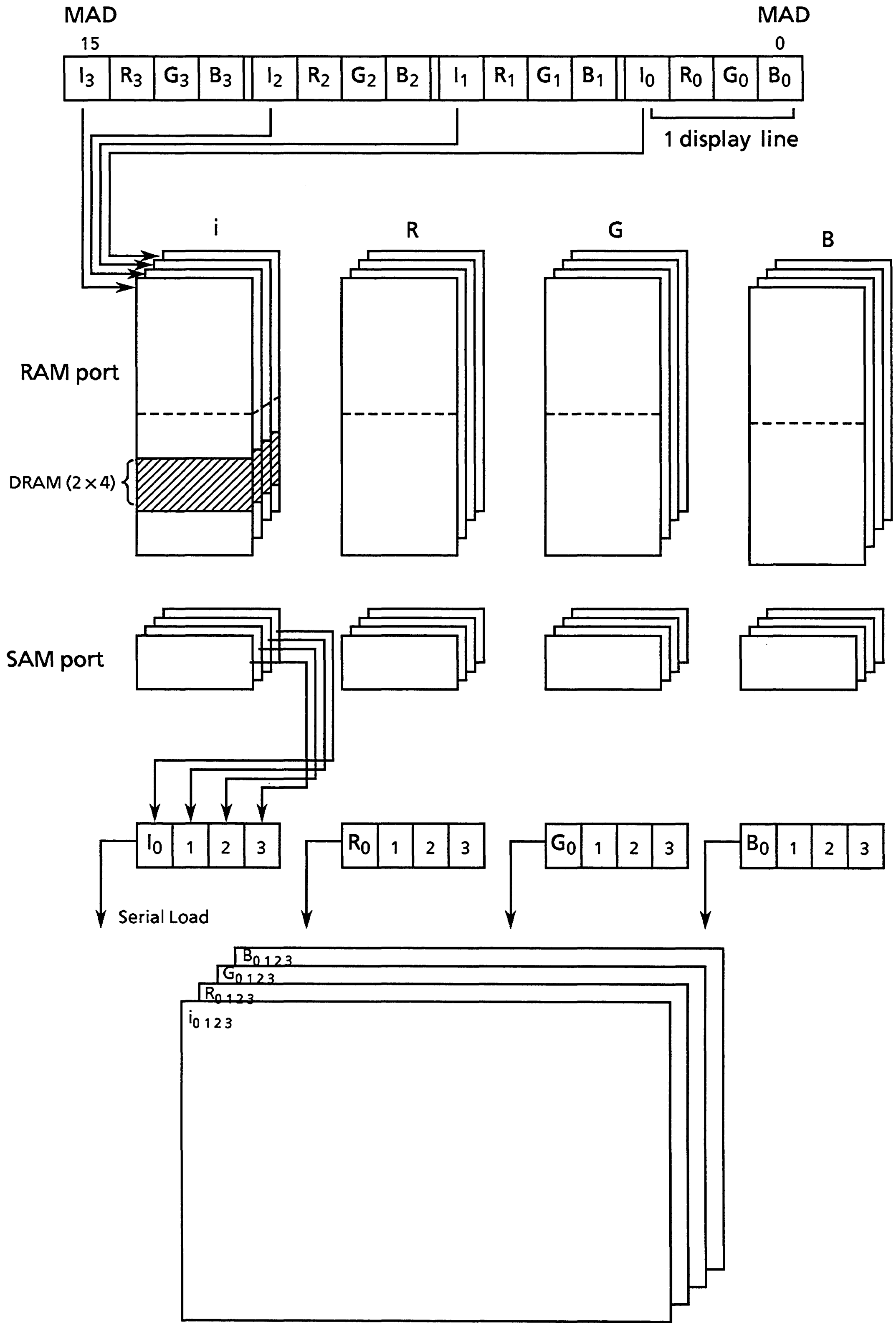
The graphic RAM is based on a multi-port DRAM, where in 1 memory cycle it can read out 2048 data. This is more than it actually needed: the actual memory area of the graphic RAM that is used is shown below.



① Memory area for ACRTC setting information
② Actual memory area used
③ The graphic RAM memory area.

● Color Processing

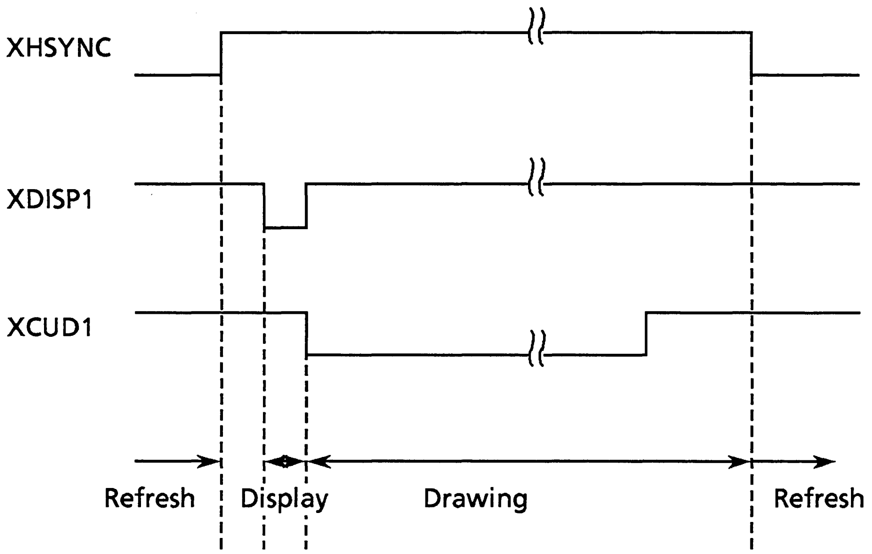
The graphic RAM reads the 16 bit data from the ACRTC. However, the main circuit consists of 4 bit per scanning line. The illustration below shows the composition of a one word data.


MAD 15
MAD 0
I3 R3 G3 B3 I2 R2 G2 B2 I1 R1 G1 B1 I0 R0 G0 B0
1 display line
i
R
G
B
RAM port
DRAM (2 x 4)
SAM port
I0 1 2 3
R0 1 2 3
G0 1 2 3
B0 1 2 3
Serial Load
B0 1 2 3
G0 1 2 3
R0 1 2 3
i0 1 2 3

• Drawing and Displaying

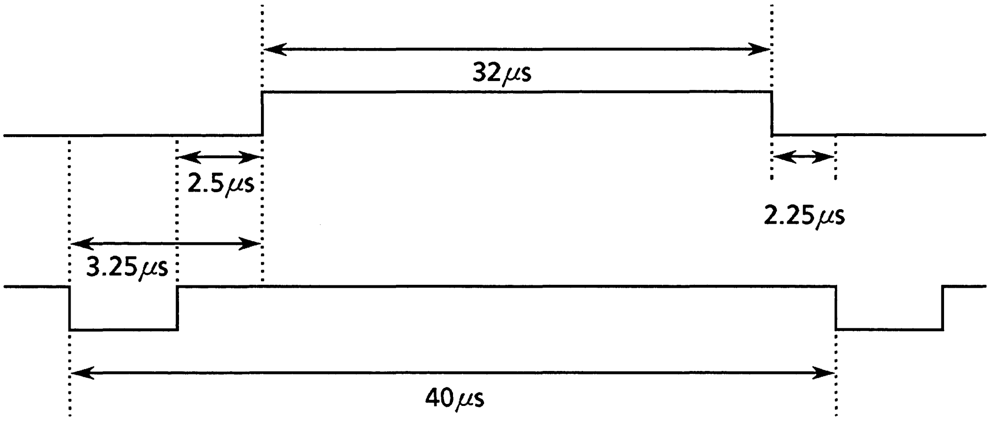
The timings used for drawing on the memory area and reading the drawn data for display are controlled by software settings. In one memory cycle, graphic data are written into the memory and the drawn data in the memory are read out simultaneously. The IC204 and 205 supply the control signals, XRAS, XCAS, XOE, and XWE.

• Drawing and Displaying Timing Chart

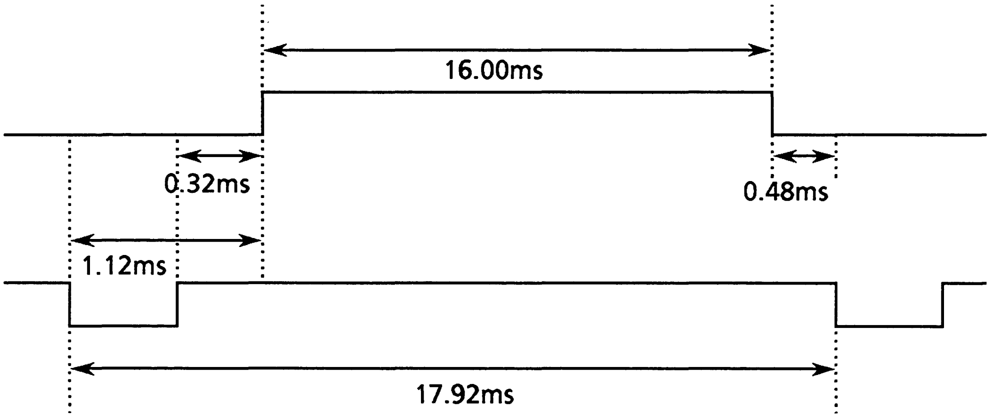

XHSYNC
XDISP1
XCUD1
Refresh
Display
Drawing
Refresh

• Graphic Display Timing

* Horizontal Synchronizing Period

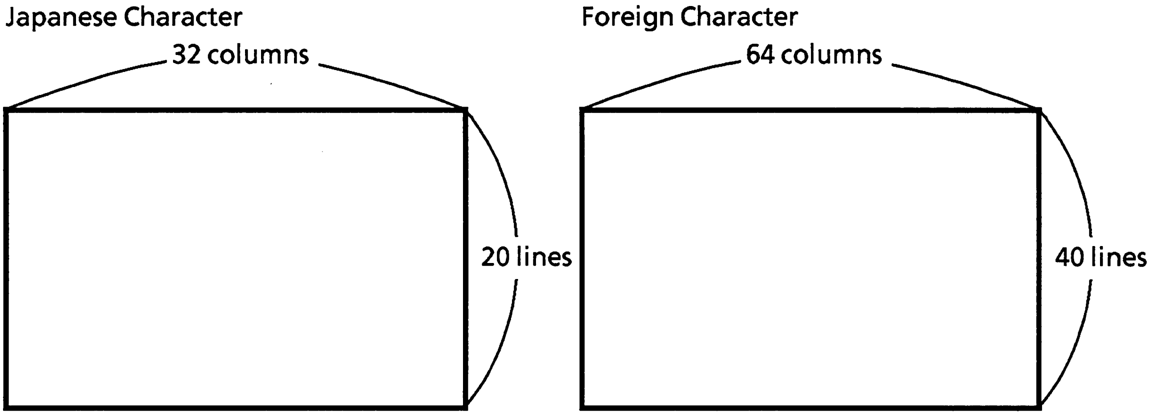

32μs
2.5μs
2.25μs
3.25μs
40μs

* Vertical Synchronizing Period


16.00ms
0.32ms
0.48ms
1.12ms
17.92ms

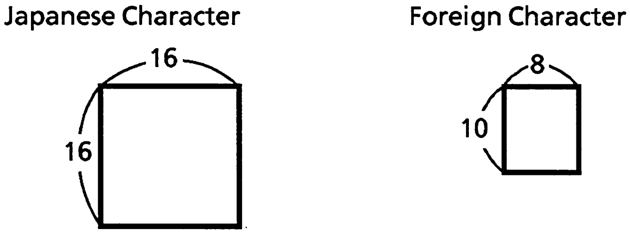
◆ Character Display Circuit

To understand the design of this circuit, a brief description of the construction of the character in the screen display is required. The character display screen for both the foreign character ROM and Japanese character ROM are shown below.



● 1 Character (Dot) Data

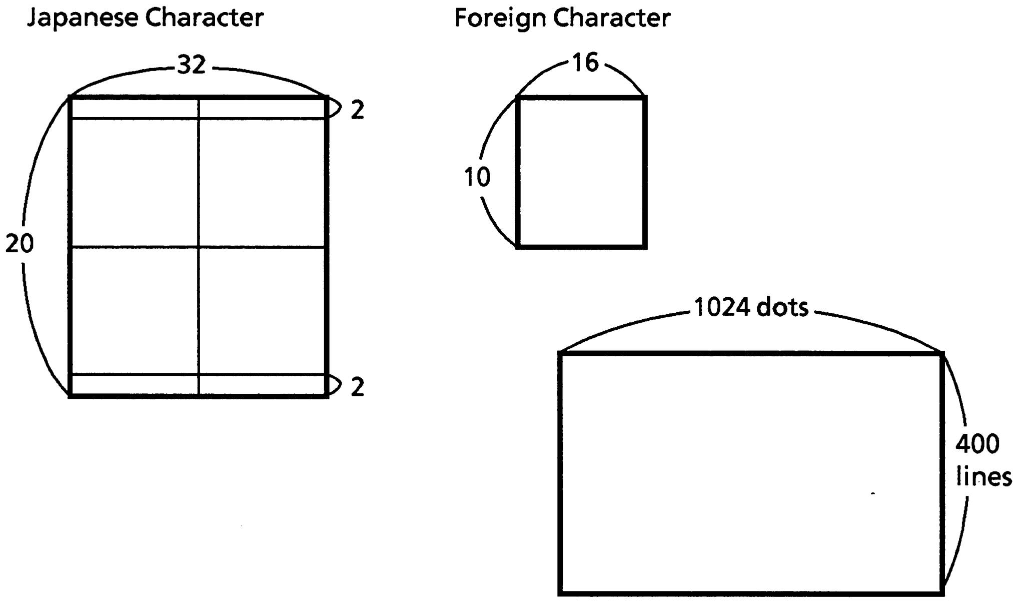
1 character (dot) data occupies 1 column and 1 line unit space on the screen.
The character (dot) data of the Japanese character (16 × 16 dots) and the foreign character (8 × 10 dots) are different. The illustration below shows the configuration of the two types of character.



In the interlace scanning method used in this system, the character data is scanned twice on the screen. This causes the character to double in sized along the vertical plane. To cancel out this elongation effect along the vertical plane, the character data is double read along the horizontal plane. This means the 1 character (dot) data doubles the number of its horizontal dots but the number of its vertical dots stay the same.

Next,the displayed Japanese character (dot) data is modified to fit 4 displayed foreign character (dot) data. Hence 1 displayed Japanese character (dot) data contains 32 × 20 dots, and consequently the display screen now contains 1024 × 400 dots. The smallest unit of character (dot) data consist of 8 × 10 dots.

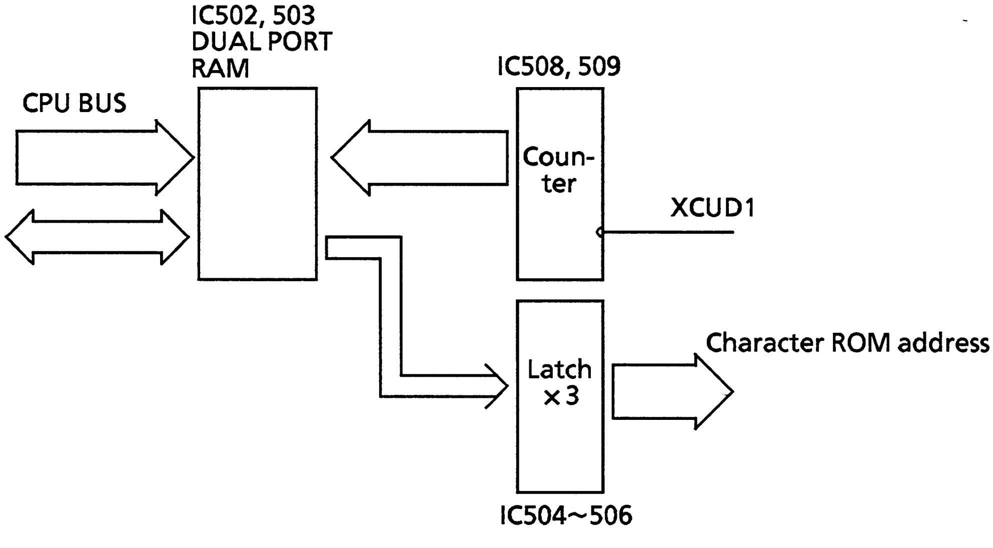
Displayed Japanese Character (Dot) Modification


Japanese Character
32
2
20
2
Foreign Character
16
10
1024 dots
400 lines

The 8 × 10 dots character (dot) data is related to one code data in the character ROM. One code data contains 24 bits (3 Bytes) of information – 2 × 8 bits of character code for the character ROM and 8 bits of attribute data of the character code.

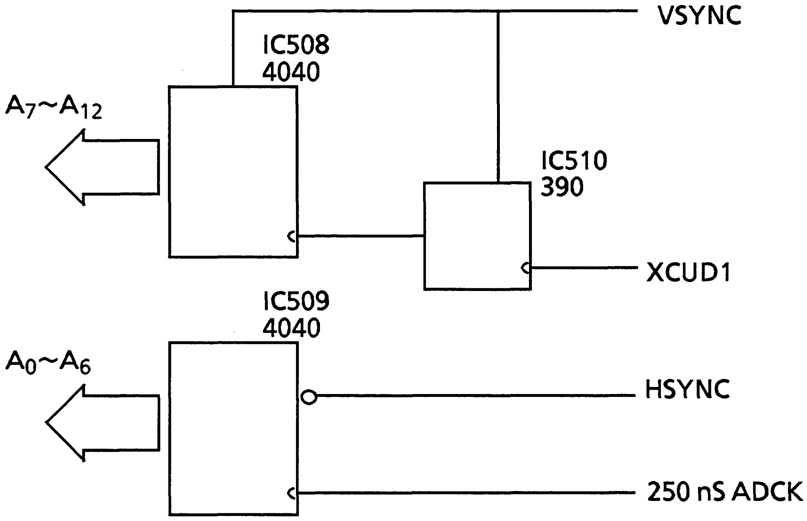
The horizontal 16 bits are read out together, hence 1 cycle takes about 500 nsec. In the cycle, the data are double read – one for the character code and one for the attribute code.

- **Character ROM**


IC502, 503
DUAL PORT
RAM
CPU BUS
IC508, 509
Coun-
ter
XCUD1
Latch
×3
Character ROM address
IC504~506

The counters IC508 and 509 generate an address for display on the display unit.
The address specifies a character code on the Character ROM. The character code and its attribute code are outputted to the character ROM IC511.

• Character Code Address Generator

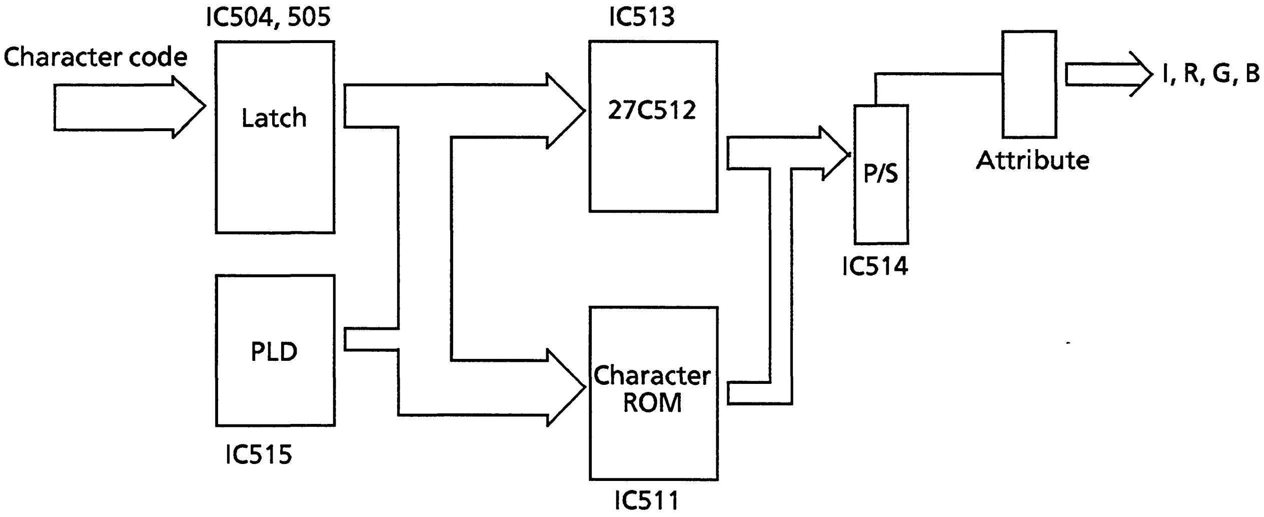

VSYNC
IC508
4040
A7~A12
IC510
390
XCUD1
IC509
4040
A0~A6
HSYNC
250 nS ADCK

The character code addresses A0 ~ A6 are read out every 250 nsec. For every 128 times the data are read out, the XHSYNC signal reset the circuit.

The character code addresses A7 ~ A12 are read out according to display timing 1 (XCUD1). For every ten times the data are read out, the VHSYNC signal reset the circuit.

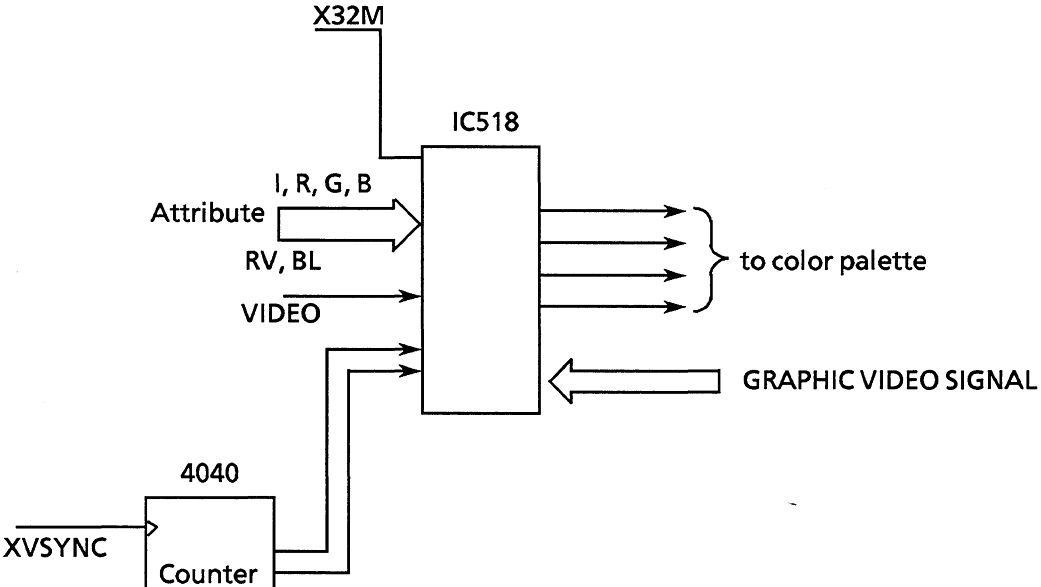
• Character ROM

The character ROM reads out the character video signals according to the address given by the character code address. The character video signals are converted into 8 bit serial data before being sent to the character attribute circuit.


IC504, 505
Character code
Latch
PLD
IC515
IC513
27C512
Character ROM
IC511
P/S
IC514
Attribute
I, R, G, B

• Character Attribute

The IC518 converts the video signals (character and graphic) according to their attribute signals. The converted video signals now not only consist of the information for the video image, but also, its color.


X32M
IC518
I, R, G, B
Attribute
RV, BL
VIDEO
to color palette
GRAPHIC VIDEO SIGNAL
4040
XVSYNC
Counter

◆ Waveform Display Circuit

The functions of this waveform display circuit:

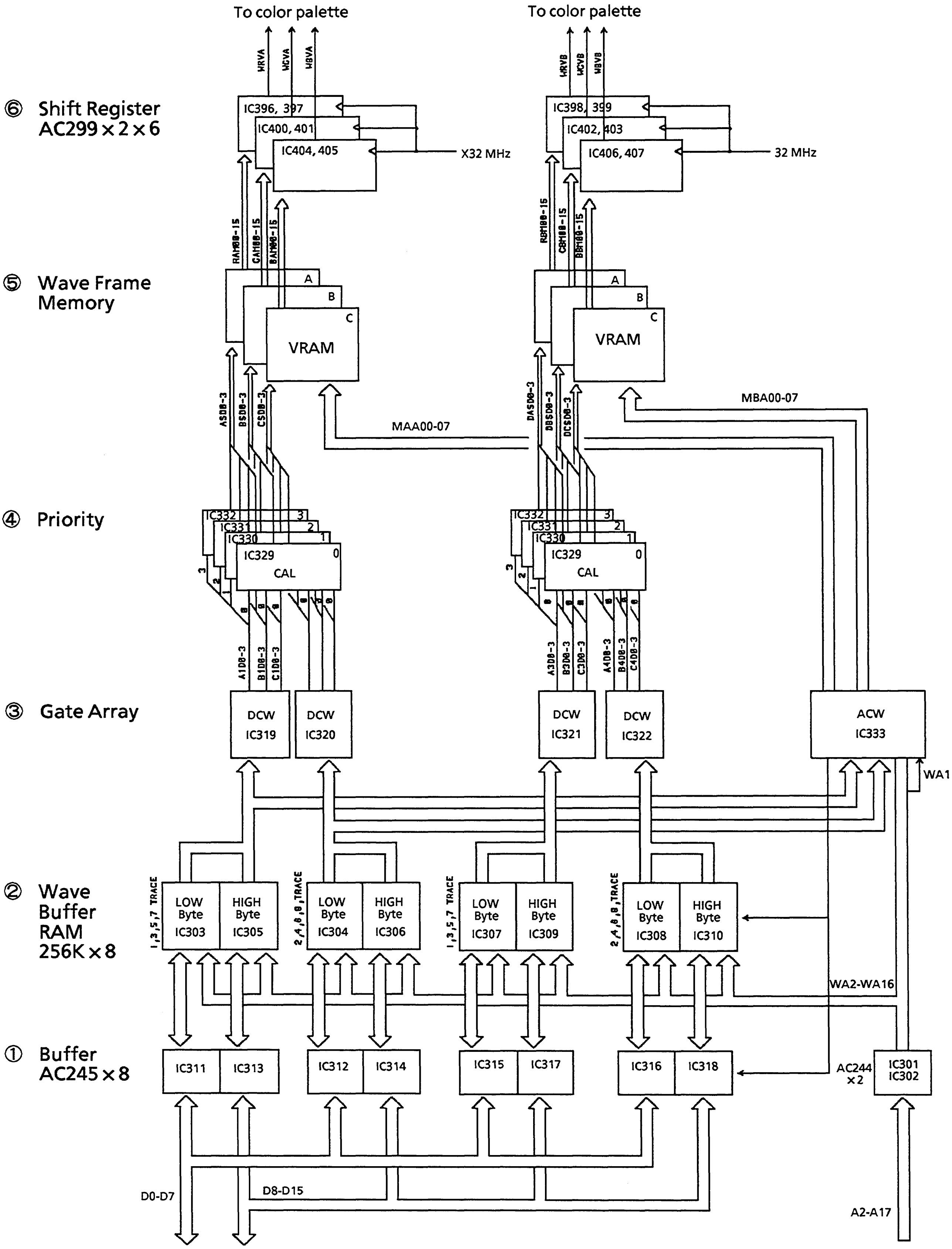
1) To display up to 8 colored waveform traces.
2) To make the waveform trace sweep across the screen.
3) To freeze the waveform trace on the screen.
4) To switch on/off the waveform trace/s on the screen.
5) To allow changeable assignment of colors to the waveform traces.

2K Word (16 bits) of waveform information is required to draw one waveform trace. This 2K Word waveform information is read out from the CPU. The frame gate array in this display unit gates the one frame waveform data into 3 bitmap memory according to the timing provided by the ACRTC.

The 2048 dots × 800 lines screen is divided into the even field and the odd field for waveform display.

The slave video controller (ACW) only controls the processing on the waveform display circuit under the direction of the master video controller (ACRTC).

• Waveform Display Block Diagram


⑥ Shift Register AC299 × 2 × 6
⑤ Wave Frame Memory
④ Priority
③ Gate Array
② Wave Buffer RAM 256K × 8
① Buffer AC245 × 8
To color palette
WRVA
WGVA
WBVA
To color palette
WRVB
WGVB
WBVB
IC396, 397
IC400, 401
IC404, 405
X32 MHz
IC398, 399
IC402, 403
IC406, 407
32 MHz
RAM00-15
GAM00-15
BAM00-15
RBM00-15
CBM00-15
BBM00-15
A
B
C
VRAM
A
B
C
VRAM
ASD0-3
BSD0-3
CSD0-3
MAA00-07
DASD0-3
DBSD0-3
DCSD0-3
MBA00-07
IC332
IC331
IC330
IC329
CAL
3
2
1
0
IC332
IC331
IC330
IC329
CAL
3
2
1
0
A1D0-3
B1D0-3
C1D0-3
A3D0-3
B3D0-3
C3D0-3
A4D0-3
B4D0-3
C4D0-3
DCW IC319
DCW IC320
DCW IC321
DCW IC322
ACW IC333
WA1
1,3,5,7 TRACE
LOW Byte IC303
HIGH Byte IC305
2,4,6,8,TRACE
LOW Byte IC304
HIGH Byte IC306
1,3,5,7 TRACE
LOW Byte IC307
HIGH Byte IC309
2,4,6,8,TRACE
LOW Byte IC308
HIGH Byte IC310
WA2-WA16
IC311
IC313
IC312
IC314
IC315
IC317
IC316
IC318
AC244 ×2
IC301 IC302
D0-D7
D8-D15
A2-A17

The waveform display circuit consists of the following units:

1) Buffer
This is a two way communication buffer. However, when the data in the WAVE RAM is read out to the gate array, the buffer inhibit the bus line to and from the CPU.

2) WAVE RAM (Waveform Buffer RAM)
The 8 WAVE RAMs are grouped in blocks of two. Two blocks of WAVE RAMs are grouped for the waveform traces 1, 3, 5, and 7. The remaining two blocks of WAVE RAMs are grouped for waveform traces 2, 4, 6, and 8. In this design, the resulting video signals from these two grouped blocks are superimposed on each other with a half clock timing difference. The horizontal resolution is doubled by this half clock timing difference during superimposing.

3) ACW and DCW
The ACW (slave video controller) has two functions:
* Controls the bitmap memory with the timing received from the ACRTC of the graphic display unit.
* Controls the communication bus lines for the CPU and the gate array DCW.

The gate Array DCW
One gate array DCW served 4 waveform traces data.

4) Priority Level Circuit
When two or more waveforms are superimposed on one another there is a tendency for the colors of the waveforms to mix and form another color. This circuit prevents this effect from happening by adding a priority level code onto the waveform data.

5) Bitmap Memory
These are two 3 plane bitmap memory. The priority level coded serial waveform data are inputted into the bitmap memory dual port RAM through the SAM ports. The bitmap memory dual port RAM reads out the parallel data according to the control signals from the ACW.

6) Shift Register
The waveform display resolution is twice of that the character or graphic display resolution, however, the illuminating time is halved. On the screen, the character or graphic display appears brighter than the waveform display. To counter this effect, the brightness signal to the waveform display unit is doubled.

◆ WAVE RAM (Waveform Buffer RAM)

The function of the WAVE RAM (IC303 ~ 310) is to improve the horizontal resolution of the 6 to 8 waveform traces display.

The waveform data read out from the WAVE RAM served two function:
a) used as a command signal by ACW.
b) used as a data signal by gate array DCW.

The IC301 and 302 controls the waveform RAM address bus lines WA1 ~ WA16 according to the command of the CPU. However, when the gate array access them, the IC301 and 302 are inhibited by the

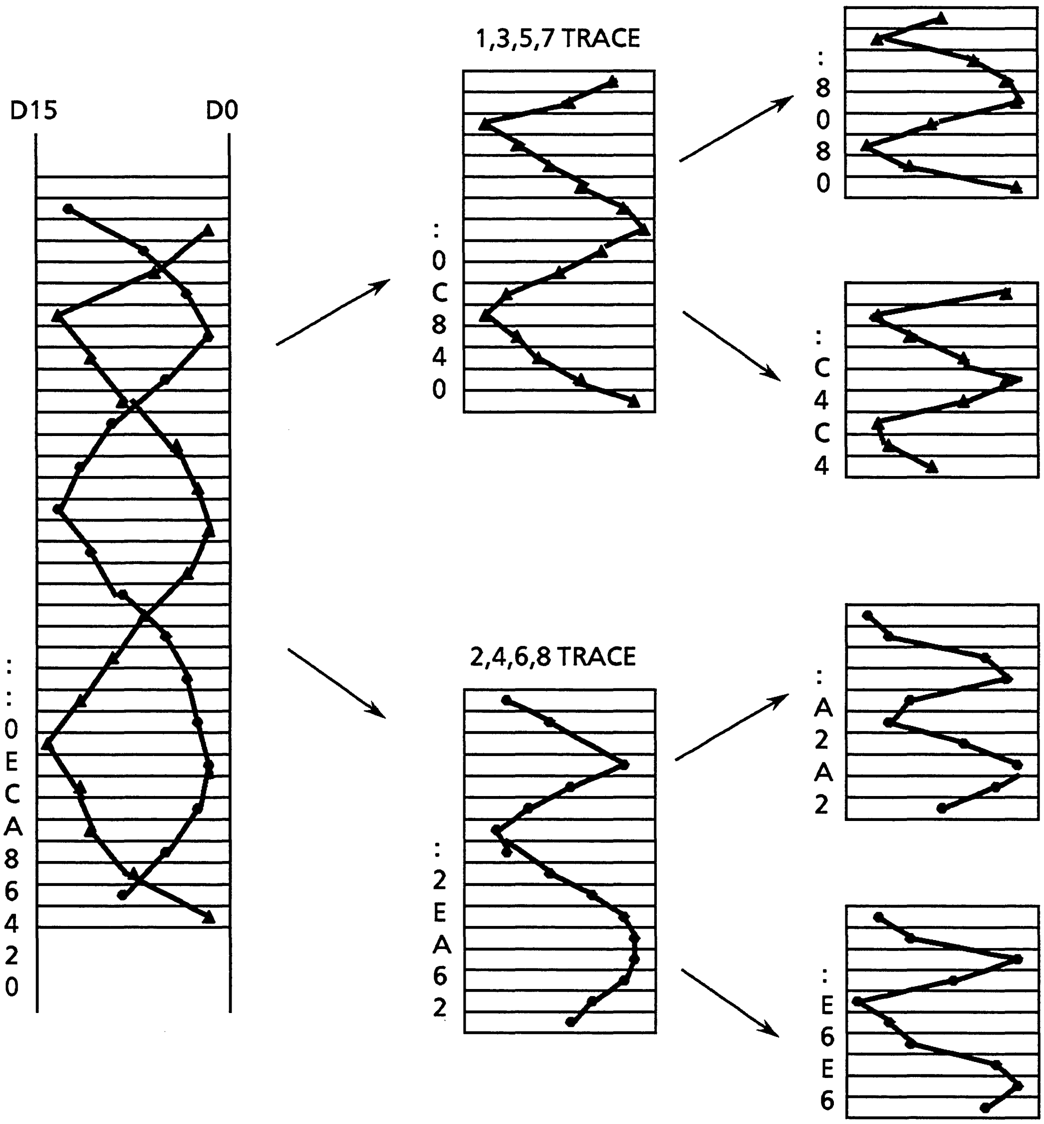
The IC301 and 302 controls the waveform RAM address bus lines WA1 ~ WA16 between the internal bus and the CPU bus according to the command given by the CPU. However, when the ACW access the waveform RAM address lines, the communication bus lines between the internal bus and the CPU bus are inhibited. The BCONT (bus control) signal from the ACW inhibit the above communication. When both the CPU and ACW access the waveform RAM address bus lines together, the ACW delays its waveform data acknowledge signal (XGDTACK) to the CPU. This causes the CPU to hold the address and allow the ACW to finish accessing the waveform RAM bus address lines.

The CPU address line A2 directs the ACW to separate the 4 blocks of two WAVE RAM into two groups of two blocks each. The IC337 and 338 further separates the two blocks of WAVE RAM according to the CPU address line A1 and A2.

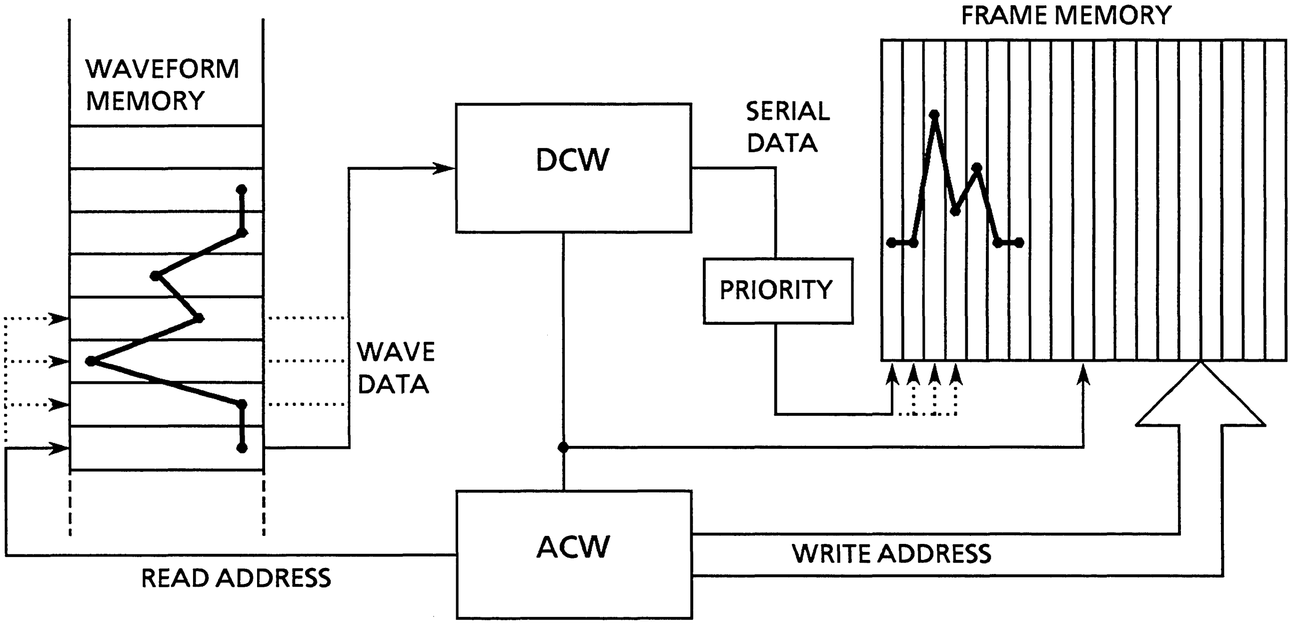
The table below shows the composition of the waveform RAM bitmap memory.

A2, A1	D15	D0	
0, 0	IC303	IC305	1, 3, 5, 7 trace
0,1	IC304	IC306	2, 4, 6, 8 trace
1, 0	IC307	IC309	1, 3, 5, 7 trace
1, 1	IC308	IC310	2, 4, 6, 8 trace
0, 0	IC303	IC305	.
0, 1	IC304	IC306	. .
	. . .	. . .	. . . . .

The illustration below shows how the 8 waveform traces are separated.


D15
D0
:
:
0
E
C
A
8
6
4
2
0
1,3,5,7 TRACE
:
0
C
8
4
0
2,4,6,8 TRACE
:
2
E
A
6
2
:
8
0
8
0
:
C
4
C
4
:
A
2
A
2
:
E
6
E
6

◆ Waveform Processing Circuit



The function of this circuit is to draw the waveform trace on the frame memory with the interpolated waveform data it received from the DCWs (IC319 ~ 322).

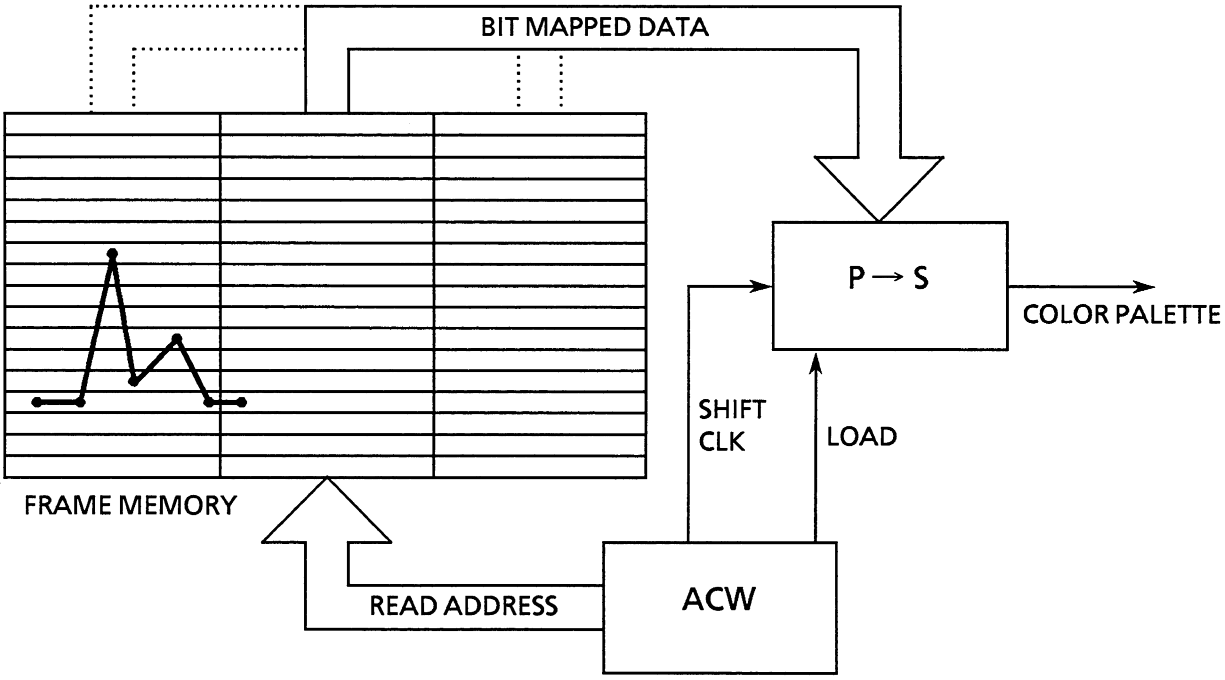
When the DSLD port of the ACW is negated, the ACW reads out the address to the buffer RAMs, IC303 ~ 306. The buffer RAMs then load out the waveform data and the DCW latch this waveform data. The latching timing LCK is provided by the ACW. Before the DSLD port of the ACW is negated again to to load the next batch of waveform data into the DCWs, the DCWs interpolates the waveform data by shifting the waveform data. The shifting timing, SCLK, is again provided by ACW. These shifted data, A1SD0 ~ 3, ...C4SD0 ~ 3, are then outputted to the priority circuit.

At a later stage the shifted data are color palette coded. Up to 7 different colors (represented by bits 0,0,1 to 1,1,1) can be coded onto the shifted data.
These color code can give each individual waveform trace a different color.
However, when these different colored waveform traces overlap each other, a color other than those of the overlapping waveform traces occurs. For example, when a green (0,0,1) waveform trace overlaps a red (0,1,0) waveform trace, the overlapping point will have a different color code (0,1,1). To prevent this from occurring, the priority code is first added to the shifted data.

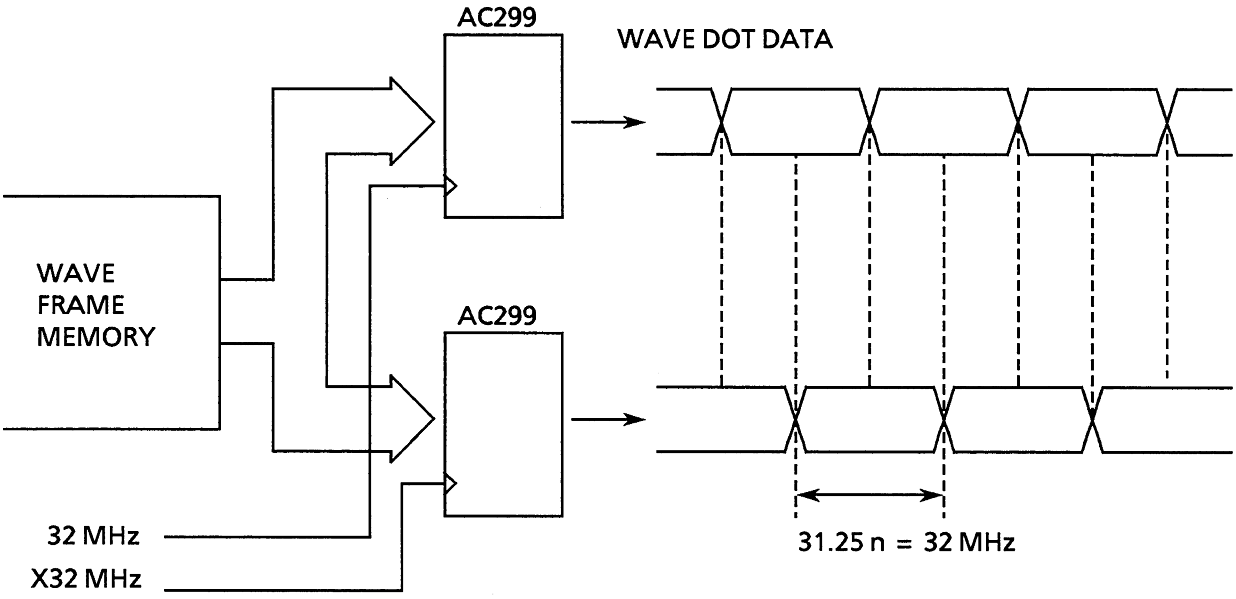
The priority level coded serial data such as ASD0 ~ 3 (shifted data) are strobe into the frame memory (IC348 ~ 395) via their serial I/O ports by the Serial Access Strobe (SAS 0,1). The ACW frame memory access timing is synchronized by the ACW 2MHz output clock. The ACW changes the access address to the WAVE RAM and frame memory with every XSLD timing signal. This process is continuously repeated.

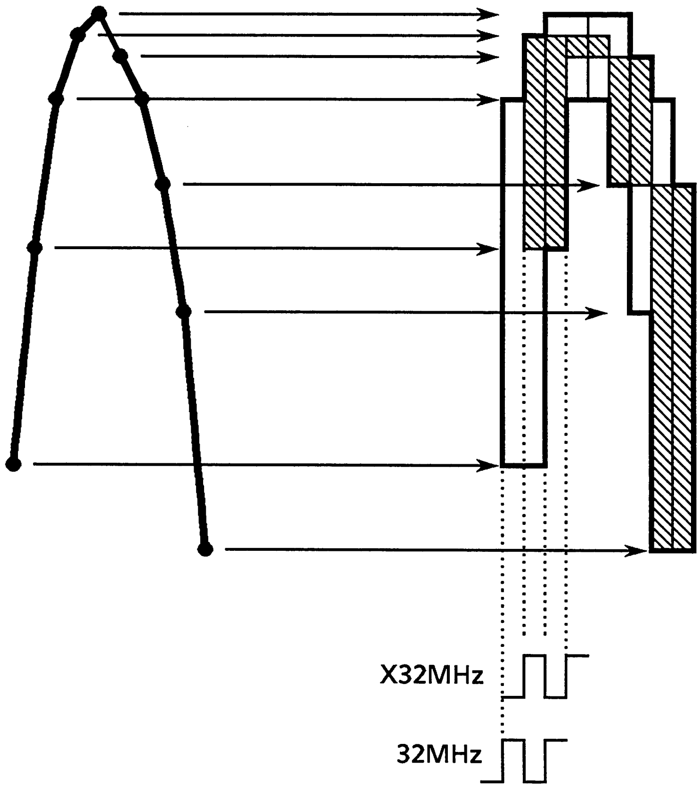
The XHSYNC signal clears the address counter in the ACW. The ACW displays the waveform trace on the CRT when it received the display command signal (XDSP1) from the ACRTC.

◆ Waveform Display circuit


BIT MAPPED DATA
P → S
COLOR PALETTE
SHIFT CLK
LOAD
FRAME MEMORY
READ ADDRESS
ACW

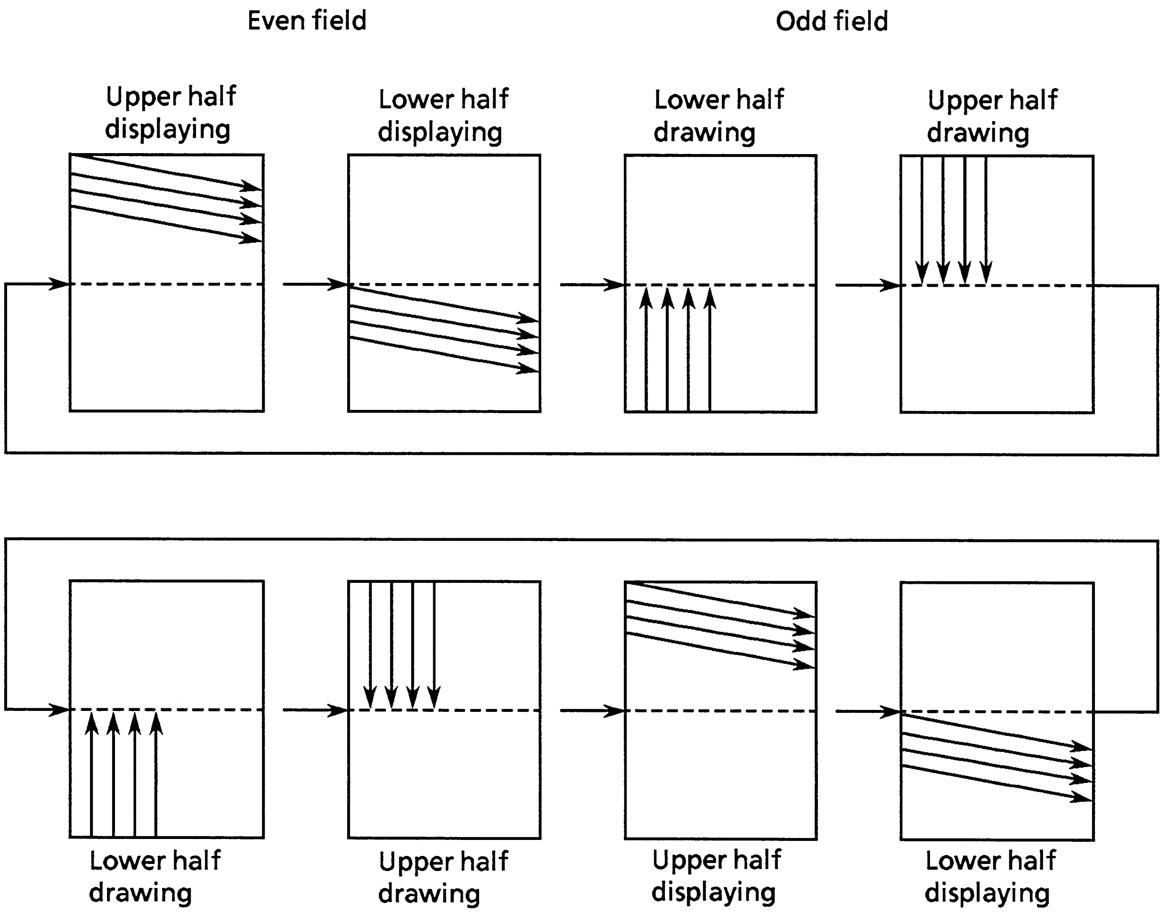
The IC396 ~ 407 latch the 16 bit parallel data from the frame memory and convert them into serial video data. The serial video data is loaded out under two timings: The 32MHz clock and X32MHz clock. The difference between the two clocks is 0.5 clock. This is to provide the display waveform trace with a high display resolution.

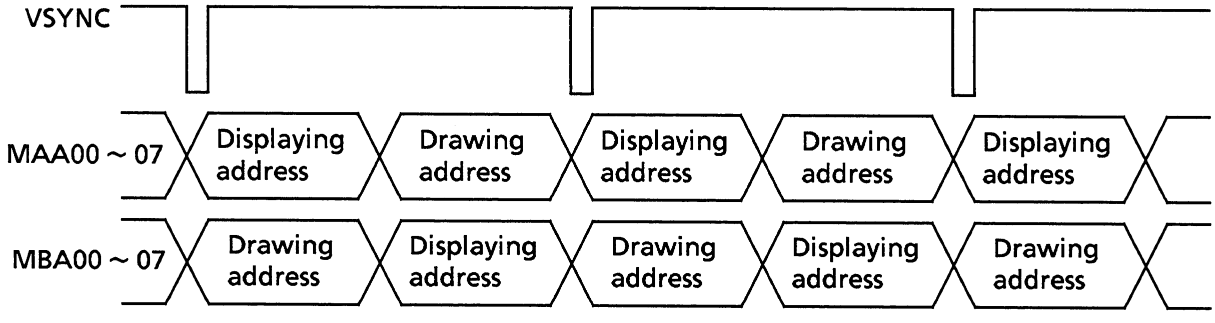

AC299
WAVE DOT DATA
WAVE
FRAME
MEMORY
AC299
32 MHz
X32 MHz
31.25 n = 32 MHz


X32MHz
32MHz

Waveform is not fixed graphic since it changes continuously. To display this continuously changing waveform, the frame memory has to simultaneously draw and display the waveform. To solve this problem, the frame memory is separated into an upper part and a lower part. The upper part of the frame memory draws the waveform and the lower part displays the waveform in the first half of its timing cycle. In the second half of the timing cycle, the upper part displays the waveform that the frame memory had drawn during the first half of the timing cycle, and the lower part draws the next waveform to replace the displayed waveform in first half of the timing cycle.

The illustration below shows the switching of the upper address (MAA00 ~ 07) and the lower address (MBA00 ~ 07).

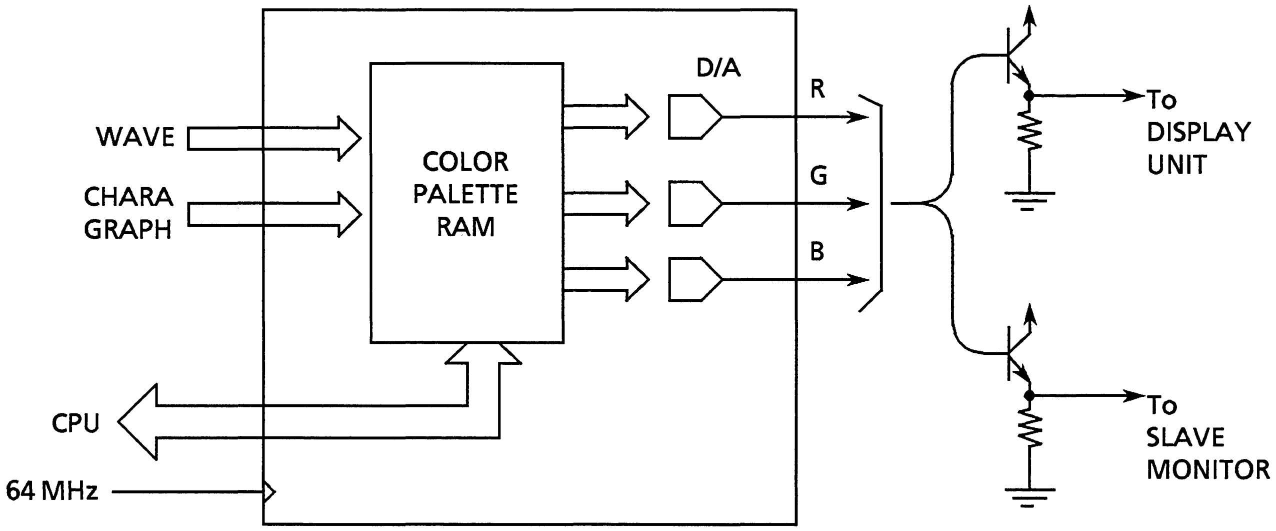

Even field
Odd field
Upper half displaying
Lower half displaying
Lower half drawing
Upper half drawing
Lower half drawing
Upper half drawing
Upper half displaying
Lower half displaying


VSYNC
MAA00 ~ 07
Displaying address
Drawing address
Displaying address
Drawing address
Displaying address
MBA00 ~ 07
Drawing address
Displaying address
Drawing address
Displaying address
Drawing address

◆ Color Palette Circuit

This color palette circuit adds the color palette code to the waveform, graphic, and character video signal. The D/A convertor converts the digital video RGB signals into analog RGB signals and outputs them to the CRT unit.

This circuit can simultaneously display up to 7 colors for waveform display and up to 15 different colors for character and graphic display.


WAVE
CHARA
GRAPH
CPU
64 MHz
COLOR PALETTE RAM
D/A
R
G
B
To DISPLAY UNIT
To SLAVE MONITOR

Color palette IC701

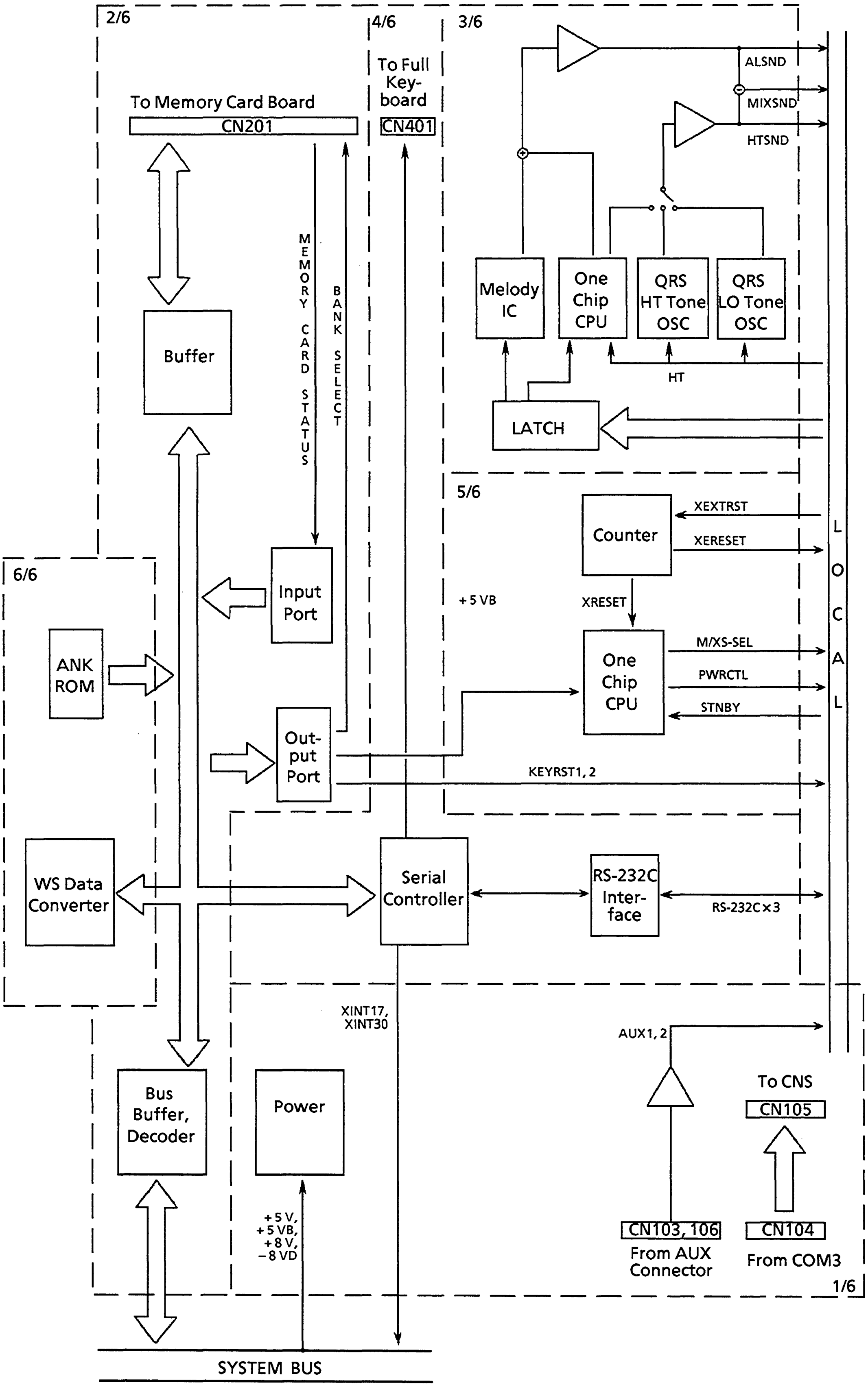
3-2-4 I/O Board, UP-0797

◆ General

The I/O board is the main interface unit with the external units, such as, the display unit and the keypad.

The functions of this board is:
* to interface with the display unit.
* to interface with the keypad.
* to read or write the memory card.
* to control the power supply.
* to generates the alarm sound and the QRS sound signals from the sound signal received from the CPU board.
* to serve as the input and output ports for the central monitors and the signal exchanger.
* to receive and amplify the waveform signals from the auxiliary (external) unit.
* to enable the screen display to be hardcopied by the recorder

Block Diagram


2/6
4/6
3/6
To Memory Card Board
CN201
To Full Keyboard
CN401
MEMORY CARD STATUS
BANK SELECT
Buffer
Input Port
Output Port
ALSND
MIXSND
HTSND
Melody IC
One Chip CPU
QRS HT Tone OSC
QRS LO Tone OSC
HT
LATCH
5/6
Counter
XEXTRST
XERESET
XRESET
+5 VB
One Chip CPU
M/XS-SEL
PWRCTL
STNBY
KEYRST1, 2
LOCAL
6/6
ANK ROM
WS Data Converter
Serial Controller
RS-232C Interface
RS-232C×3
XINT17, XINT30
AUX1, 2
To CNS
CN105
Bus Buffer, Decoder
Power
+5 V, +5 VB, +8 V, −8 VD
CN103, 106
From AUX Connector
CN104
From COM3
1/6
SYSTEM BUS

The I/O board consists of the following circuits:

- **Bus Buffer and Decoder Circuit**
  This circuit consists of the system bus and the decoder for the bus control signals from the CPU.

- **Memory Card Interface Circuit**
  This circuit reads/writes the data onto the selected bank in the memory card.

- **Serial Communication Circuit**
  IC404 and 408 control the serial communication with keypad, display unit, and the full-key board.

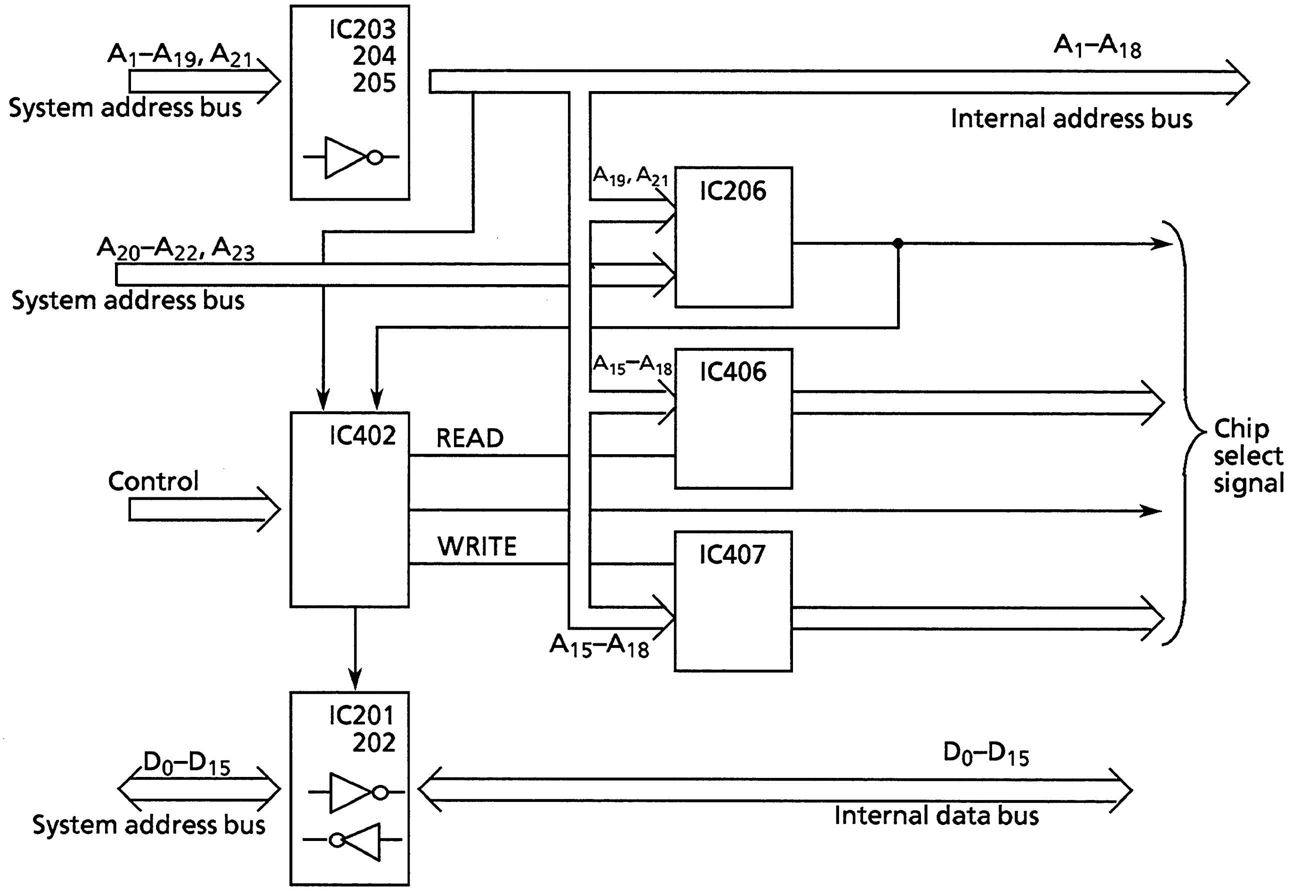
- **Power Supply Control Circuit**
  This circuit controls the power supply according to the instruction set by the CPU on the CPU board, or the keypad.

- **Sound Generator circuit**
  This circuit generates the alarm sound and the QRS sound.

- **Auxiliary Amplification Circuit**
  This circuit amplifies the signals from the front panel auxiliary unit input connector (AUX) , and the rear panel auxiliary unit input connector.

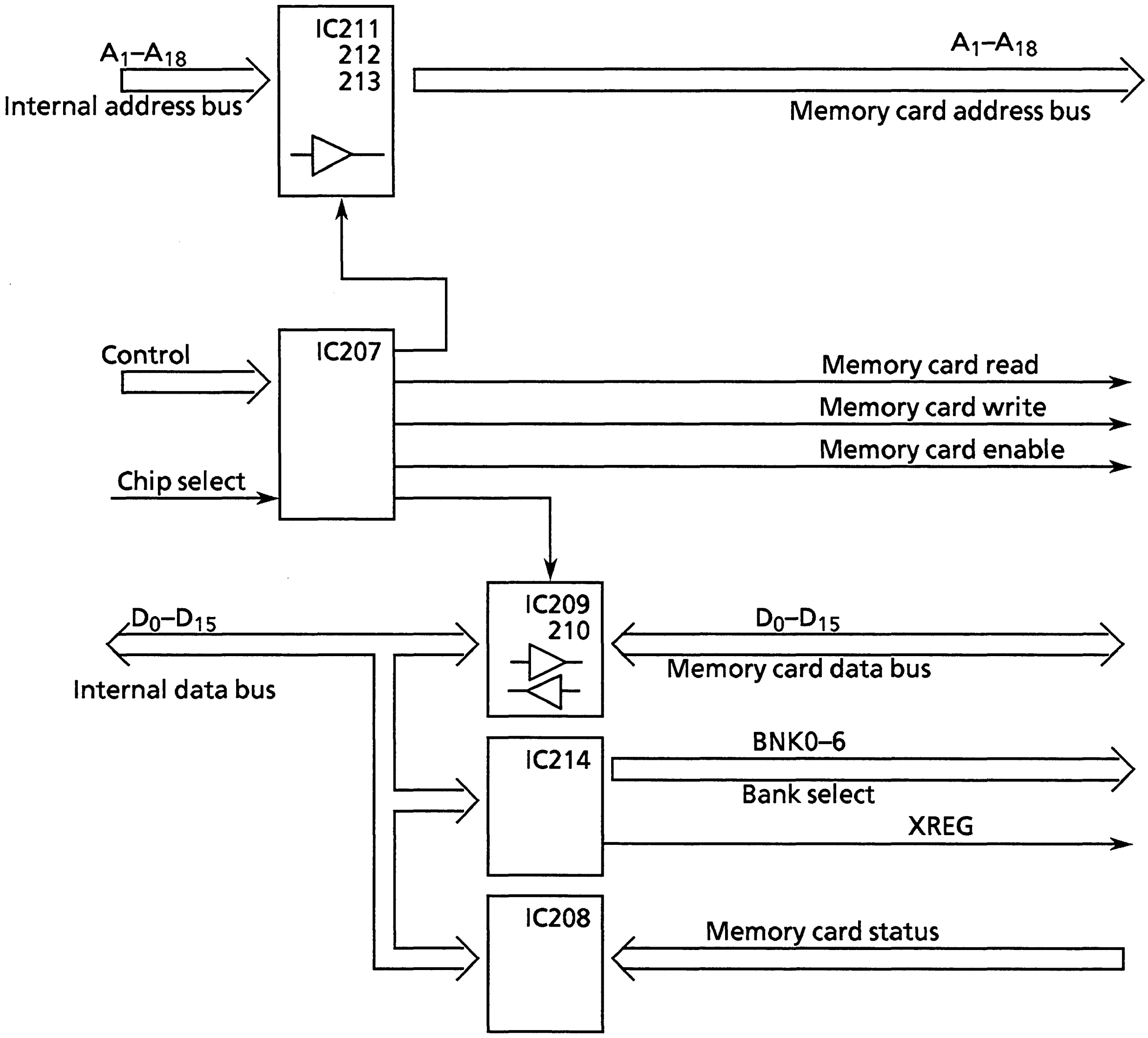
- **Hardcopying Processing Circuit**
  This circuit converts the screen data into recording data for the recorder.

◆ Bus Buffer and Decoder Circuit


A1–A19, A21
System address bus
IC203
204
205
A1–A18
Internal address bus
A19, A21
IC206
A20–A22, A23
System address bus
A15–A18
IC406
IC402
READ
Control
WRITE
IC407
A15–A18
Chip select signal
IC201
202
D0–D15
System address bus
D0–D15
Internal data bus

The buffers IC203 ~ 205 receive the address information from the system address bus and drive it to the internal bus. The bidirectional buffers IC201 ~ 202 receive and transmit the data from/to system data bus to/from internal data bus. IC402 receive the control signals (READ, WRITE, and DTACKB) from the CPU on the CPU board and in turn direct the bidirectional bus to transmit or the receive.
It also directs the decoders/multiplexers IC406 ~ 407 to access the bus.
The decoders/multiplexers decode the address data and outputs the chip selection signals to ROM IC509 ~510.

◆ Memory Card Interface Circuit


A1–A18
Internal address bus
IC211
212
213
A1–A18
Memory card address bus
Control
IC207
Memory card read
Memory card write
Memory card enable
Chip select
D0–D15
Internal data bus
IC209
210
D0–D15
Memory card data bus
IC214
BNK0–6
Bank select
XREG
IC208
Memory card status

The buffers IC211 ~ 213 receive the address information from the internal address bus and drive it to the memory card address bus. The buffers' latching timing is provided by IC207. IC207 also provides the latching timings and control signals (READ, WRITE, MEMORY CARD ENABLE, and DTACKB for the bidirectional bus transceivers IC209 ~ 210 to receive/transmit data to/from the internal data bus from/to the memory card data bus.

IC208 reads and interprets the status of the memory card. The table shows the signals received from the memory card board and their interpretation messages appearing on the display.

XCD1, XCD2 either or both are "HIGH" ——— MEMORY CARD NOT INSERTED

BVD1, BVD2 either or both are "LOW" ——— LOW BATTERY

WP is "HIGH" ——— WRITE PROTECT ERROR

IC214 selects the memory banks BNK0 ~ 6 in the memory card as directed by the control signal XMCPORTW from the IC407.

The memory card has two kinds of memory, namely, common memory and attribute memory. The selection of one these memories depends on the status of signal XREG.

XREG	Memory Selection
High	Common memory
Low	Attribute memory

◆ Serial Communication Circuit

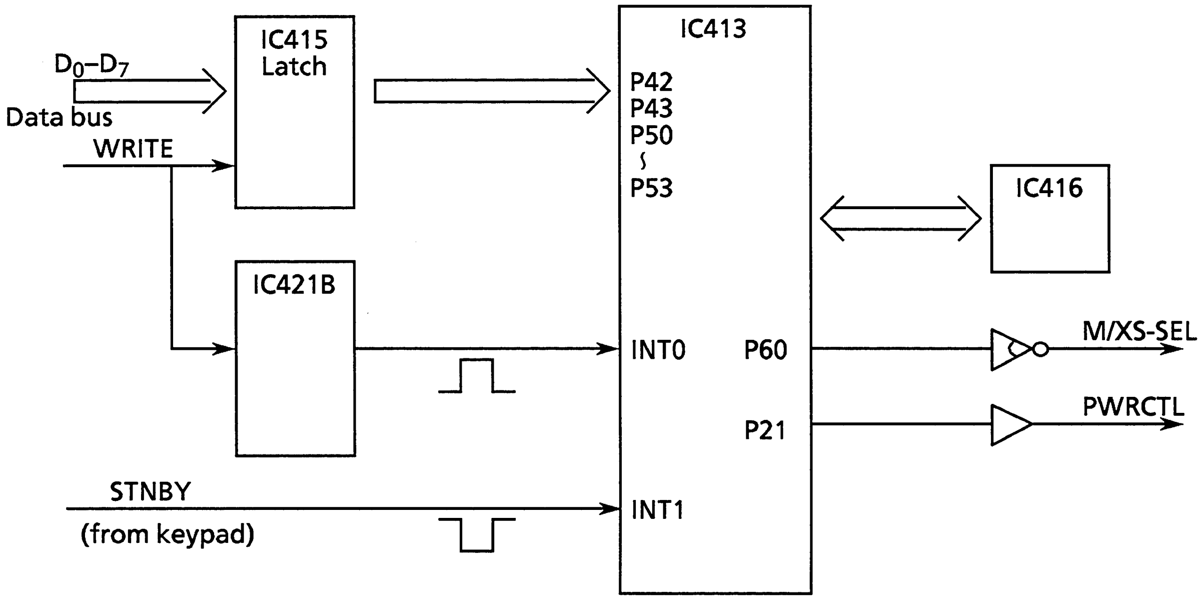
IC404 and 408 control the serial communication circuit. Each port in the two ICs communicates with different unit. The table below shows the port and the unit the port is communicating with.

IC404	Port A Port B	Full-key board Display unit
IC408	Port A Port B	Keypad when connected to the display unit Keypad when connected to the main unit

Communication with the display unit and keypad is by the RS-232C communication.

◆ Power Supply Control Circuit

● Function


D_0–D_7
Data bus
WRITE
IC415
Latch
IC421B
STNBY
(from keypad)
IC413
P42
P43
P50
∫
P53
INT0
P60
P21
INT1
IC416
M/XS-SEL
PWRCTL

This circuit controls the power supply of the bedside monitor main unit when POWER ON/OFF key on the keypad is pressed. The POWER ON/OFF key on the keypad switches the power supply unit either to its standby mode, or its operating mode. In the standby mode, the power supply unit only supplies the +5VB. Almost all the operating functions on the main unit shut down. The I/O board and the keypad are operational as they run on the +5 VB power supply.

IC413 controls this circuit. The status of the PWRCTL terminal of the IC413 sets the power supply unit to its operating mode or standby mode. The table below shows the status of the PWRCTL terminal and its power supply unit setting.

PWRCTL	Power supply
High	Standby
Low/Open	Fully operational

• Keypad Power ON/OFF

Prerequisite condition: The bedside monitor main unit is operating and waveforms are displayed on the display unit.

1) To set the bedside monitor main unit on standby, press the POWER ON/OFF key:
   i) The keypad senses that the Power ON/OFF key is pressed.
   ii) The keypad sends out the command signal to CPU board's CPU.
   iii) The CPU board's CPU receives the command signal and immediately sets the display unit's power supply off.
   iv) The CPU board's CPU then sends the command signal to IC413. This signal sets the monitor main unit power supply unit to its standby mode.
   v) IC413 of the I/O board receives the command signal via ports P42 and P43. This immediately sets IC413 PWRCTL terminal (P21) to HIGH.
   vi) The bedside monitor's power supply unit enters its standby mode.

2) To set the bedside monitor main unit back to its full operational mode, press the POWER ON/OFF key again:
   i) The keypad senses that the Power ON/OFF key is pressed.
   ii) The keypad sends out the command signal to IC413 of the I/O board.
   iii) IC413 of the I/O board receives the command signal via its INT1 terminal, and this consequently sets its PWRCTL terminal LOW/OPEN.
   iv) The bedside monitor main unit's power supply unit returns to full operational mode.
   v) The CPU of the CPU board undergoes reset procedure, and finally switches the display unit's power supply unit on.

• Bedside Monitor Main Unit Master/Slave Mode Function

The bedside monitor main unit, when connected to the display unit, can operate in either the master mode (display unit in the slave mode), or the slave mode (display unit in the master mode). The IC413 sets the operating mode of the bedside monitor main unit by reading the data in its ports P50 ~ P53. The IC413 then asserts or negates the selection signal M/XS-SEL. In normal operation, the bedside monitor main unit operates in the slave mode.

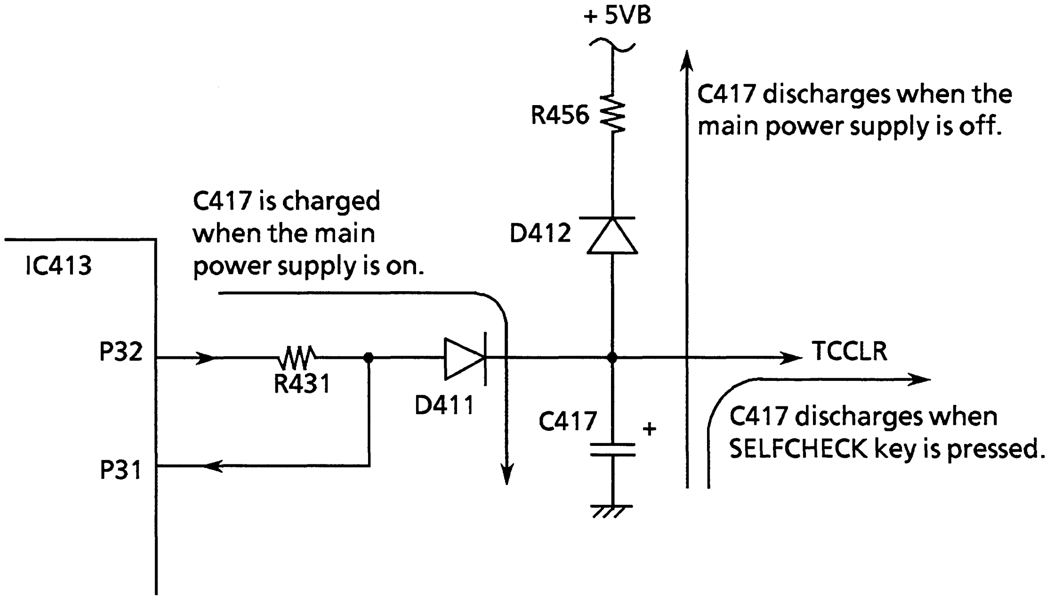
• Power Down Protection Control

This is to prevent IC413 from reading any data inputted into its INT0 terminal when when the + 5V supply is LOW.

• Reset

During normal operation, when the main power switch is accidentally switched off, or a sudden temporary loss of power occurrs, the operating settings of the bedside monitor may be lost. These operating settings are the power supply status (standby mode or full operational mode) and the operating status of the main unit (master mode or slave mode). Therefore, when the main power supply is reconnected, the bedside monitor is reset.The bedside monitor may now operate on the operating settings different from those before the power failure.

To prevent this from affecting the bedside monitor, the IC416 reads the operating settings of IC413 and stores them in its memory. When the power supply is reconnected, the IC413 now reads the memory of IC416 for the operating settings. This is only effective as long as the temporary + 5VB power supply from capacitor C417 is available.


+ 5VB
R456
C417 discharges when the main power supply is off.
C417 is charged when the main power supply is on.
D412
IC413
P32
R431
D411
TCCLR
C417
+
C417 discharges when SELFCHECK key is pressed.
P31

P31 = H ·········· Instantaneous → operating settings maintained
P31 = L ·········· Main power supply ON → Power supply ON

• Main Power Supply On

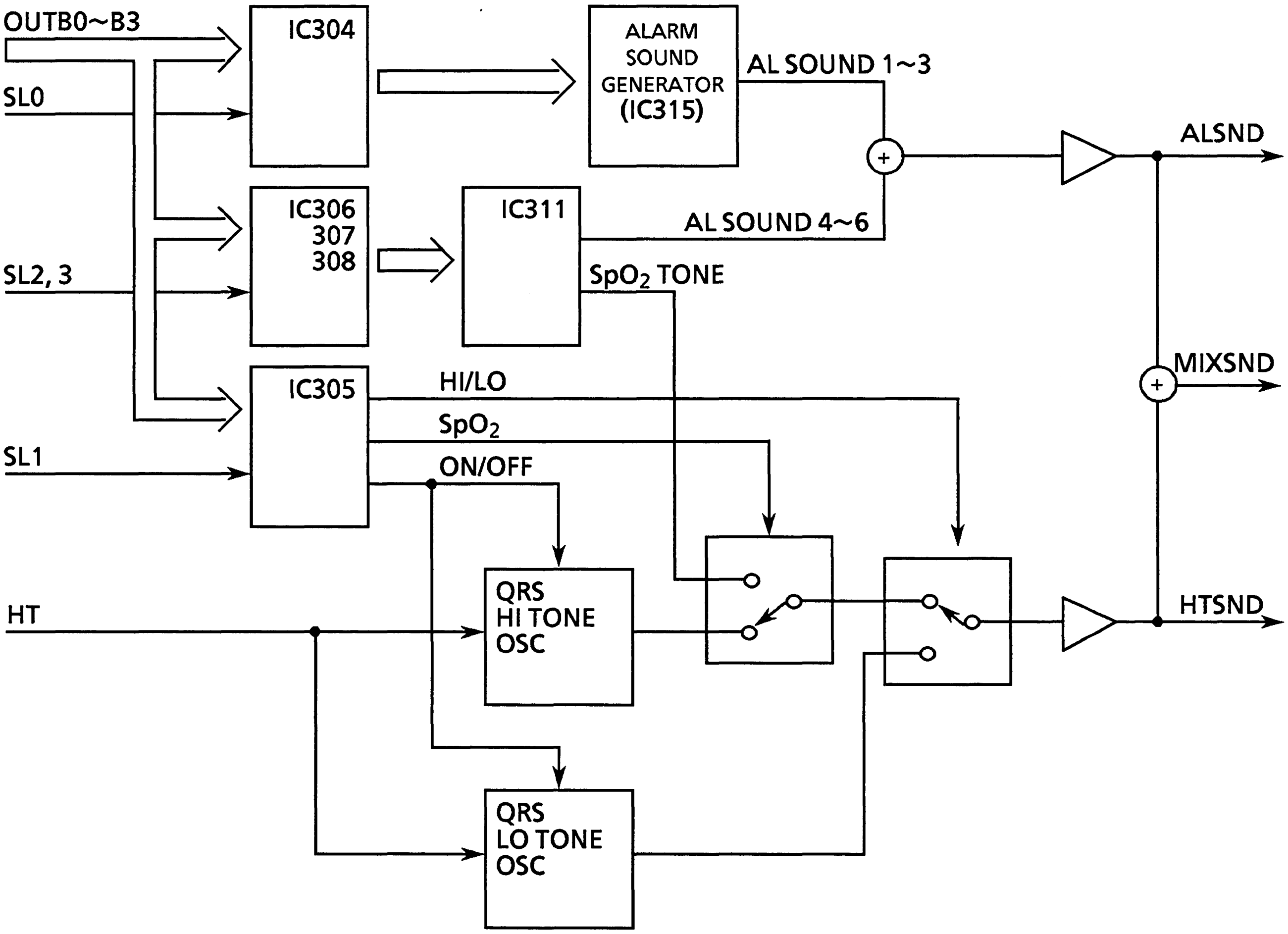
To differentiate the reset operation after a temporary power failure from that of initially switching the main power supply on, IC413's port P31 status is read. When this port is HIGH, the memory in IC416 is read during resetting procedures. However, when the port is LOW, the memory in IC416 is disregarded during resetting procedures.

In the SELFCHECK mode, both the IC413 and capacitor are cleared and reset.

NOTE

The resupply of power back to the bedside monitor is different from that of the function of the POWER ON/OFF key of the keypad.

◆ Sound Generator Circuit


OUTB0~B3
SL0
SL2, 3
SL1
HT
IC304
ALARM SOUND GENERATOR (IC315)
AL SOUND 1~3
ALSND
IC306 307 308
IC311
AL SOUND 4~6
SpO2 TONE
IC305
HI/LO
SpO2
ON/OFF
MIXSND
QRS HI TONE OSC
QRS LO TONE OSC
HTSND
+

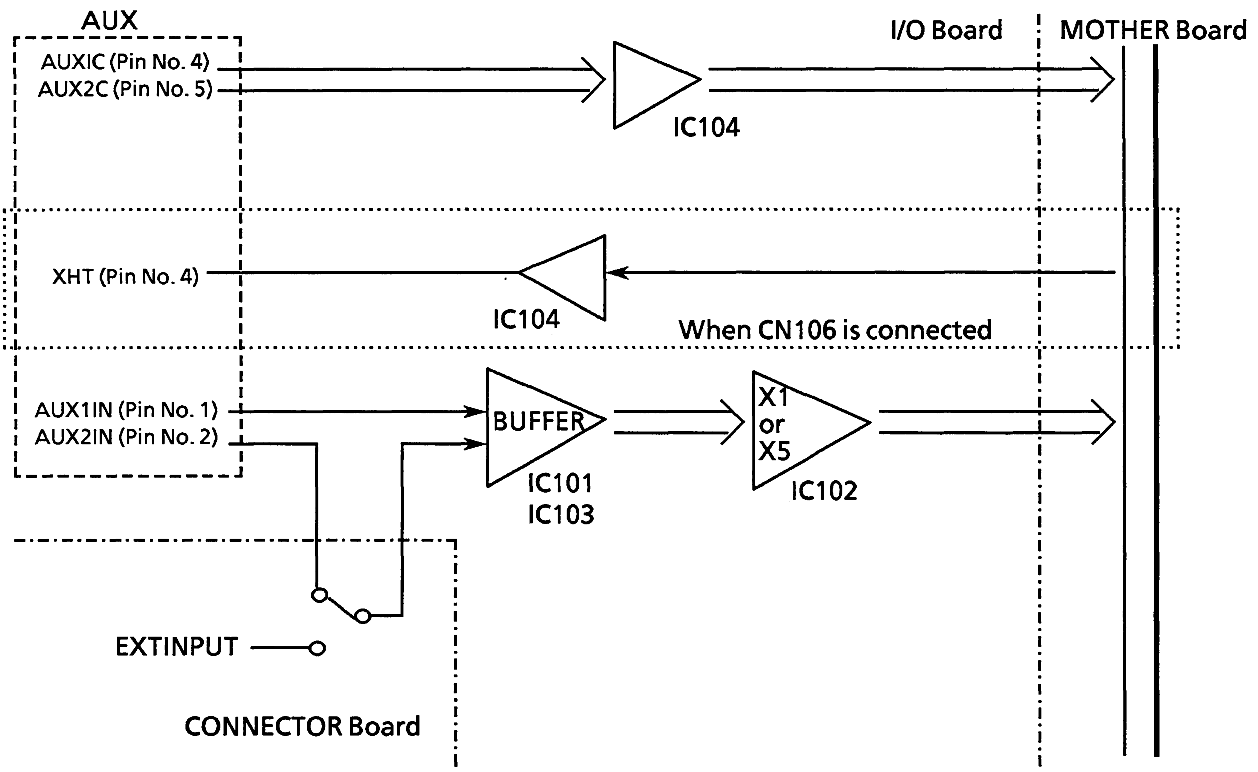
The key controller IC176 of the CPU board supplies the control signals (OUTB0 ~ 3 and SL0 ~ 3) to this sound generator circuit. The table below shows the output port of the key controller IC176 of the CPU board.

Sound Generator Output Signal

SL	OUT	Description		
SL0	B0	Continuous alarm	1: ON	0: OFF
	B1 B2	Alarm Sound 1~3	$\binom{0}{0}$: “piropiro” sound $\binom{0}{1}$: “pinpon” sound $\binom{1}{1}$: “pon” sound	
	B3	Alarm sounds once	1: ON	0: OFF
SL1	B0	QRS SYNC sound pitch	1: high pitch	0: low pitch
	B1	QRS SYNC sound ON/OFF	1: ON	0: OFF
	B2	SpO$_2$ tone	1: normal sound	0: SpO$_2$ tone
	B3	Not used		
SL2	B0	IC311 reset		0: reset
	B1 B2	Alarm sound 4~5	$\binom{0}{0}$: high pitch “pipipi” sound $\binom{1}{0}$: middle pitch “pipi” sound $\binom{0}{1}$: low pitch “pipi” sound $\binom{1}{1}$: OFF	
	B3	SpO$_2$ tone highest level bit		
SL3	B0	SpO$_2$ tone lowest level bit	From the 5 bits data 25 different pitches are generated. (1,1,1,1,1) highest pitch (0,0,1,1,1) lowest pitch	
	B1	SpO$_2$ tone second level bit		
	B2	SpO$_2$ tone third level bit		
	B3	SpO$_2$ tone fourth level bit		

These control signals are latched by IC304 ~ 308 in the sound generator circuit.
In this sound generator circuit, IC315 and 311 generate the alarm sound signal, ALSND. When the SpO$_2$ tone function is selected, the IC311 outputs the SpO$_2$ value to the QRS high tone generator circuit. Here, the resulting QRS high tone pitch varies with the value of the SpO$_2$.

◆ Auxiliary Amplification Circuit


AUX
AUXIC (Pin No. 4)
AUX2C (Pin No. 5)
IC104
I/O Board
MOTHER Board
XHT (Pin No. 4)
IC104
When CN106 is connected
AUX1IN (Pin No. 1)
AUX2IN (Pin No. 2)
BUFFER
IC101
IC103
X1
or
X5
IC102
EXTINPUT
CONNECTOR Board

The main function of this board is to amplify the external unit input signals.
The settings of jumpers J101 and 102 determine the amplifications factor (X1 or X5) of IC102.

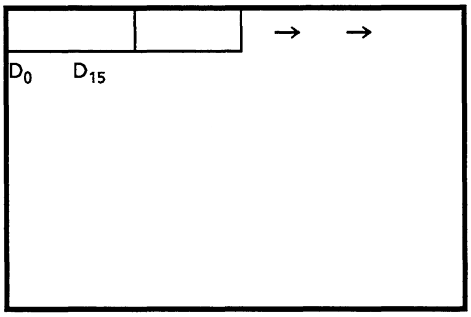
The bedside monitor can receive the external unit input via its two auxiliary inputs (AUX) – one located at the front panel of the main unit and the other located at rear panel of the main unit. The auxiliary input in the front panel is given the priority over the one of the rear panel. This means, if the two auxiliary inputs are used simultaneously, the main unit receive the auxiliary input signal connected to its front panel only. The selection device in the CONNECTOR board selects the auxiliary input signal from the front panel when its auxiliary input signal connector of the front panel is connected.

The auxiliary unit is connected to the I/O board through either the I/O board's STANDARD connector CN103, or HTOUT connector CN106. In standard application, the STANDARD connector CN103 is used. The main unit receive the various alarm signals (depending on the auxiliary unit, $ETCO_2$ alarm or SpO_2 alarm) via the AUX1C pin (pin No.4) of auxiliary connector.
For external unit that requires the QRS synchronizing signal (HTOUT), the HTOUT connector CN106 is used. The pin No.4 of the auxiliary connector now carries the output signal (HTOUT) to the external unit.

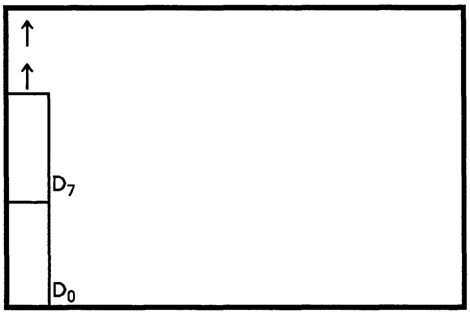
◆ Hardcopying Processing Circuit

The function of this circuit is to allow the recorder to hardcopy the display on the screen of the display unit. To do this the format of the screen data needs to be converted so that the recorder can print the information.

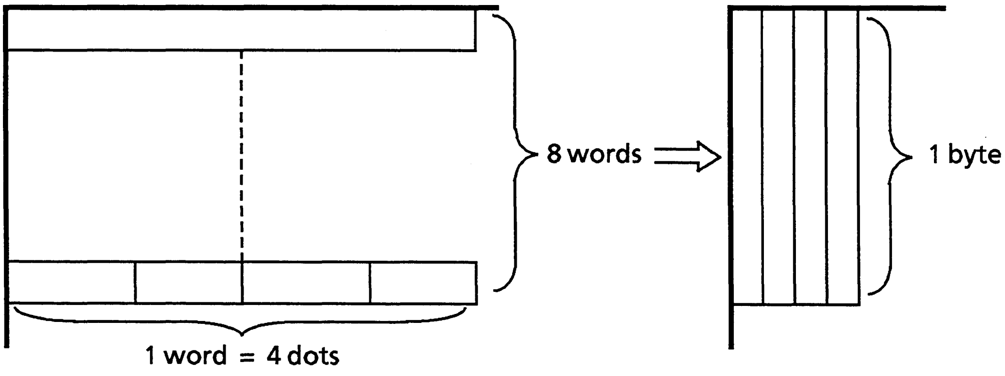
The screen data is arranged from left to right and from top to bottom as shown in the illustration below.



The hardcopy data to the recorder is arranged from bottom to top and from left to right as shown in the illustration below.



The screen 4 bit data (R, G, B, and I) is converted to 4 bit recorder data. This 4 bit recorder data represents 1 printing dot. Hence, 1 WORD of screen is converted into 4 dots of printing information. The shift registers IC505 ~ 508 input the 1 WORD screen data 8 times before they output 4 BYTE of vertical arranged printing data.

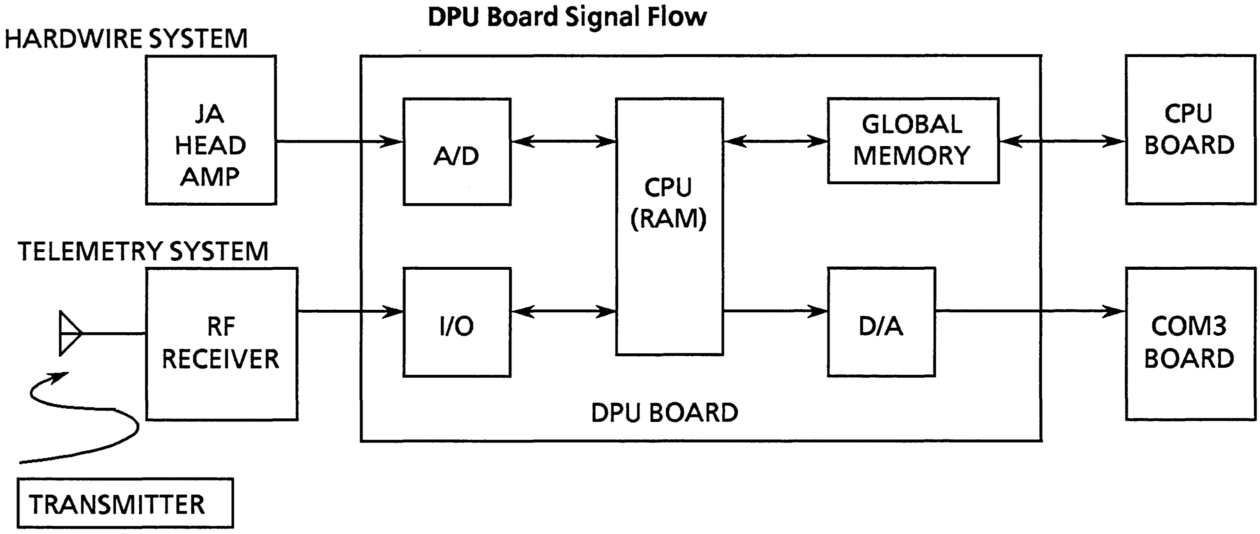


For printing the characters displayed on the screen, the addresses of the characters are read by ANKROMs IC509 and 510. Since the character data for the screen is doubled to increase the character width, this process is replicated in this circuit. Here, IC511 and 512 are used so that the vertical printing character data read out from the ANKROMs is doubled. The horizontal printing character data is doubled through software program to balance out the final printing.

3-2-5 DPU Board, UP-0670

◆ General

DPU Board Signal Flow



The Data Processing Unit (DPU) board processes vital signs data, from the hardwired input box or telemetry transmitter, with the slave Micro Processing Unit (MPU) [68HC000] which is controlled by the master MPU on the CPU board (UR-3027).

• Hardwired System

The DPU board controls head amplifiers and processes ECG/Respiration analog signals before timesharing or directly timeshares the other analog signals with the 16-ch. Multiplexer (IC705 & 706).

The DPU board converts all the analog signals to digital signals with the 12-bit A/D converter (IC725) through the Gain selector (IC723) [twice gain: blood pressure signals. once gain: the others] and Base-line shifter (IC721).

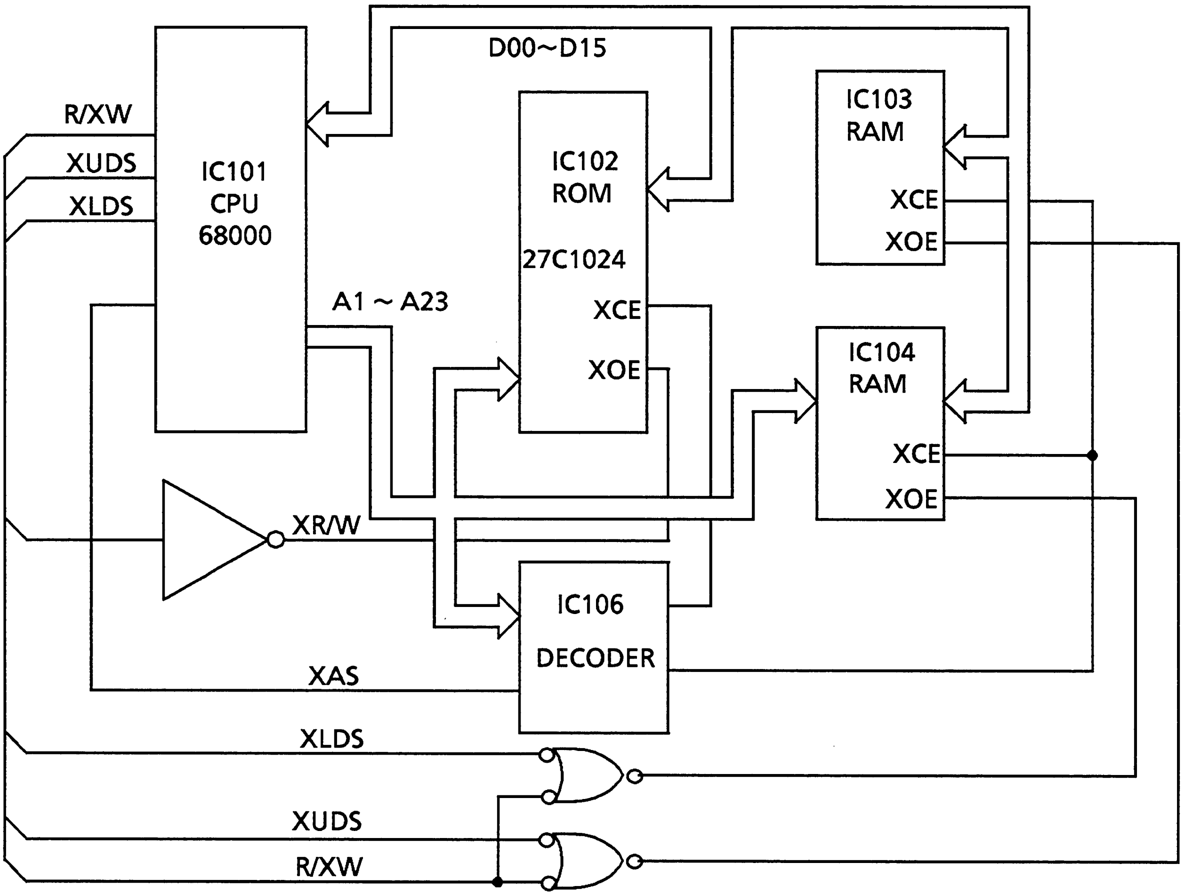
The DPU board primarily formats the digital signals with the slave 16-bit MPU [68HC000] (IC101) and stores the formatted data into the Global memory (IC225 & 226) so that the CPU board reads the data from the global memory at a fixed interval (128 msec.).

• Telemetry System

The analog wave acquired a patient is converted to digital data on a transmitter and sent to the main unit. After reception of the data on RF receiver unit, the data is converted from serial to parallel by gate array IC and then read by 16 bit CPU.

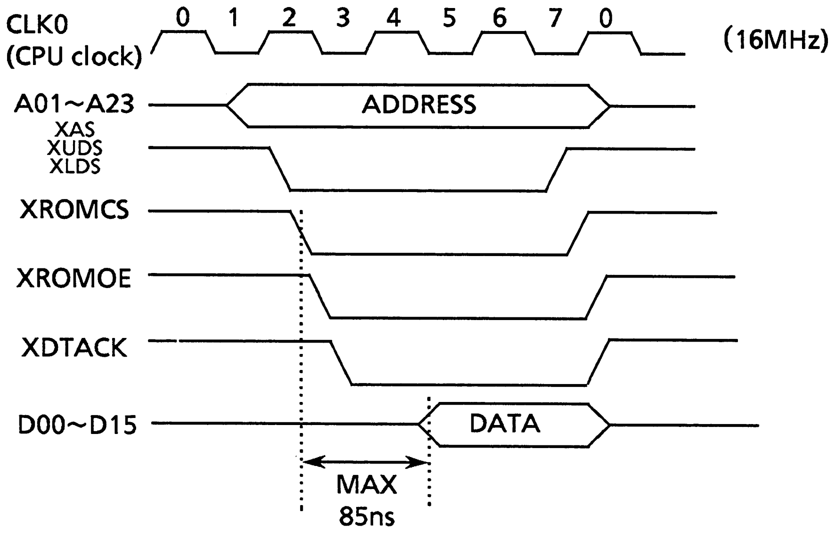
The processing method afterward is the same as the above hardwired system.

◆ MPU/ROM/RAM Circuit


D00~D15
R/XW
XUDS
XLDS
IC101
CPU
68000
IC102
ROM
27C1024
XCE
XOE
IC103
RAM
XCE
XOE
IC104
RAM
XCE
XOE
A1 ~ A23
XR/W
IC106
DECODER
XAS
XLDS
XUDS
R/XW

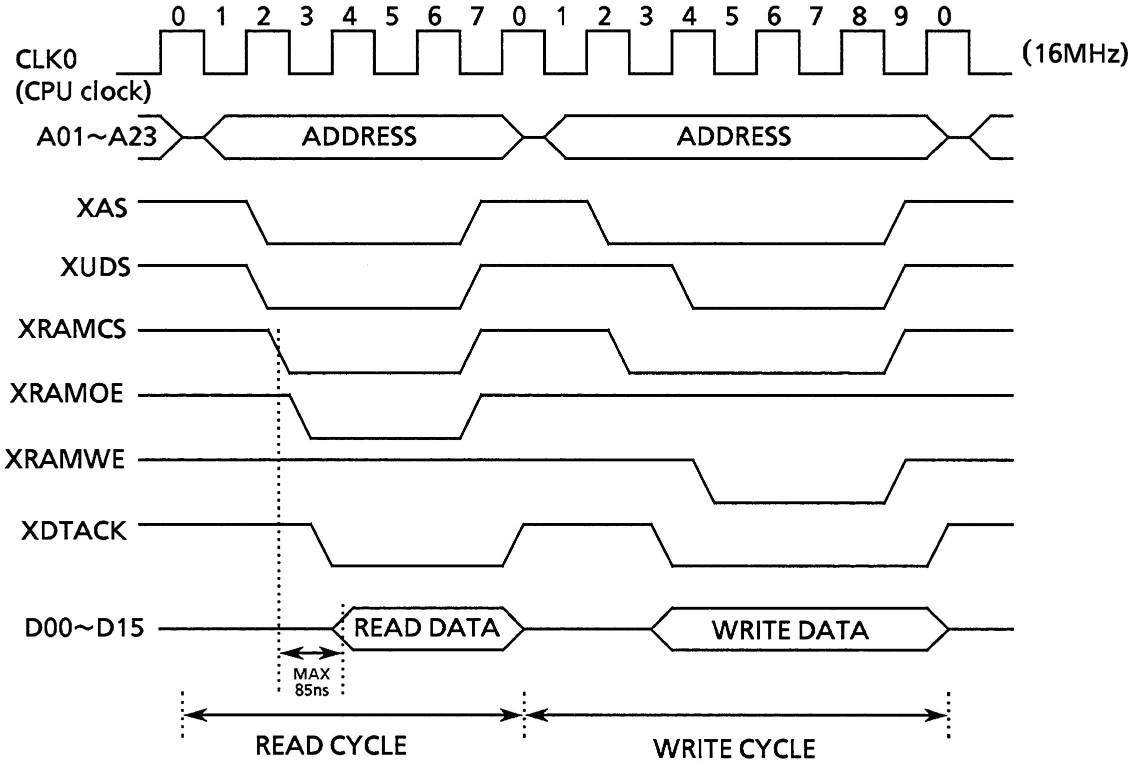
The Micro Processor Unit MPU [68000] (IC101) accesses ROMs (IC102) or RAMs (IC103,104) as follows:

[ROM ACCESS TIMING CHART]


CLK0
(CPU clock)
0 1 2 3 4 5 6 7 0
(16MHz)
A01~A23
ADDRESS
XAS
XUDS
XLDS
XROMCS
XROMOE
XDTACK
D00~D15
DATA
MAX
85ns

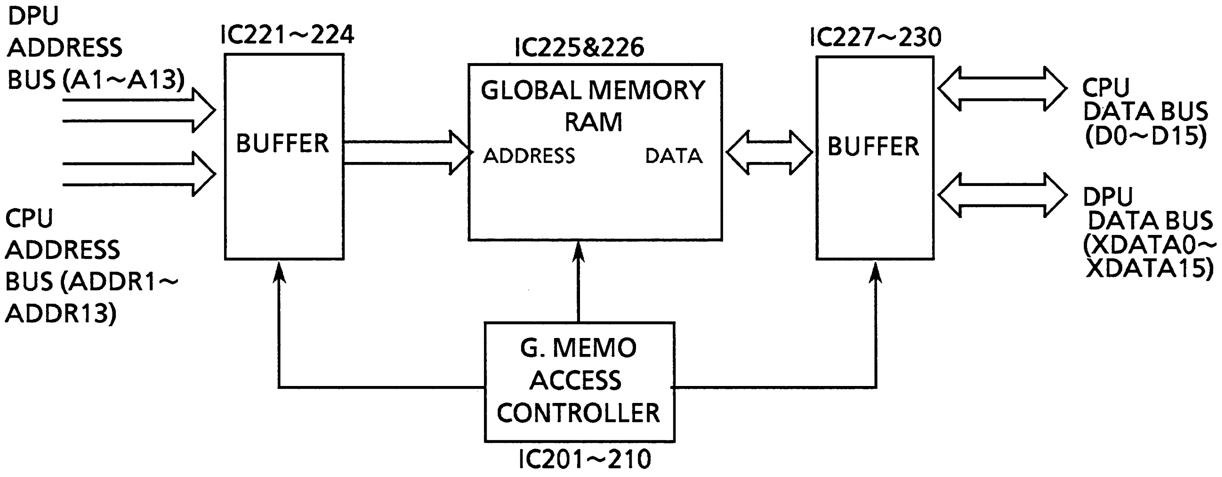
The ROM (IC102) provides 1 Mbit memory and 85 ns access time. The total memory capacity of the ROM is 128 kbytes.

[RAM ACCESS TIMING CHART]


0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 8 9 0
CLK0
(CPU clock)
(16MHz)
A01~A23
ADDRESS
ADDRESS
XAS
XUDS
XRAMCS
XRAMOE
XRAMWE
XDTACK
D00~D15
READ DATA
WRITE DATA
MAX
85ns
READ CYCLE
WRITE CYCLE

The RAM provides 256 kbit memory and 85 ns access time. The total capacity of the RAMs (IC103,104) is 32 kwords.

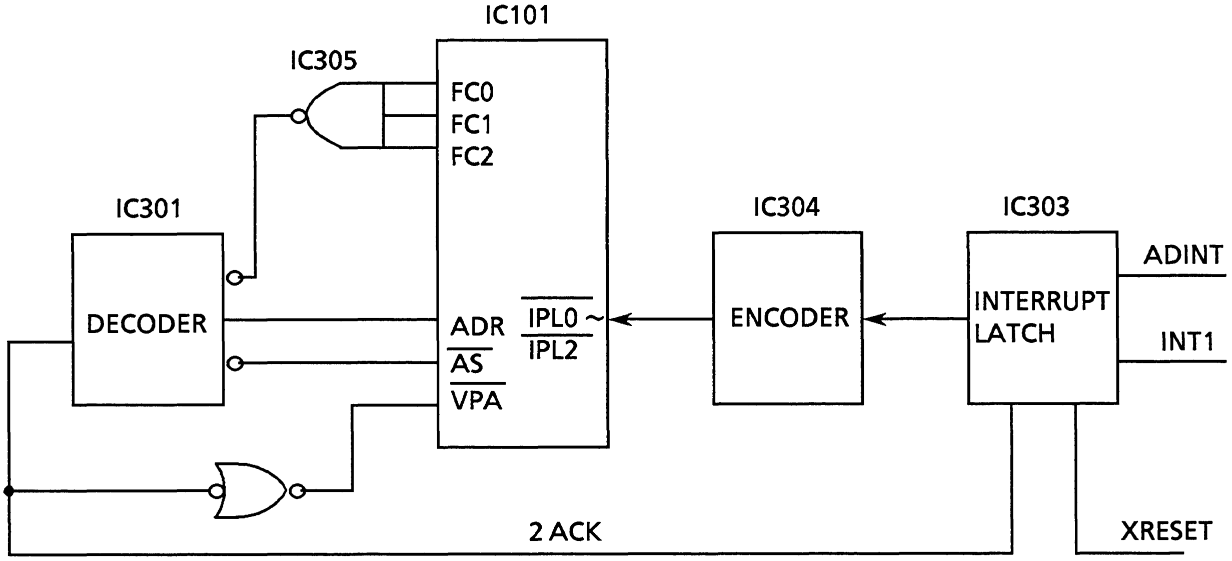
◆ Global Memory Control Circuit


DPU
ADDRESS
BUS (A1~A13)
CPU
ADDRESS
BUS (ADDR1~
ADDR13)
IC221~224
BUFFER
IC225&226
GLOBAL MEMORY
RAM
ADDRESS
DATA
IC227~230
BUFFER
CPU
DATA BUS
(D0~D15)
DPU
DATA BUS
(XDATA0~
XDATA15)
G. MEMO
ACCESS
CONTROLLER
IC201~210

XDATA, XADDR: from System Bus
D, A: from CPU Bus of DPU

The above global memory control circuit provides dual access function to the global memory (IC225&226) from the master MPU on the CPU board or the slave MPU on this board for communication between the CPU and DPU board.
The dual access function is controlled by the global memory access controller (IC201~210). The access controller accepts a former access and keeps another one waiting when both accesses are found.
The global memory data is read, modified or written by both MPUs.

◆ Interrupt Control Circuit



The above circuit generates an Auto-vectored interrupt to the MPU on this board or a Vectored interrupt to the MPU on the CPU board.

• Auto-vectored Interrupt

The interrupt is processed with a vector generated in the MPU.
The encoder (IC143) requests an interrupt to the MPU (IPL0~2 terminal) when the interrupt request signal, ADINT or INT1 is latched by the interrupt latch (IC303).
The IC1303 latches ADINT or INT1 with a positive-going edge and resets with the initialization signal, XRESET or the individual interrupt acknowledge signal from the decoder (IC301).
The interrupt acknowledge signal from the MPU sets FC0~FC2 High and the same level signals appear on A1~A3 of Address line. They are inputted to the decoder and an interrupt acknowledge signal (ACK) is generated. Simultaneously, the ACK signal is returned to VPA terminal of MPU, which is the Auto-vectored interrupt.

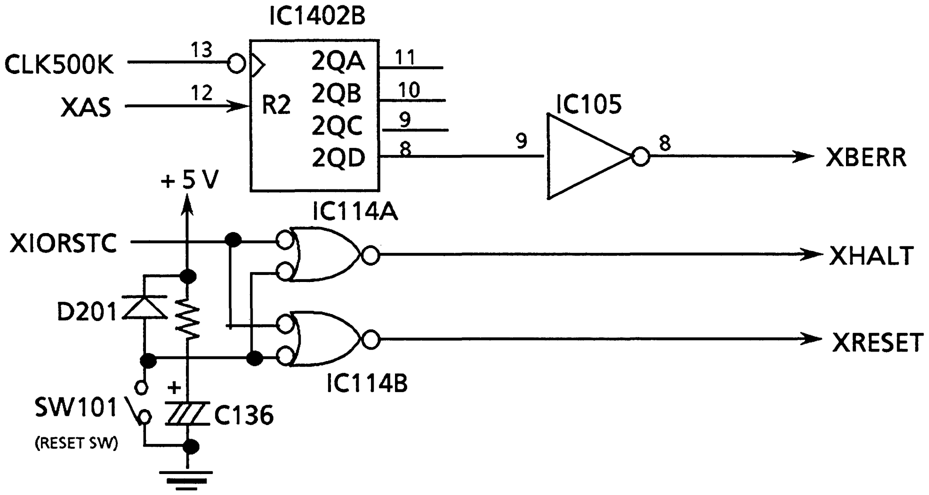
INTERRUPT PRIORITY	Interrupt Request signal	Explanation
7		No use
6		No use
5		No use
4	ADINT	Periodic interrupt for A/D conversion timing (every 2 msec)
3		No use
2		No use
1	INT1	Command interrupt from the MPU on the CPU board (at random)

• Vectored Interrupt

The interrupt signal (INT13) is generated from the MPU on the DPU board to the MPU on the CPU board approximately every 128 msec to indicate a wave data set on the global memory to the MPU (CPU board).

INTERRUPT PRIORITY	Interrupt Request signal	Explanation
INT13	XCPU INT	Periodic Interrupt to CPU from DPU to have wave data (approx 128 msec) set

◆ **Bus Error & Reset Circuit**

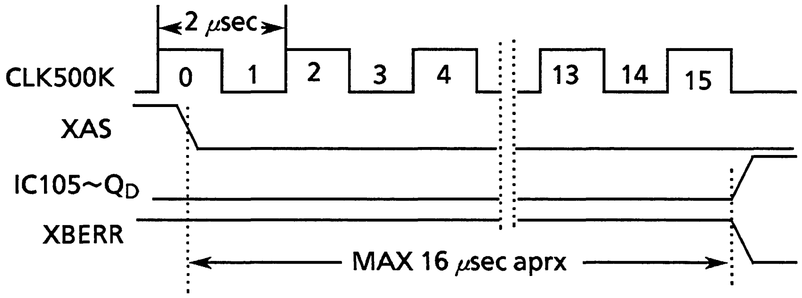

IC1402B
CLK500K
13
XAS
12
R2
2QA
2QB
2QC
2QD
11
10
9
8
IC105
9
8
XBERR
+5V
IC114A
XIORSTC
XHALT
D201
XRESET
IC114B
SW101
(RESET SW)
+
C136

● Bus Error Detecting circuit

The detecting circuit informs the MPU (IC101) on this board of any trouble found in the bus cycle during an execution. If Address Strobe signal XAS is not negated on the Counter (IC402B) within 16 μsec due to the following condition, Bus Error XBERR is outputted to the MPU through the IC105.

DTACK signal is not asserted.

VPA signal is not asserted.


2 μsec
CLK500K
0
1
2
3
4
13
14
15
XAS
IC105~QD
XBERR
MAX 16 μsec aprx

● Reset circuit

The reset circuit which consists of IC114B,R201 and C201 generates the reset signal XRESET (XHALT) in the following case.

When the reset switch (SW101) is depressed;

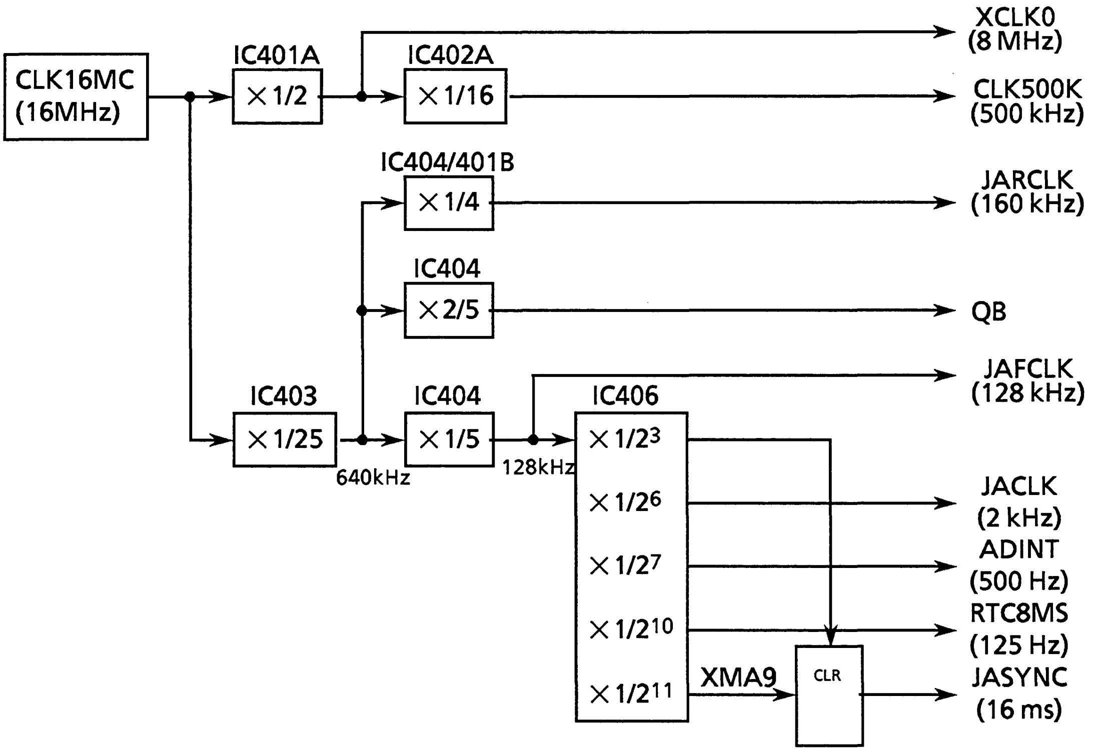
When the power switch is turned on;

When a reset command is executed;

When the reset signal XIORSTC is outputted from the CPU board to this circuit.

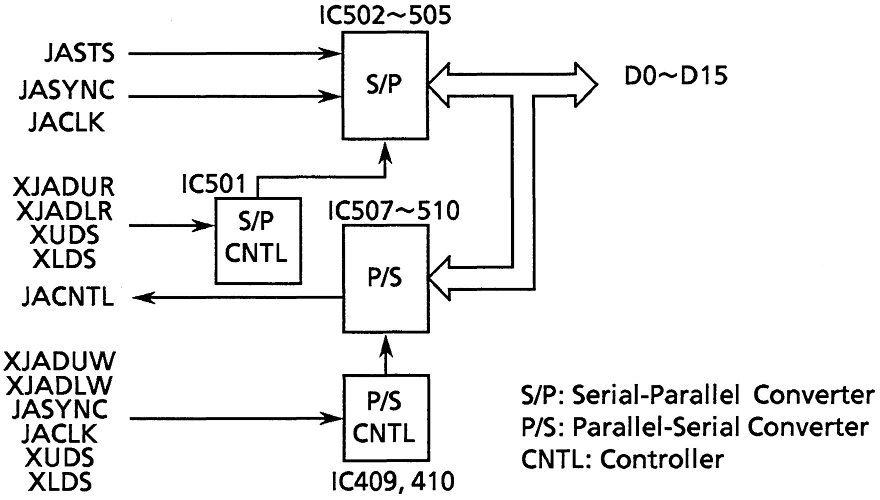
◆ Timing Control Circuit

The timing control circuit generates the following various clocks with the 16MHz system clock from the CPU board.


CLK16MC
(16MHz)
IC401A
×1/2
IC402A
×1/16
XCLK0
(8 MHz)
CLK500K
(500 kHz)
IC404/401B
×1/4
JARCLK
(160 kHz)
IC404
×2/5
QB
IC403
×1/25
640kHz
IC404
×1/5
128kHz
JAFCLK
(128 kHz)
IC406
×1/2³
×1/2⁶
×1/2⁷
×1/2¹⁰
×1/2¹¹
JACLK
(2 kHz)
ADINT
(500 Hz)
RTC8MS
(125 Hz)
XMA9
CLR
JASYNC
(16 ms)

CLOCK	Frequency	Duty	Function
CLK0 XCLK0	8 MHz	50 %	MPU clock on DPU board
CLK500K	500 kHz	50 %	Clock to detect Bus Error or convert A to D, D to A
JARCLK	160 kHz	50 %	Clock to detect respiration waveform at the input box
JAFCLK	128 kHz	40 %	Clock to float the input circuit on each Head Amp board
JACLK	500 μS	50 %	Clock to communicate (DPU - Input box)
ADINT	2 ms	50 %	Timing clock to convert A to D every 1ms
RTC8MS	8 ms	50 %	Timing clock to interrupt to CPU board (ever 8 ms) Timing clock to synchronize wave display between CPU board and CRTC board
JASYNC	16 ms	See next page	Timing clock to synchronize communication (DPU-Input box)

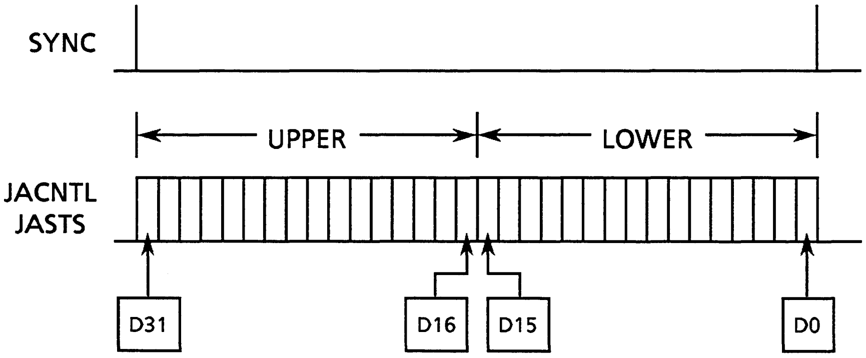
◆ JA Data Control Circuit


IC502~505
JASTS
JASYNC
JACLK
S/P
D0~D15
XJADUR
XJADLR
XUDS
XLDS
IC501
S/P CNTL
IC507~510
JACNTL
P/S
XJADUW
XJADLW
JASYNC
JACLK
XUDS
XLDS
P/S CNTL
IC409, 410

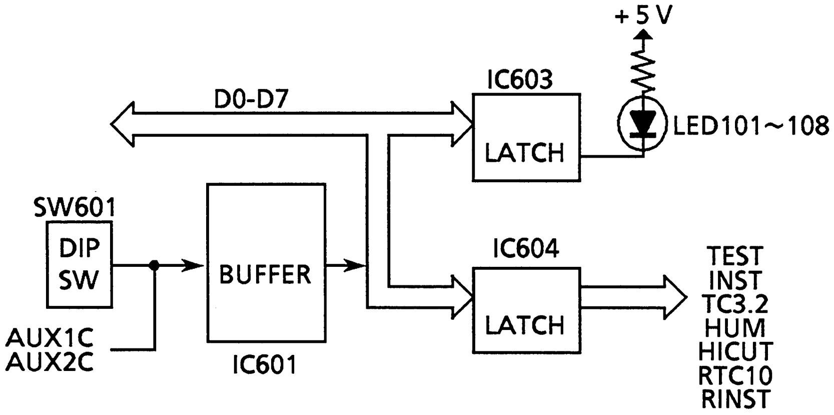
S/P: Serial-Parallel Converter
P/S: Parallel-Serial Converter
CNTL: Controller

32-bit serial format signals JACNTL and JASTS are transferred between the DPU board and Input box.
The Parallel-serial converter (IC507~510) converts parallel data D0~D15 to the serial format signal JACNTL to control the input box.
The Serial-parallel converter (IC502~505) converts the serial format signal JASTS to parallel data D0~D15. The JASTS signal indicates the status of the input box to the MPU on this board.

JACNTL: to control each head amplifier and LEDs/key sound on the input box
JASTS : to indicate the status of each head amplifier and keys in the input box


SYNC
UPPER
LOWER
JACNTL
JASTS
D31
D16
D15
D0

◆ LED/DIP Switch Circuit


+5V
IC603
D0-D7
LATCH
LED101~108
SW601
DIP SW
BUFFER
IC604
LATCH
TEST
INST
TC3.2
HUM
HICUT
RTC10
RINST
AUX1C
AUX2C
IC601

The buffer (IC601) is an input port to indicate the status of the DIP switch (SW102) and external signals AUX1C/AUX2C to the MPU on this board.

The latch (IC603) is an output port to latch data for the LEDs (LED101~108) indication.

The latch (IC604) is an output port to latch control signals for the ECG/RESP Processing circuit on this board.

[IC601]

D0	DIPSW0	OFF {Factory Set}
D1	DIPSW1	↓
D2	DIPSW2	(1: OFF. 0: ON)
D3	DIPSW3	
D4		{No use}
D5		
D6	AUX1C	(Active-low)
D7	AUX2X	

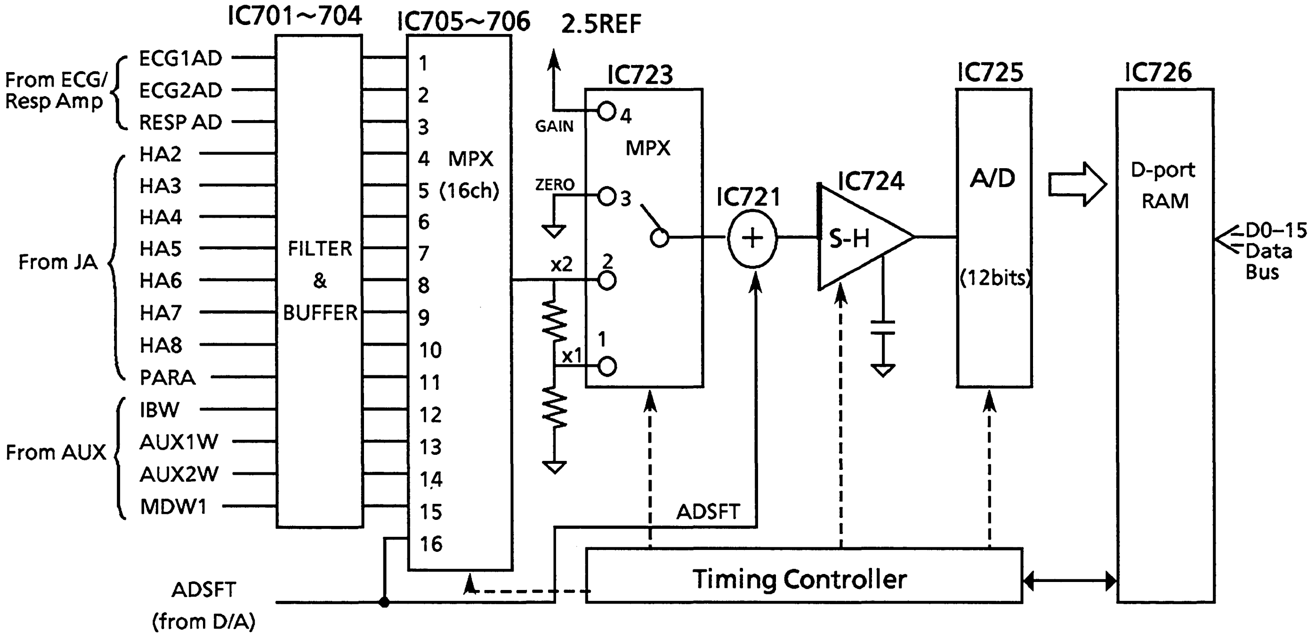
[IC603]

D0	LEDBIT0	
D1	LEDBIT1	
D2	LEDBIT2	
D3	LEDBIT3	(1: No lighting)
D4	LEDBIT4	(0: Lighting)
D5	LEDBIT5	
D6	LEDBIT6	
D7	LEDBIT7	

[IC604]

D0		No use		
D1	TEST	ECG Calibration	(1: Test.	0: Normal)
D2	INST	ECG INST	(1: ON.	0: OFF)
D3	TC3.2	ECG Time Constant	(1: 3.2s.	0: 0.5s)
D4	HUM	ECG Hum Filter	(1: ON.	0: OFF)
D5	HICUT	ECG Low-pass Filter	(1: ON.	0: OFF)
D6	RTC10	RESP Time Constant	(1: 10s.	0: 1.5s)
D7	RINST	RESP INST	(1: ON.	0: OFF)

◆ A/D Control Circuit


IC701~704
IC705~706
2.5REF
IC723
IC725
IC726
From ECG/ Resp Amp
ECG1AD
ECG2AD
RESP AD
From JA
HA2
HA3
HA4
HA5
HA6
HA7
HA8
PARA
From AUX
IBW
AUX1W
AUX2W
MDW1
FILTER & BUFFER
1
2
3
4 MPX
5 (16ch)
6
7
8
9
10
11
12
13
14
15
16
GAIN
ZERO
x2
x1
4
MPX
3
2
1
IC721
IC724
S-H
A/D
(12bits)
D-port RAM
D0–15 Data Bus
ADSFT
Timing Controller
ADSFT (from D/A)

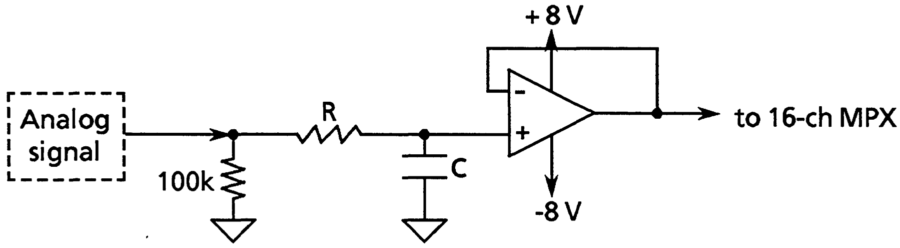
Analog signals collected from the input box or external equipment are timeshared by the 16-ch. Multiplexer through the Filter & Buffer.

The timeshared signal is sampled and held by the Sample-holder after adding a DC voltage for the base line shift (ADSFT signal from D/A converter) to the signal with the Adder through the Gain selector multiplexer.

The held signal is converted to digital signals by the 12-bit A/D converter and written into Dual-port RAM by AUTO A/D system.

• Filter & Buffer (R014~117, C101~115, IC173~176)

The low-pass filter composed of the resistor and capacitor provides the following cut-off frequency.


+8V
Analog signal
R
100k
C
-8V
to 16-ch MPX

RESP signal: 16 Hz

The others: 1.6 kHz

• 16-ch Multiplexer (IC705&706)

CH	SIGNAL	Explanation
1	ECG1AD	Output from ECG/RESP Processing circuit
2	ECG2AD	
3	RESPAD	
4	HA2	Output from Head Amplifier
5	HA3	
6	HA4	
7	HA5	
8	HA6	
9	HA7	Extra
10	HA8	
11	PARA	Parameter recognition signal
12	IBW	Interbed ECG in connecting the other BSM (ICU 7000 series)
13	AUX1W	External input
14	AUX2W	
15	MDW	Delayed ECG from COM3 board
16	ADSFT or RSSI	A/D shift voltage for inspection

• Gain Selector Multiplexer (IC723)

The multiplexer selects gain or generates +2.5 V d.c. or 0V for inspection according to the following table.

CH	Output	Function
4	2.5 V REF	for Gain adjustment
3	0V	for Offset adjustment
2	× 2	for Blood pressure wave (necessary to obtain high resolution)
1	× 1	for Other wave

• Adder (IC721)

The adder provides a base line shift function to convert each timeshared signal to digital signals at the most suitable position. The DC voltage signal for the base line shift ADSFT is generated by a 12-bit D/A converter. The function is mainly used to auto-zero the base line of blood pressure waveforms.

Shift range: within ±5 V
Resolution: by 2.5 mV

• Sample-holder (IC724)

The sample-holder samples and holds each timeshared signal to prevent the voltage level from changing during A/D conversion.

Sampling time: 10 μsec
Error: 0.01 % or less
Capacitor for holding: 1000 pF

• A/D Converter (IC725)

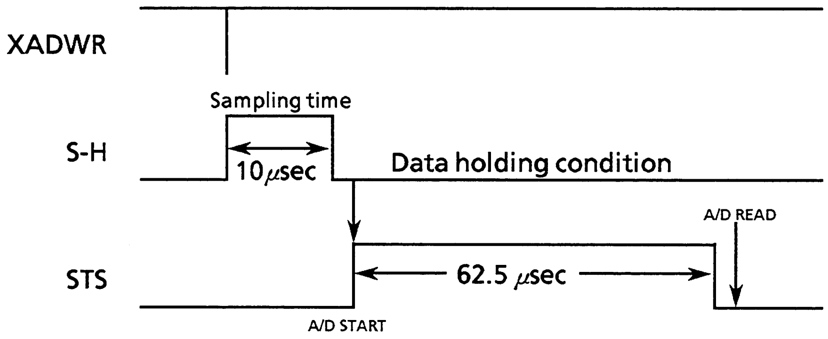
The A/D converter provides the following specifications.

[Model name: AD574]
Resolution: 12 bits
Linearity tolerance: ±1 bit
Input range: ±5.12 V (400 D/V)

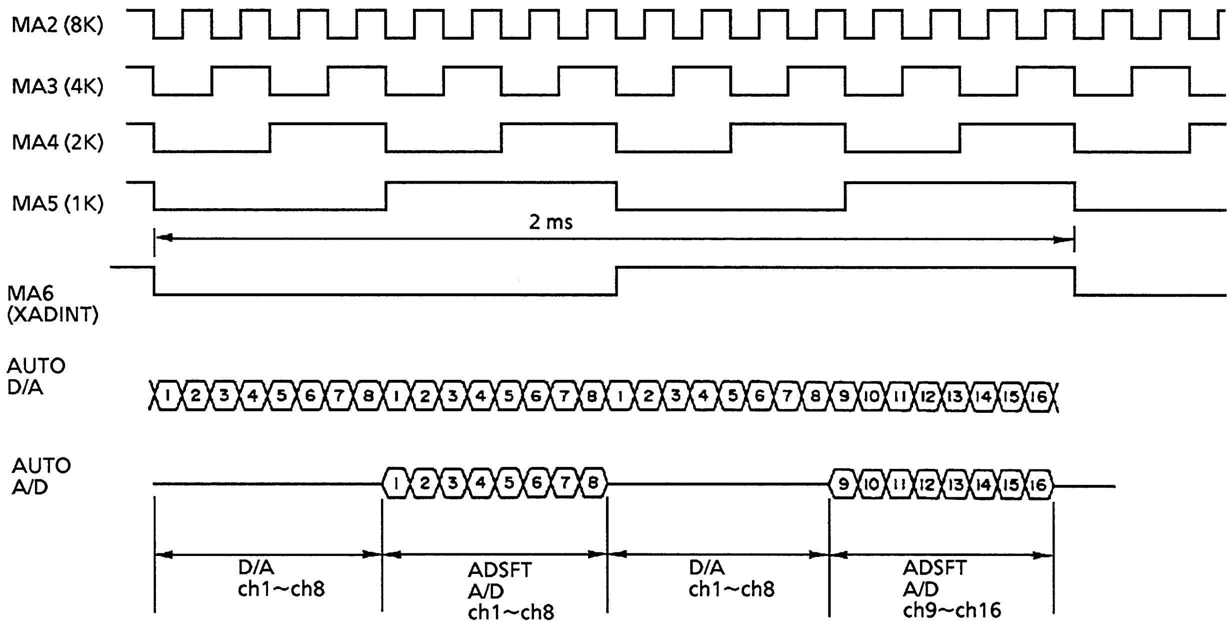
INPUT VOLTAGE	A/D OUTPUT DATA	
+5.12 V	4095 D	FFF H
+5.00 V	4048 D	FD0 H
0.00 V	2048 D	800 H
−5.00 V	48 D	30 H
−5.12 V	0 D	0 H

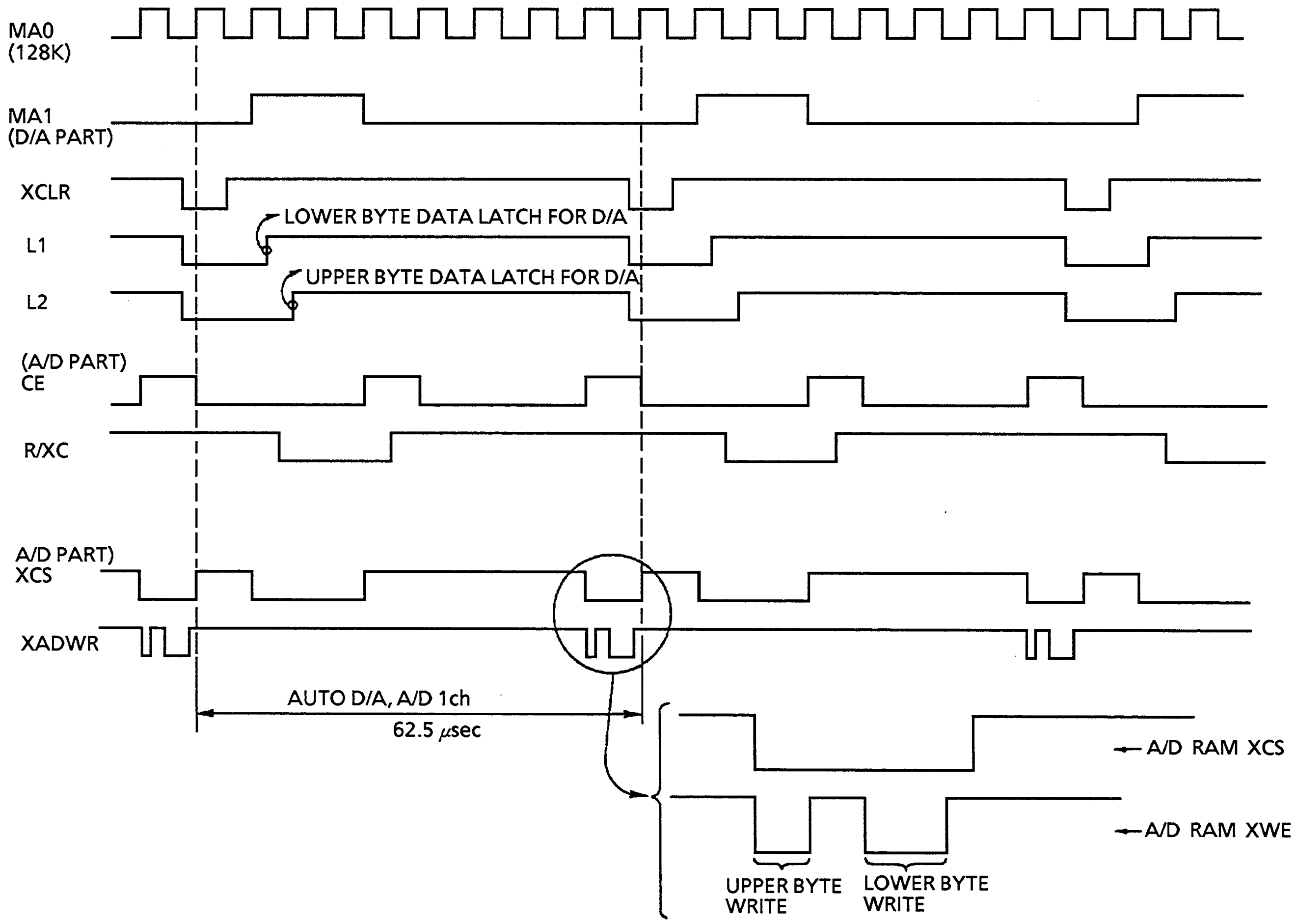
Converting time: 62.5 μsec

[Timing Chart]

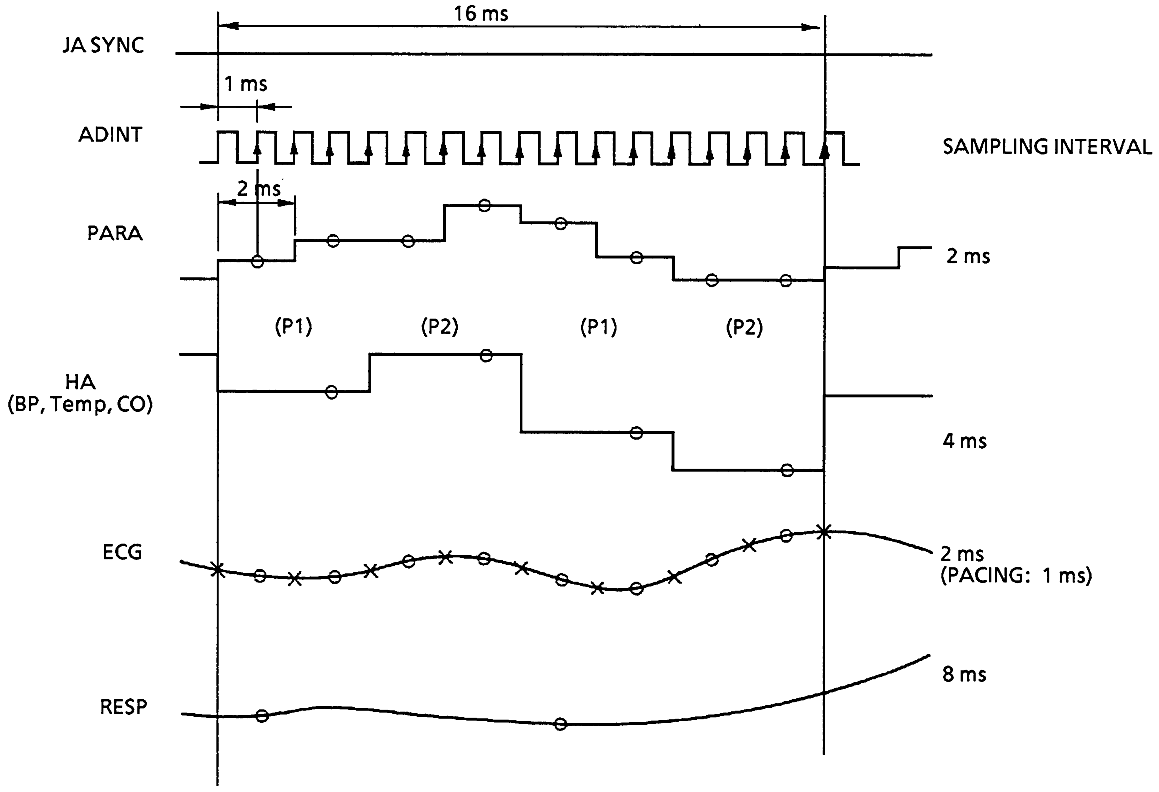

XADWR
Sampling time
S-H
10μsec
Data holding condition
A/D READ
STS
62.5 μsec
A/D START

[A/D . D/A Basic timing]: Generated by IC406

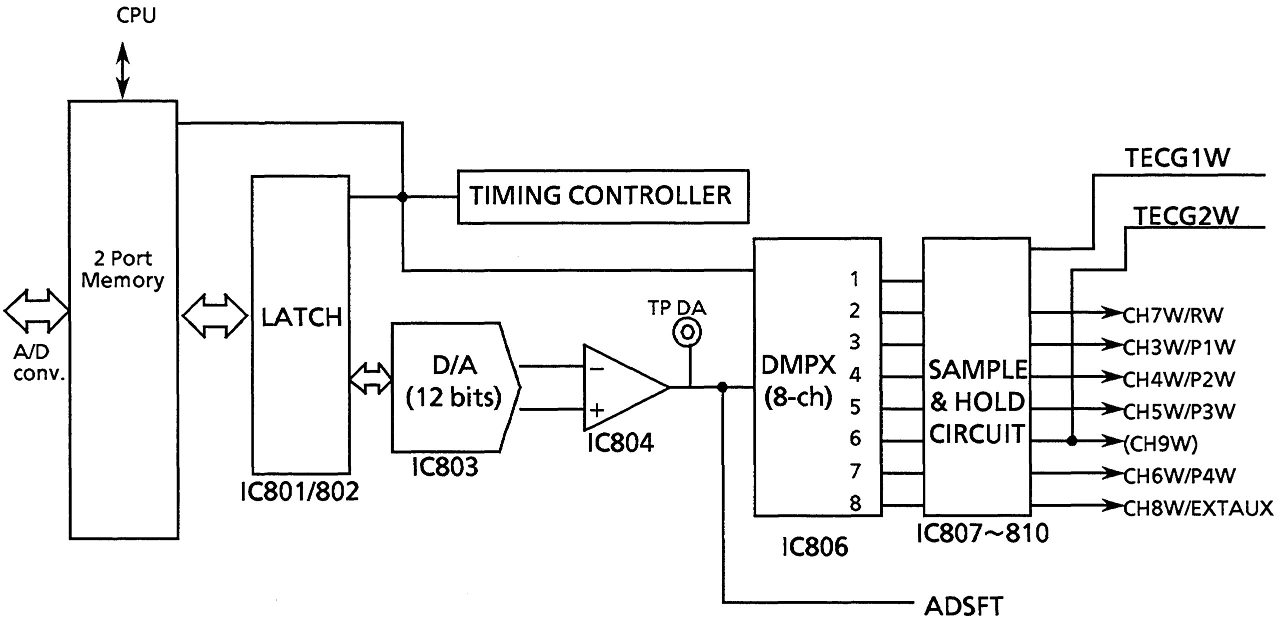

MA2 (8K)
MA3 (4K)
MA4 (2K)
MA5 (1K)
2 ms
MA6
(XADINT)
AUTO
D/A
1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
AUTO
A/D
1 2 3 4 5 6 7 8
9 10 11 12 13 14 15 16
D/A
ch1~ch8
ADSFT
A/D
ch1~ch8
D/A
ch1~ch8
ADSFT
A/D
ch9~ch16


MA0
(128K)
MA1
(D/A PART)
XCLR
L1
LOWER BYTE DATA LATCH FOR D/A
L2
UPPER BYTE DATA LATCH FOR D/A
(A/D PART)
CE
R/XC
A/D PART)
XCS
XADWR
AUTO D/A, A/D 1ch
62.5 μsec
A/D RAM XCS
A/D RAM XWE
UPPER BYTE
WRITE
LOWER BYTE
WRITE

[A/D SAMPLING TIMING CHART]


16 ms
JA SYNC
1 ms
ADINT
SAMPLING INTERVAL
2 ms
PARA
2 ms
(P1)
(P2)
(P1)
(P2)
HA
(BP, Temp, CO)
4 ms
ECG
2 ms
(PACING: 1 ms)
RESP
8 ms

◆ D/A Control Circuit


CPU
2 Port Memory
A/D conv.
LATCH
IC801/802
TIMING CONTROLLER
D/A (12 bits)
IC803
TP DA
IC804
DMPX (8-ch)
1
2
3
4
5
6
7
8
IC806
SAMPLE & HOLD CIRCUIT
IC807~810
TECG1W
TECG2W
CH7W/RW
CH3W/P1W
CH4W/P2W
CH5W/P3W
(CH9W)
CH6W/P4W
CH8W/EXTAUX
ADSFT

Data for D/A is converted by the 12-bit D/A converter through the latch (IC801&802). The D/A converted signals are distributed to each signal line by the 8-ch Demultiplexer. Channel 1 & 6 output TECG1W & 2W, and the other channels output each waveform, Respiration, Blood pressure or External input waveform.
The D/A signal is outputted synchronized with A/D conversion timing.
Each waveform signal except the Respiration wave is outputted approximately every 1msec.

- **D/A converter (IC803)**

The D/A converter provides the following specifications.

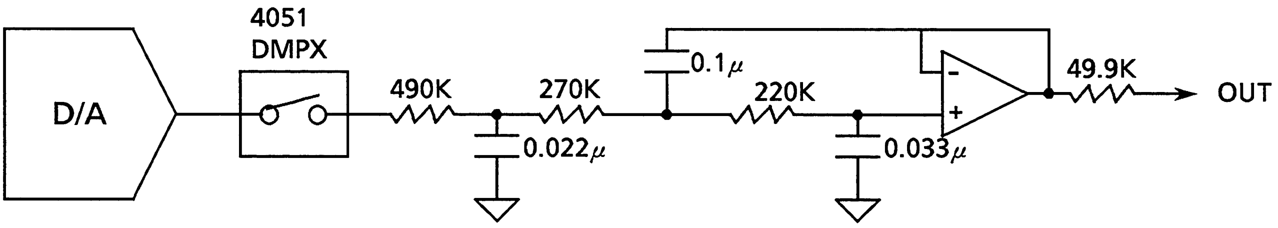
[Model name: HA-17012PB]
Resolution: 12 bits
Linearity tolerance: ±0.05 %FS (±2 bits)
Output range: ±5.12 V (1 V/400 D)
Settling time: 250 nsec

D/A INPUT DATA		D/A OUTPUT VOLTAGE
4095 D	FFF H	+5.12 V
4048 D	FD0 H	+5.00 V
2048 D	800 H	0.00 V
48 D	30 H	−5.00 V
0 D	0 H	−5.12 V

- **8-ch. Demultiplexer (IC806)**

CH	SIGNAL	Explanation
1	TECG1W	Telemetry ECG wave
2	CH7W/RW	↑
3	CH3W/P1W	
4	CH4W/P2W	
5	CH5W/P3W	Analog output to CNS
6	(CH9W)	
7	CH6W/P4W	
8	CH8W/EXTAUX	↓

- **D/A sample and hold circuit**



Sampling time: 62.5 μsec
Sampling interval: 1 msec
Holding frequency characteristic: 62.5 Hz at minimum (ECG),
31.25 Hz at minimum (Others)
Held voltage gap after 4msec: approx. 2 mV at maximum
Output range: ±5 V
Output offset voltage: ±37 mV at maximum (ECG1)
±11 mV at maximum (ECG2)
±5 mV at maximum (CH3~CH8)

◆ ECG/RESP Processing Circuit

• ECG Processing circuit

The ECG processing circuit consists of the following components.

Calibration voltage generator (15 mV to 1 V on CRT)
Pacing pulse limiter .... (1)
Time constant selector (0.5 sec or 3.2 sec)
Instantaneous short circuit in ECG lead selection
Auto-instantaneous short circuit .... (2)
Hum filter (50/60 Hz: common use)
Low-pass filter

Each ECG processing circuit in the dual ECG lead is the same.
When the hum filter is on in the monitor mode, the ECG processing circuit functions by hardware to directly pass the ECG signal to the A/D converter, not through the low-pass filter, since pacing pulse detection by software needs ECG data including high frequency component.

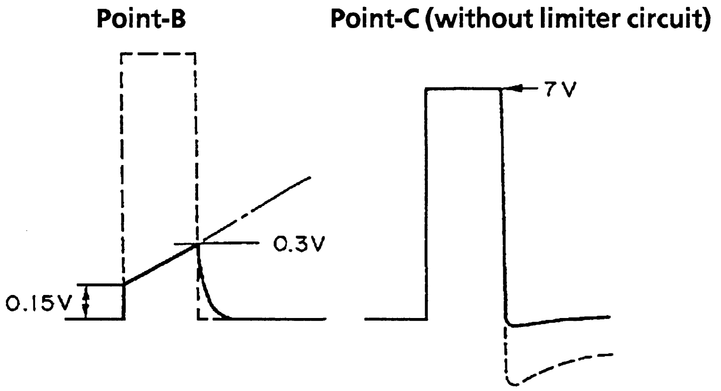
NOTE

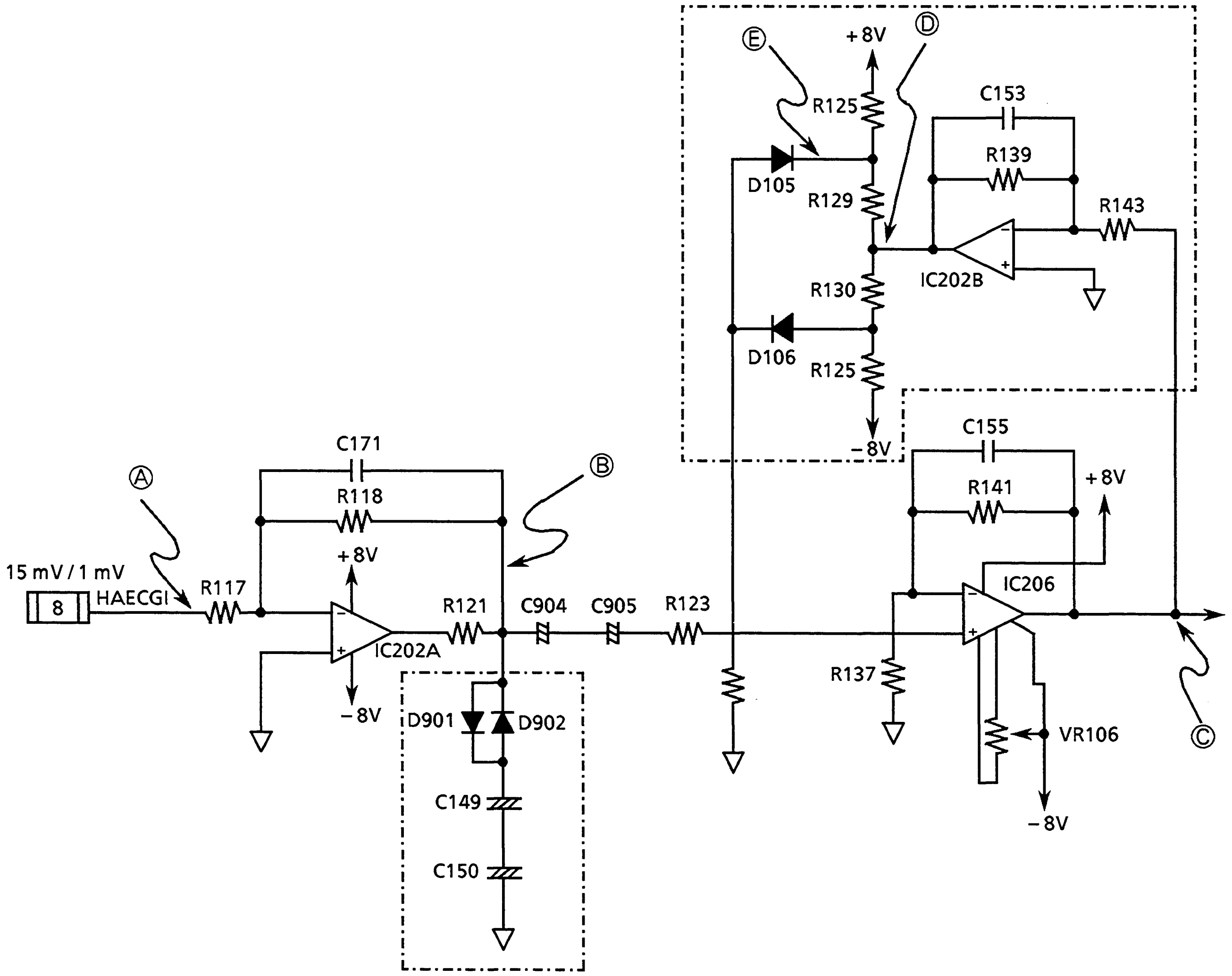
QRS detector and Pacing pulse detector which had been processed by hardware are processed by software.

1) Pacing-pulse Limiter circuit

A large amplitude signal such as a pacing pulse is limited at point-B by having either a schottky diode, D901 or D902 on while a small amplitude signal such as ECG (15 mV at the point-B to 1mV at the ECG Head Amp input) keeps both diodes D901 and D902 off (high impedance).

If the limiter circuit is removed, the large amplitude signal through the capacitors (C904/905) will make the base line shift as shown in the following figure, and the ECG wave next to every pacing pulse will not be stable on the CRT.

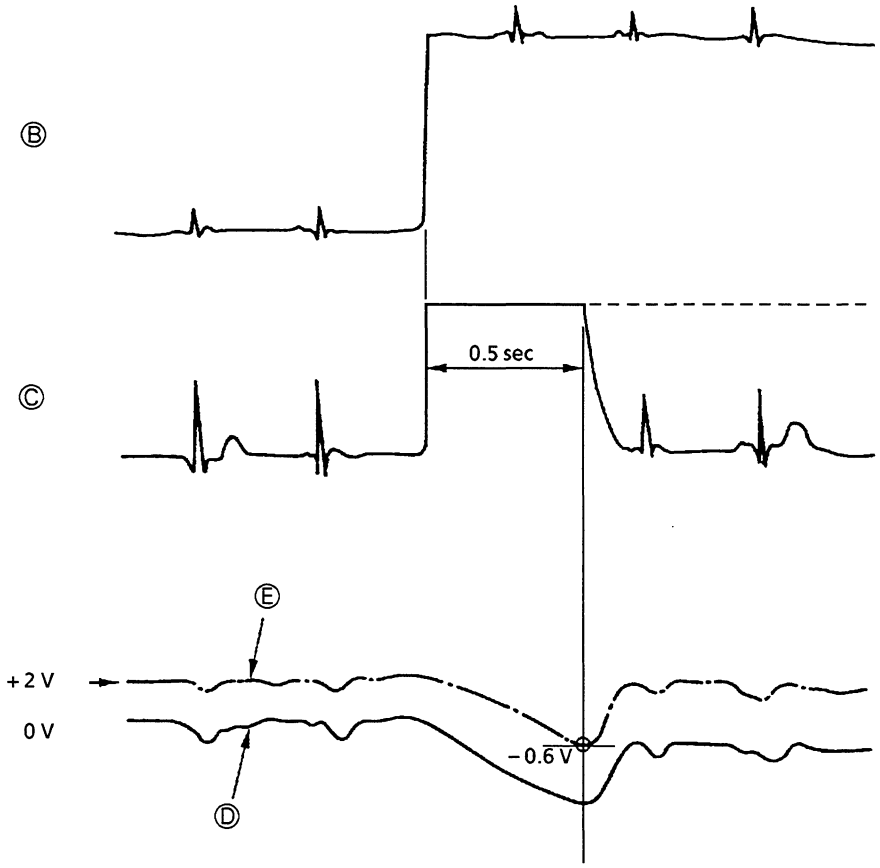

Point-B **Point-C (without limiter circuit)**


Ⓐ
15 mV / 1 mV
8
HAECGI
R117
C171
R118
+8V
-8V
IC202A
R121
Ⓑ
C904
C905
R123
D901
D902
C149
C150
Ⓔ
+8V
Ⓓ
R125
C153
R139
D105
R129
R143
IC202B
R130
D106
R125
-8V
C155
R141
+8V
IC206
R137
VR106
-8V
Ⓒ

2) Auto-instantaneous short circuit

This circuit instantaneously discharges the charged coupling capacitor (C904/905) caused by a rapid large change of an offset voltage before the ECG Head Amp input.

When the base line shifts largely upward (toward positive) at point-C due to the offset voltage change as shown in the following figure, the base line gradually shifts from the initial setting, + 2 V level toward the negative at point-E while shifting toward the negative at point-D gradually. After the 0.5 seconds from the offset voltage change, the charged capacitor (904/905) is discharged through the diode (D903) since D903 comes on. Therefore, the base line is recovered to approximately 0 V level.
When the base line largely shifts downward(toward negative) at point-C, the base line gradually shifts from the initial setting − 2 V level toward the positive at point-E while shifting toward the positive at point-D gradually. After 0.5 seconds, the C904/905 is discharged through the diode (D904) since D904 comes on. Therefore, the base line is recovered to approximately 0 V level.

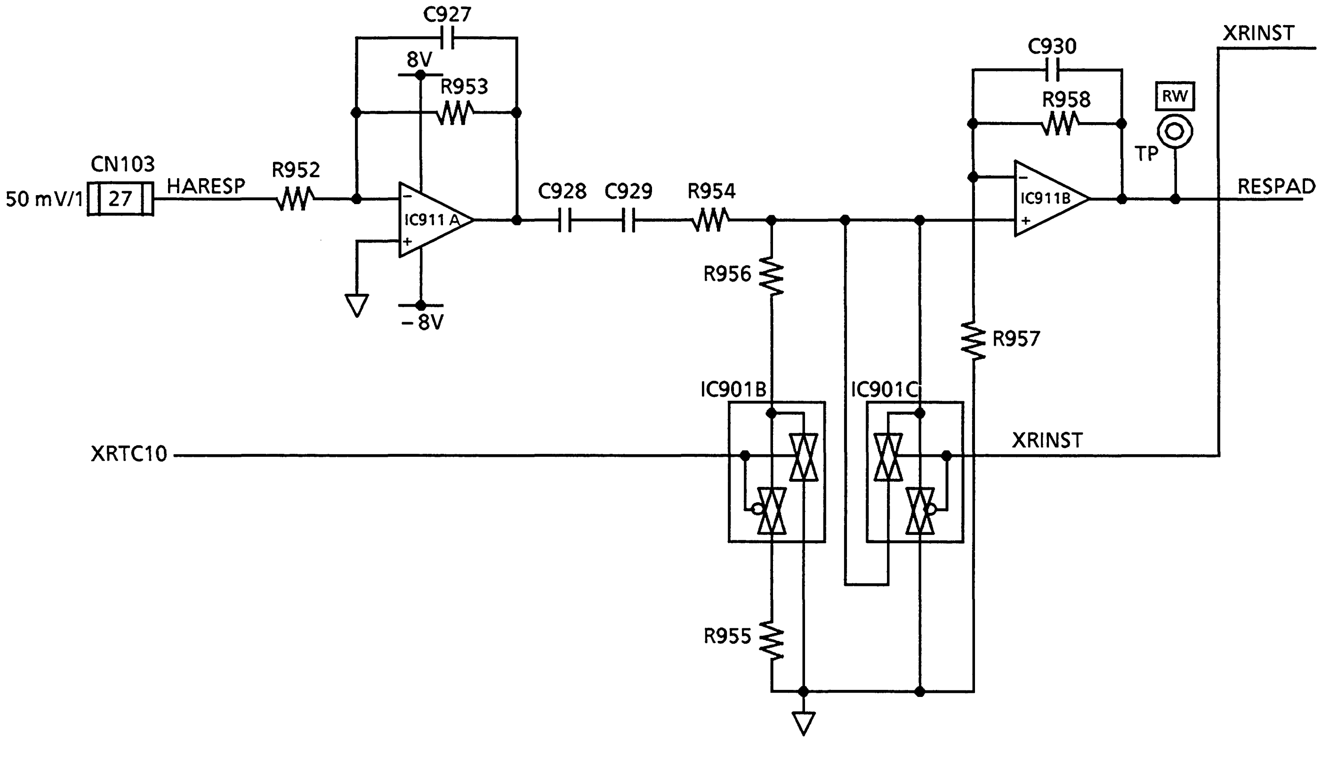


• Respiration-wave Processing circuit

The circuit consists of the following components.

20 time-inverted Amplifier (IC911A/B)
1.5/10 seconds Time constant Selector (IC901B)
Instantaneous Short circuit (IC901C)

When a respiration wave signal HARESP is deflected to the saturation level, the base line is recovered to approximately 0 V level by software.


C927
8V
R953
CN103
50 mV/1
27
HARESP
R952
IC911 A
-8V
C928
C929
R954
R956
IC901B
IC901C
XRTC10
R955
C930
R958
IC911B
R957
RW
TP
XRINST
RESPAD
XRINST

◆ JA Interface & Power Supply Circuit

This circuit generates control signals (CNTL, SYNC, FCLK, RCLK), status signal (STS) and power source for the input box .

The circuit composed of resistors (R971~974, R001, R002, DA921, DA922) is a protection circuit.

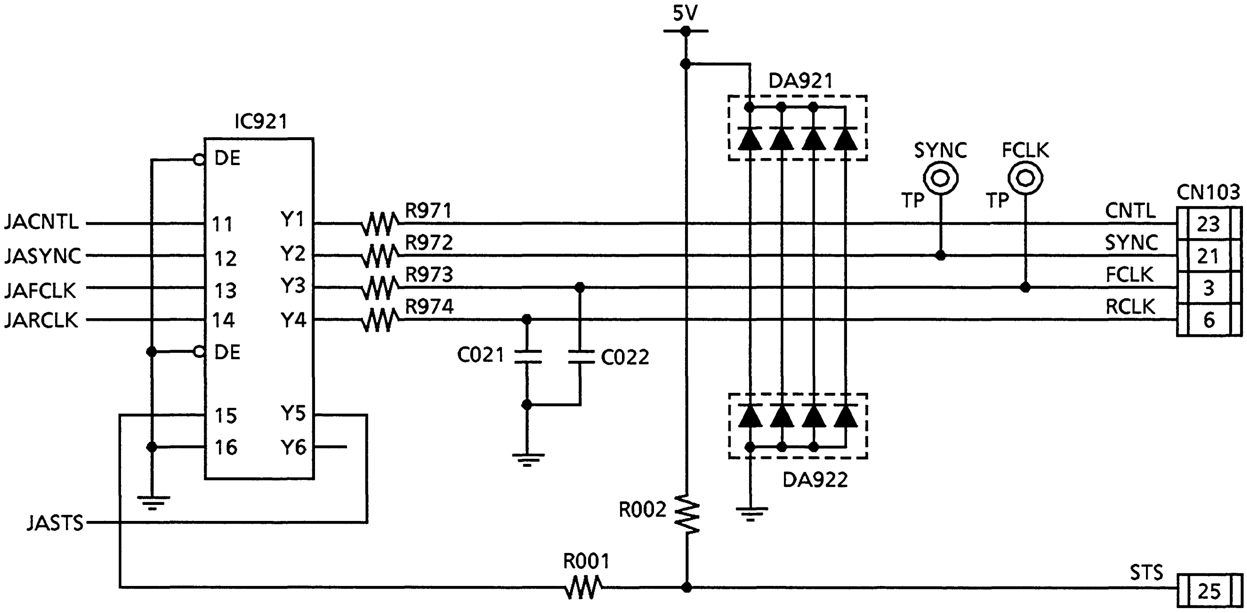
The buffer (IC213) functions to the control and status signals.

The capacitor (C132/133) is a low-pass filter component to allow the ringing on the clock pulses (FCLK,

RCLK) to be ignored.

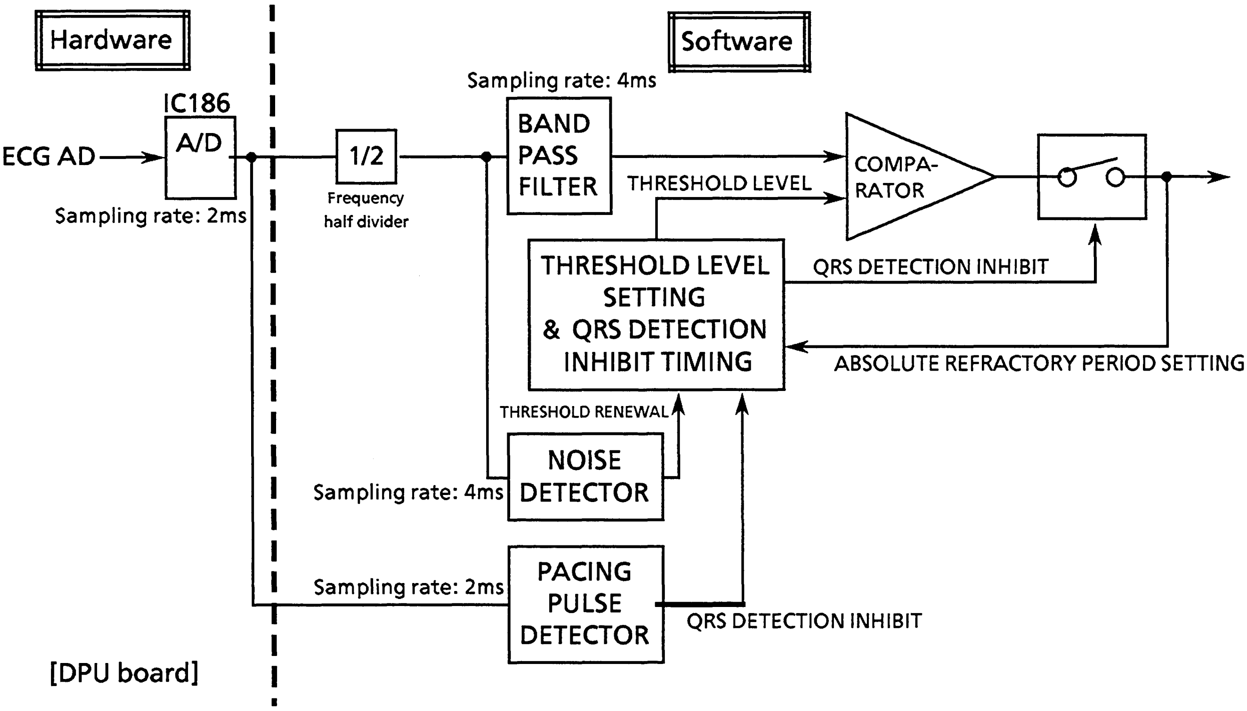
The power source supples the input box with ±8 V and +21 V.

The ground terminals, E1(for ±8 V) and EH/EHC/ER(for +21 V), are shorted to the analog signal ground AGND (for ±15 V, A/D and D/A converter power source).


5V
DA921
IC921
DE
JACNTL
JASYNC
JAFCLK
JARCLK
11
12
13
14
Y1
Y2
Y3
Y4
DE
15
16
Y5
Y6
R971
R972
R973
R974
C021
C022
SYNC
FCLK
TP
TP
CN103
CNTL
SYNC
FCLK
RCLK
23
21
3
6
DA922
JASTS
R002
R001
STS
25

◆ Software Data Process [Hardwire system]

(1) ECG Data process


Hardware
Software
IC186
A/D
ECG AD
Sampling rate: 2ms
1/2
Frequency half divider
Sampling rate: 4ms
BAND PASS FILTER
THRESHOLD LEVEL
COMPA-RATOR
THRESHOLD LEVEL SETTING & QRS DETECTION INHIBIT TIMING
QRS DETECTION INHIBIT
ABSOLUTE REFRACTORY PERIOD SETTING
THRESHOLD RENEWAL
NOISE DETECTOR
Sampling rate: 4ms
PACING PULSE DETECTOR
Sampling rate: 2ms
QRS DETECTION INHIBIT
[DPU board]

● Definition

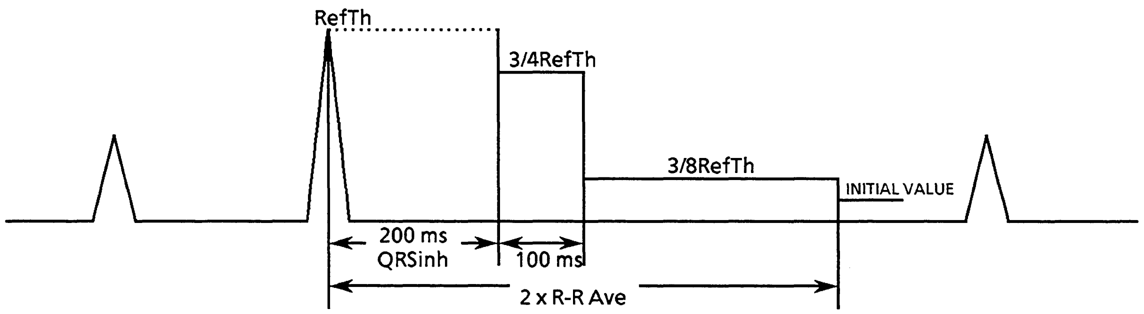
Sampling data through QRS band pass filter is defined as Reference Threshold level "RefTh" when a QRS is detected.

Another QRS detection is inhibited for 200 msec after detecting a QRS. The 200msec is defined as the Absolute Refractory period, "QRSinh".

The threshold level is changed according to the elapse time so as to detect the next QRS after the 200msec.

The threshold level data is defined as "HighTh".

Averaged R-R interval out of 4 beats is defined as "R-R Ave".


RefTh
3/4RefTh
3/8RefTh
INITIAL VALUE
200 ms
QRSinh
100 ms
2 x R-R Ave

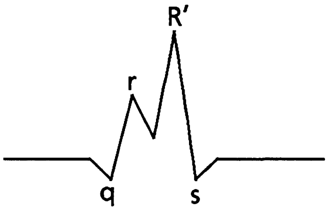
● Threshold level renewal

When the next QRS is not detected, the threshold level is changed as follows:

During QRSinh: Data inhibit
For 100msec after QRSinh: 3/4 RefTh
From the time after the 100msec to 2 x R-R Ave: 3/8 RefTh
From 2 x R-RAve to 2sec after detecting the last QRS: Initial value

When sampling data through the band-pass filter is larger than RefTh during the same QRSinh, the RefTh data is renewed with the sampling data to be the threshold level for the next QRS.

[EXAMPLE QRS]



● QRS Band-pass filter

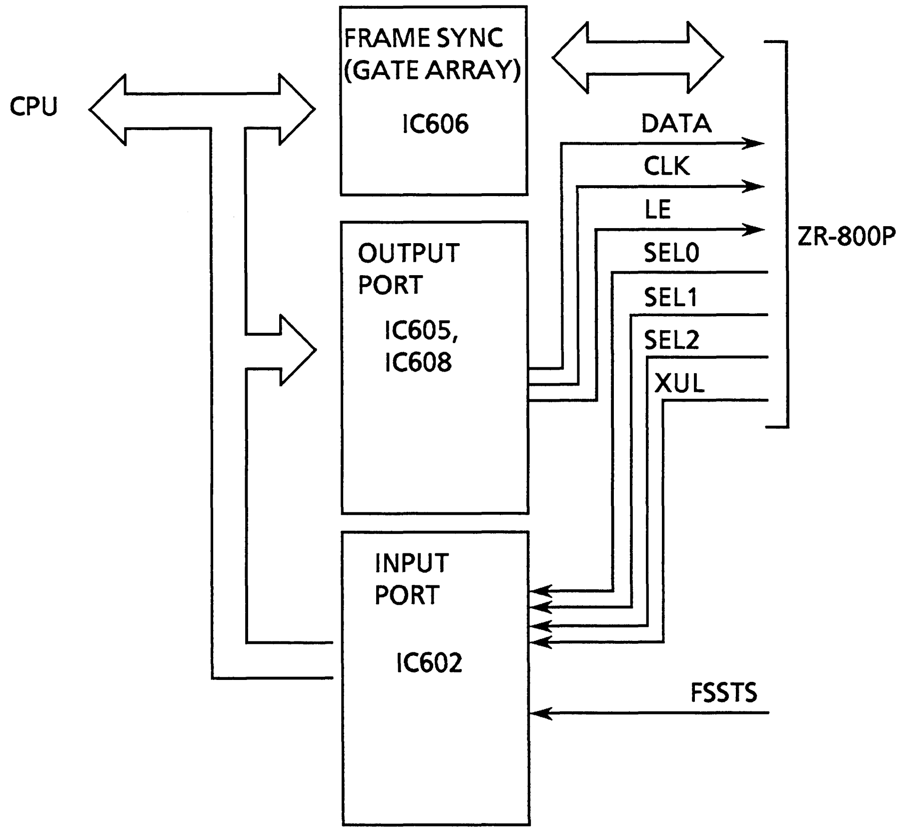
The band-pass filter consists of a low-pass filter and high-pass filter. The frequency characteristic is 8 to 20 Hz.

● QRS Detection

When 2 units of continuous sampling data or more through the filter exceeds HighTh during QRS detection enable period, the sampling data is detected and counted as a QRS.

◆ Digital Telemetry Signal Processor

Interface on DPU board for digital telemetry receiver consists of following block diagram.


CPU
FRAME SYNC
(GATE ARRAY)
IC606
OUTPUT
PORT
IC605,
IC608
INPUT
PORT
IC602
DATA
CLK
LE
SEL0
SEL1
SEL2
XUL
FSSTS
ZR-800P

IC606 receives the serial data from the receiver and converts the data to parallel one. Then it is transferred to CPU.

IC606

Signal symbol	Function	
RD	Input data in serial	Input signal
RT	Synchronization clock for input data in serial	Input signal

IC 605 is an output port latch device and outputs the receiving channel setting data to the CPU .

IC605

Pin	Signal symbol	Function	
D0	DATA	Output data	Output signal
D1	CLK	Clock for output data	Output signal
D2	LE	Latch enable signal	Output signal

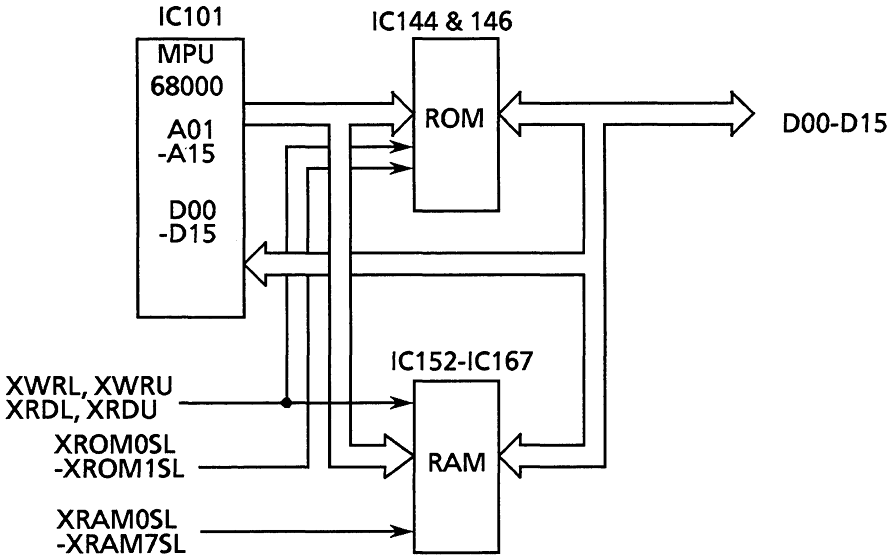
IC602 functions as an input port and inputs the condition information of the receiver to the CPU.

IC602

Pin	Signal symbol	Function	
D0	SEL0	Shows the values of DIG switch in the receiver (ZR-800P)	Input signal
D1	SEL1		Input signal
D2	SEL2		Input signal
D3	XUL		Input signal
D4	FSSTS	Asserts every 8ms	Input signal

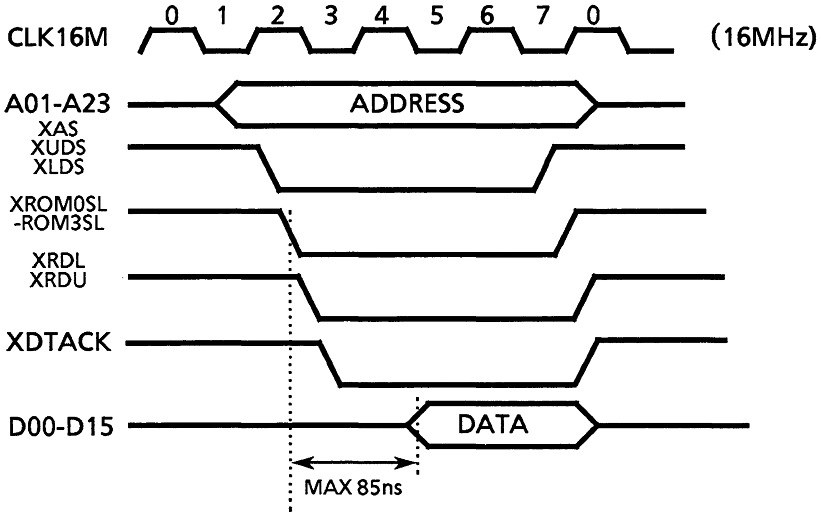
3-2-6 CPU Board, UR-3027

◆ MPU/ROM/RAM Circuit


IC101
MPU
68000
A01
-A15
D00
-D15
IC144 & 146
ROM
D00-D15
IC152-IC167
RAM
XWRL, XWRU
XRDL, XRDU
XROM0SL
-XROM1SL
XRAM0SL
-XRAM7SL

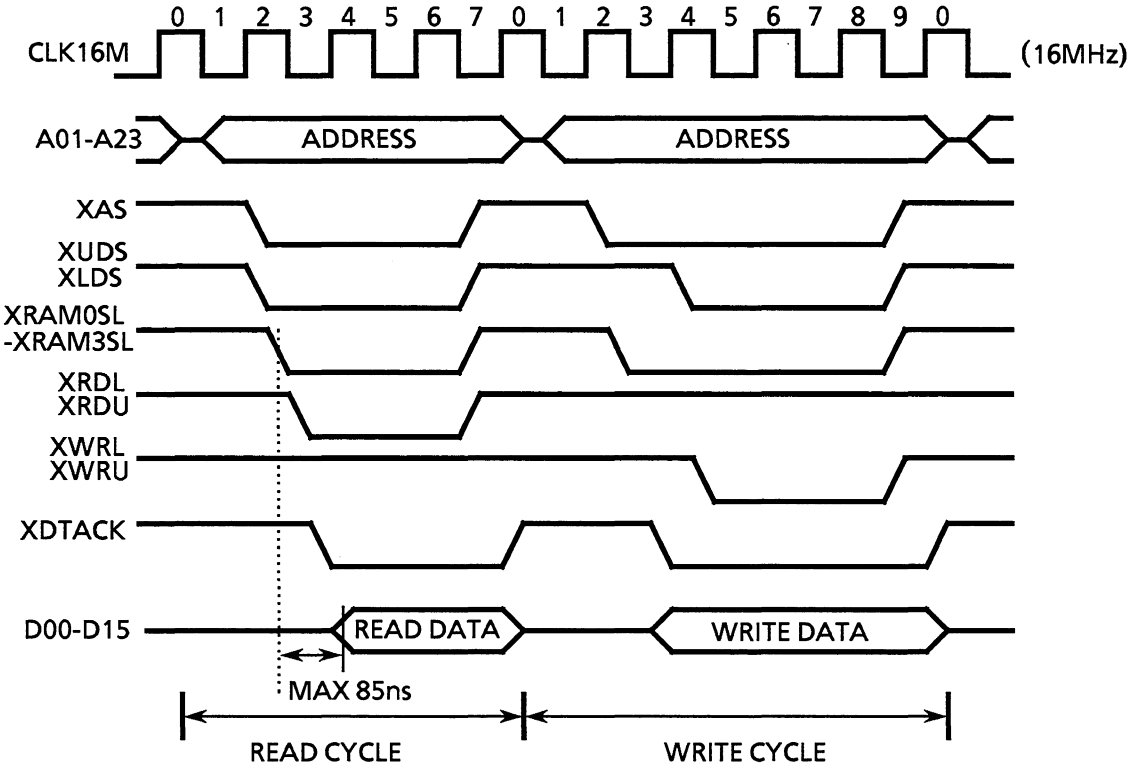
The Micro Processor Unit MPU[68000] (IC101) accesses ROMs (IC144 & 146) or RAMs (IC152-167) as follows:

[ROM ACCESS TIMING CHART]


CLK16M
0 1 2 3 4 5 6 7 0
(16MHz)
A01-A23
ADDRESS
XAS
XUDS
XLDS
XROM0SL
-ROM3SL
XRDL
XRDU
XDTACK
D00-D15
DATA
MAX 85ns

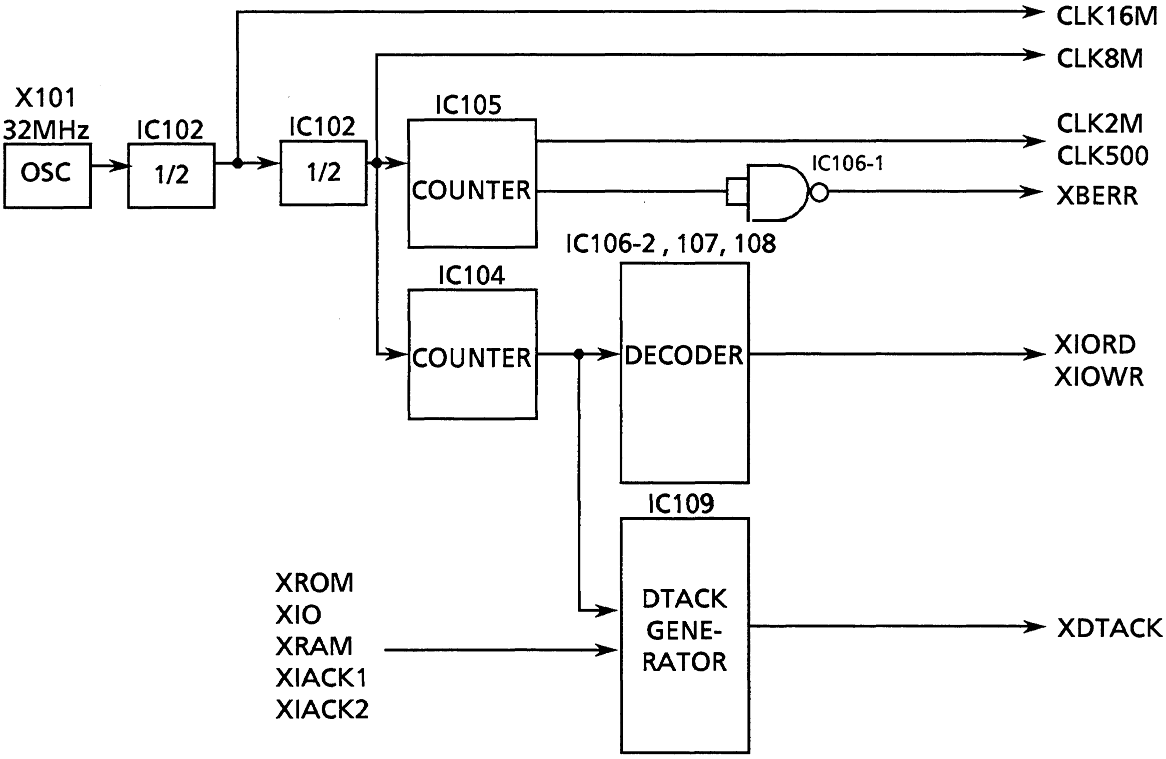
The ROM provides 128kbit memory and 85ns access time. The total memory capacity of the ROMs is 512kwords.

[RAM ACCESS TIMING CHART]


0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 8 9 0
CLK16M
(16MHz)
A01-A23
ADDRESS
ADDRESS
XAS
XUDS
XLDS
XRAM0SL
-XRAM3SL
XRDL
XRDU
XWRL
XWRU
XDTACK
D00-D15
READ DATA
WRITE DATA
MAX 85ns
READ CYCLE
WRITE CYCLE

The RAM provides 32kbit memory and 85ns access time.

◆ Timing Control Circuit


X101
32MHz
OSC
IC102
1/2
IC102
1/2
IC105
COUNTER
IC106-1
IC106-2, 107, 108
IC104
COUNTER
DECODER
IC109
DTACK GENE-RATOR
XROM
XIO
XRAM
XIACK1
XIACK2
CLK16M
CLK8M
CLK2M
CLK500
XBERR
XIORD
XIOWR
XDTACK

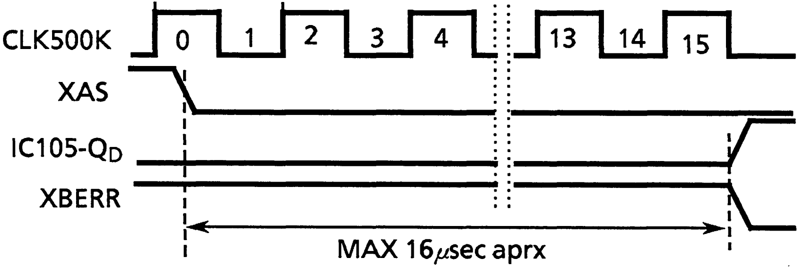
The above circuit generates clock signals, Read/Write Control signals, and Data Transfer Acknowledge signals. Moreover, the circuit provides a Bus Error Detector (IC105,106-1).

● Bus Error Detector

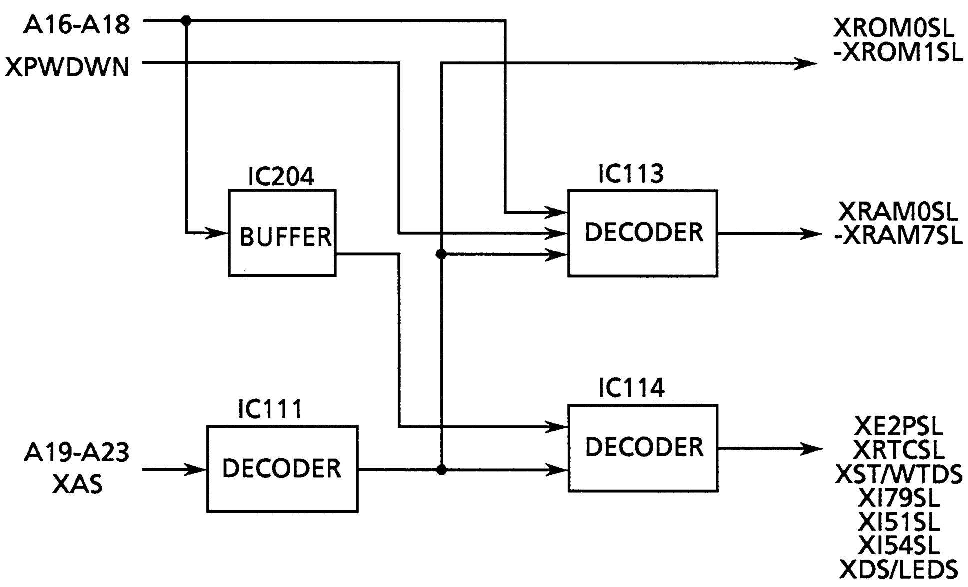
The detector informs the MPU (IC101) on this board of any trouble found in the bus cycle during an execution. If Address Strobe signal XAS is not negated on Counter (IC105-2) within16μsec due to the following condition, Bus Error signal XBERR is outputted to the MPU through the IC106-1.

DTACK signal is not asserted.

VPA signal is not asserted.


2μsec
CLK500K
0
1
2
3
4
13
14
15
XAS
IC105-QD
XBERR
MAX 16μsec aprx

◆ Address Decoding Circuit

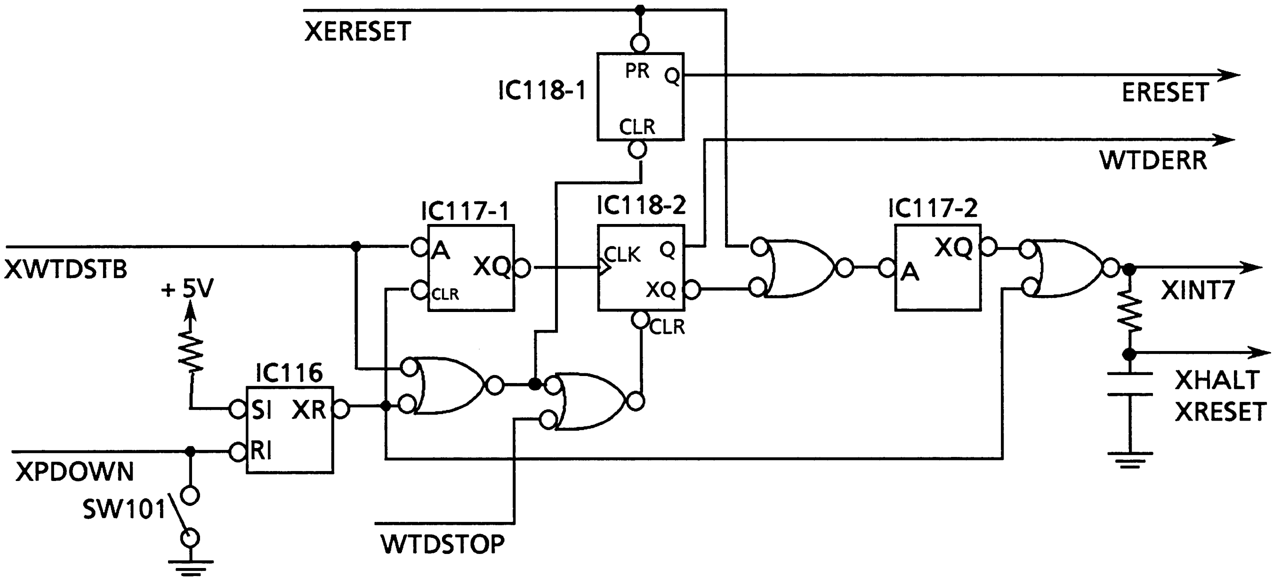

A16-A18
XPWDWN
IC204
BUFFER
IC113
DECODER
XROM0SL
-XROM1SL
XRAM0SL
-XRAM7SL
IC111
DECODER
A19-A23
XAS
IC114
DECODER
XE2PSL
XRTCSL
XST/WTDS
XI79SL
XI51SL
XI54SL
XDS/LEDS

IC111 generates ROM selection signals XROM0SL-3SL.

IC113 generates RAM selection signals XRAM0SL-7SL.

IC114 generates the other I/O chip selection signals.

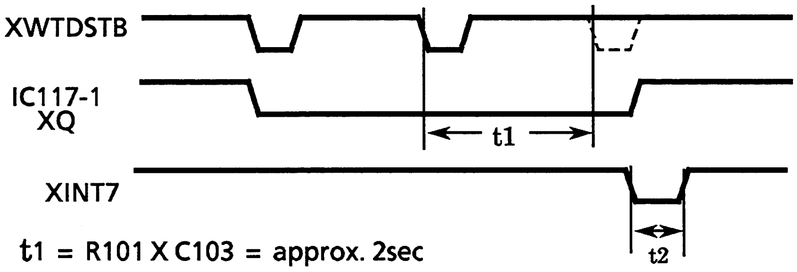
◆ Reset/Watch Dog Timer/Power Down Detector Circuit


XERESET
IC118-1
PR
Q
CLR
ERESET
WTDERR
IC117-1
IC118-2
IC117-2
XWTDSTB
A
XQ
CLR
CLK
Q
XQ
CLR
A
XQ
XINT7
+5V
IC116
SI
XR
RI
XHALT
XRESET
XPDOWN
SW101
WTDSTOP

● Reset circuit

When external reset signal XERESET is asserted by pressing the SELF CHECK key on the operation panel, the following signals are generated. The output (Q) on External Reset Status Flip Flop (IC118-1) is set to high, assertion of ERESET signal. Interrupt request signal to MPU (IC101), XINT7 is asserted for 50μsec. Reset signal to MPU (IC101), XRESET (XHALT) is asserted for 50μsec after 10μsec delay from XINT7 assertion.

● Watch Dog Timer circuit


XWTDSTB
IC117-1
XQ
t1
XINT7
t2

t1 = R101 X C103 = approx. 2sec

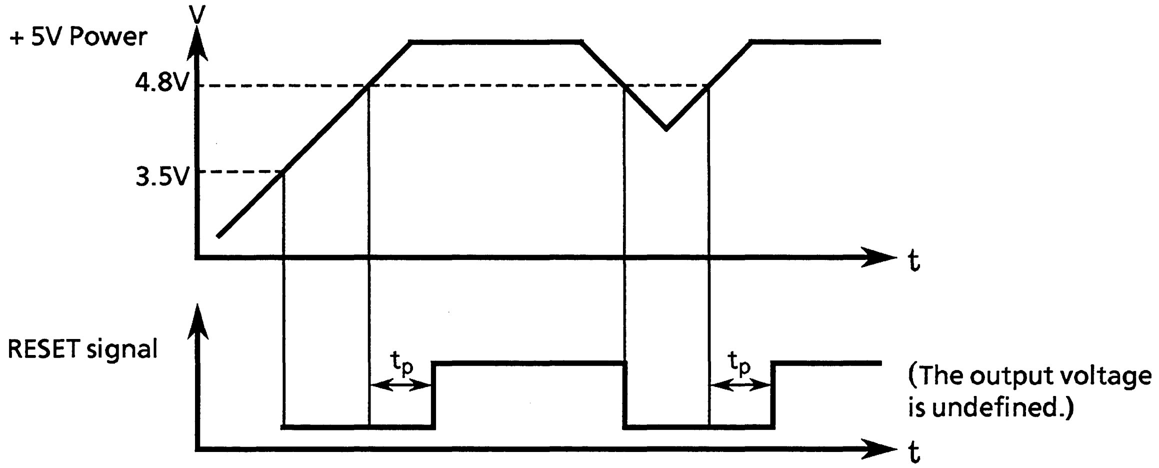
t2 = (RA109-5) X C104 = 47μsec

If MPU (IC101) runs away, this circuit resets the MPU as follows:
Under normal conditions, the output (XQ) on One-shot multi. (IC117-1) keeps low since IC117-1 receives the Watch Dog Strobe signal from MPU XWTDSTB within 2sec. However, under abnormal conditions, XQ on IC117-1 is changed to high since IC117-1 does not receive XWTDSTB signal. The following signals are generated.
The output (Q) on Watch Dog Timer Error Status F/F (IC118-2) is set to high (assertion of WTDERR signal).

XINT7 signal is asserted for 50 μsec.

XRESET (XHALT) is asserted for 50 μsec after a 10 μsec delay from XINT7 assertion.

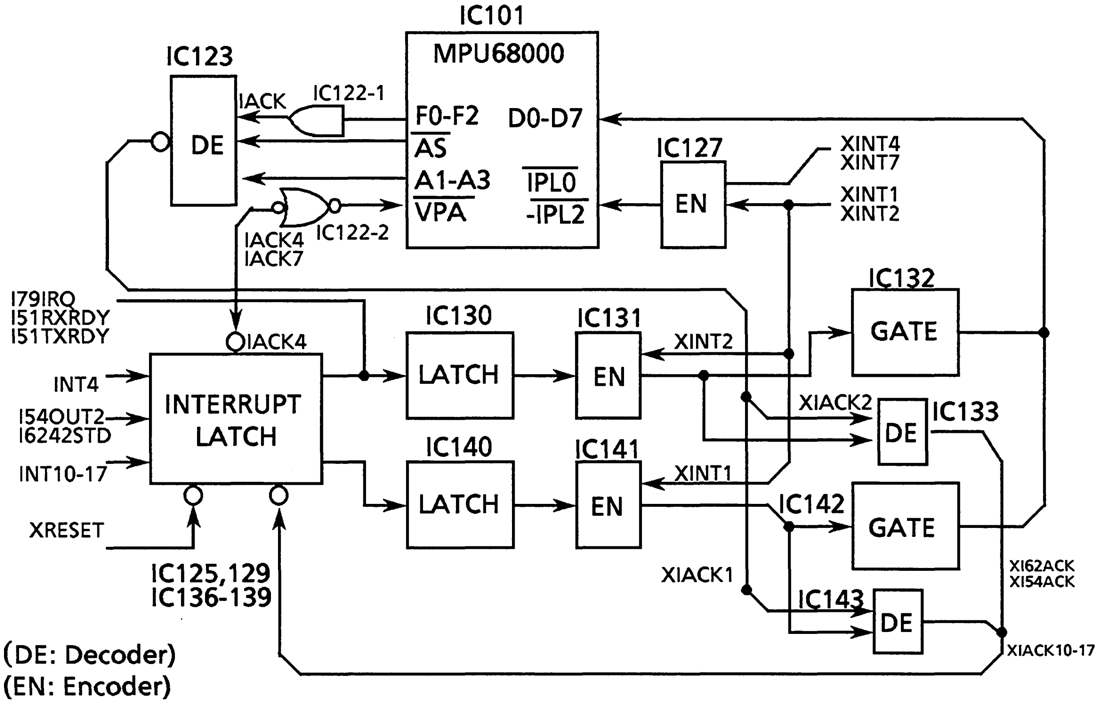
• Power Down Detecting circuit


V
+ 5V Power
4.8V
3.5V
t
RESET signal
t_P
t_P
(The output voltage is undefined.)
t

(t_P : 200msec, Additional time for Reset condition)

If the +5 V power changes to 4.8 V or less in Power Down signal, the Power Down detector (IC116) generates reset signal (active-low) for IC118-1& 2 until 200msec passes after the +5 V power returns to 4.8V.
When the power is turned on, IC116 keeps reset signal until 200msec passes after the +5V power comes to 4.8V.
In the both cases, INT7 signal is asserted for 50μsec. and XRESET signal is also asserted for 50 μsec after 10 μsec delay from XINT7 assertion.
When the switch (SW101) is turned on, the reset input (RI) on IC116 is set to active-low.

◆ Interrupt Control Circuit


IC101
MPU68000
IC123
DE
IACK
IC122-1
F0-F2
D0-D7
AS
A1-A3
VPA
IPL0
-IPL2
IC122-2
IACK4
IACK7
IC127
EN
XINT4
XINT7
XINT1
XINT2
IC132
GATE
I791RQ
I51RXRDY
I51TXRDY
IACK4
INT4
I54OUT2
I6242STD
INT10-17
INTERRUPT
LATCH
XRESET
IC130
LATCH
IC131
EN
XINT2
XIACK2
IC133
DE
IC140
LATCH
IC141
EN
XINT1
IC142
GATE
XIACK1
IC143
DE
XI62ACK
XI54ACK
XIACK10-17
IC125,129
IC136-139
(DE: Decoder)
(EN: Encoder)

The interrupt request signals are divided into Auto-vectored interrupt and Vectored interrupt while being divided into seven levels according to the following table. Level-7 provides the highest priority.

INTERRUPT PRIORITY	VECTOR NUMBER	INTERRUPT REQUEST SIGNAL	EXPLANATION	GENERATED IN
7	Auto	XPDOWN WTDERR XERESET	Power down Watch dog External reset	CPU board
6			Not used	
5			Not used	
4	Auto	INT40	CRTC Frame synchronizing (16msec)	CRTC board
3	Auto	INT30	For keypad's 72001	I/O board
2	4D 4C 4B 4A 49	16242STD 154OUT2 151TXRDY 151RXRDY 1791RQ	Real time (1sec) 71054 OUT2 (10msec) RS232CT$_{X}$RDY RS232CR$_{X}$RDY Key-in	CPU board
1	47 46 43 41	INT17 INT16 INT13 INT11	Interrupt for VD (72001) Interrupt from COM3 Interrupt from DPU Interrupt for WS recording	I/O board COM3 board DPU board COM3 board

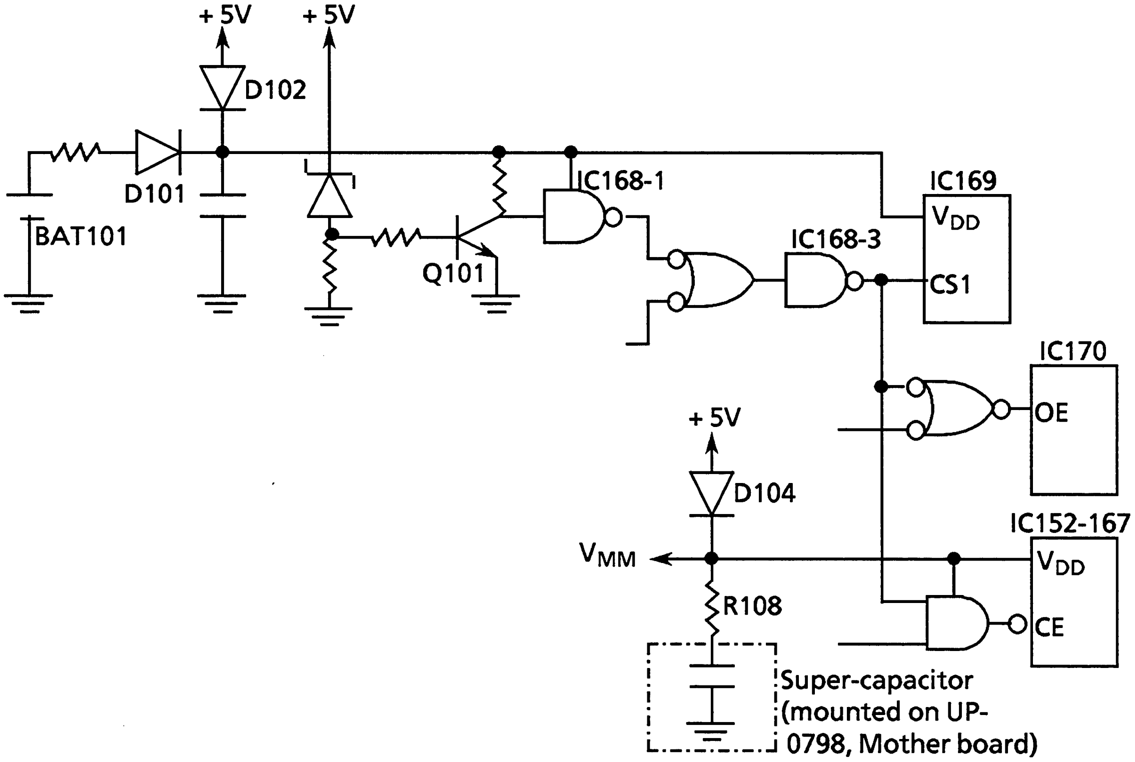
- **Auto-vectored Interrupt**

The Interrupt is processed by using a vector generated in the MPU. The interrupt request signal INT4 or INT7, is inputted to the Interrupt Control terminals, IPL0-2 on the MPU through Interrupt Latch (IC125) or Priority Encoder (IC127).
The IC125 latches an INT4 signal by triggering the positive-going edge of the signal and resets the output with XRESET or Interrupt Acknowledge signal IACK.
The IC127 generates the interrupt request to the IPL0-2 on the MPU whenever a higher interrupt priority level than before is inputted.
The IC122-1, IC123 and IC122-2 generate Interrupt Acknowledge signals, IACK and XIACK1/2 and Auto-vector recognition signal XVPA.

- **Vectored Interrupt**

The interrupt is processed by acquiring a vector number from the others by the MPU.
The interrupt level signal, XINT1 or XINT2, is inputted to IPL0-2 on the MPU through the Priority encoder (IC127). An interrupt request signal is changed to vector number signal (D0-7) through IC129/136-139, IC130/140, IC131/141 and Gate (IC132 /142).
The AND (IC122-1) and Decoder (IC123,133/143) generates interrupt acknowledge signals.
The Interrupt latch (IC129,136-139) resets the output by triggering the positive-going edge of the XRESET signal or each interrupt acknowledge signal.
The IC132/142 generates the vector number according to an interrupt request signal and then the vector number is acquired by the MPU.

◆ **Real Time Clock (RTC)/Battery/EEPROM**



• RTC

The real time clock IC (IC169) can be read or written by the MPU from second to year. IC169 provides four data lines, four address lines, three control lines and two lines of chip select signal for communication with the MPU.

IC169 provides real time setting or modification or readout function.

•Battery & Super-capacitor

The lithium battery (BAT101) provides a backup power function to prevent a data break in IC169 due to a power failure. The BAT101 supplies the IC169 through D101 with the +3 V power instead of the +5 V power when the +5 V power is lower than the battery power.

The super-capacitor (C101,102) mounted on the mother board (UP-0798) is always charged by the +5V power. The super-capacitor provides a backup function to prevent a data break in Static RAMs (IC152-167) when power fails. The super-capacitor supplies the Static RAMs through D104 with the charged power instead of the +5 V power when the +5 V power is lower than the charged power.

When the +5 V power starts to drop, the transistor (Q101) reaches cut-off condition and NAND IC (IC168-3) outputs low (0 V) through IC168-1, 2. Therefore, IC169, IC152-167 and IC170 work as follows:

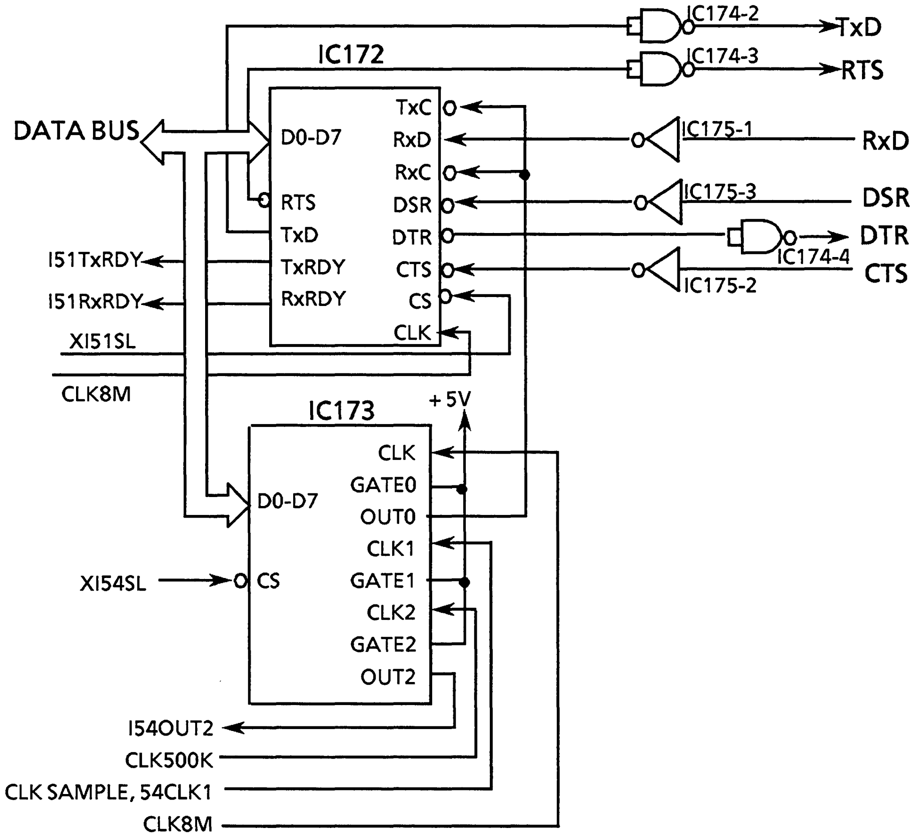
IC169:	The write mode is disabled since chip select terminal CS1 is set to Low, negation.
IC152-167:	The write mode is disabled since chip enable terminal CE is set to High, negation.

IC170: When the power is within 3.0 V to 4.85 V, the write mode is disabled since output enable terminal OE is set to Low, assertion. When the power is between 0 to 3 V, the write mode is disabled owing to itself.

• EPROM

The Electrically Erasable Programmable ROM (IC170), HN58C65, provides 8kbyte memory capacity and 250nsec access time.

◆ RS232C Control Circuit


IC174-2
TxD
IC172
IC174-3
RTS
DATA BUS
D0-D7
TxC
RxD
RxC
RTS
DSR
TxD
DTR
TxRDY
CTS
RxRDY
CS
CLK
IC175-1
RxD
IC175-3
DSR
DTR
IC174-4
CTS
IC175-2
I51TxRDY
I51RxRDY
XI51SL
CLK8M
IC173
+5V
CLK
GATE0
D0-D7
OUT0
CLK1
XI54SL
CS
GATE1
CLK2
GATE2
OUT2
I54OUT2
CLK500K
CLK SAMPLE, 54CLK1
CLK8M

• Serial Inter-Face Controller (IC172), µPD71051C

The following items are controlled by software.

Baud rate:	1200, 2400 or 9600 bits/sec
Data length:	7 or 8 bits
Number of Stop bit:	1 or 2 bits
Operation mode:	Synchronizing or Asynchronizing mode
Parity bit:	Even or Odd

*** Transmitting operation**

When a parallel data is inputted at D0-7 on IC172, the data is converted to serial format data. The serial data is transmitted from Transmit Data terminal TxD. When the data transmission is completed, Transmitter Ready terminal TxRDY is set to High so as to interrupt the MPU operation and wait for the next parallel data.

*** Receive operation**

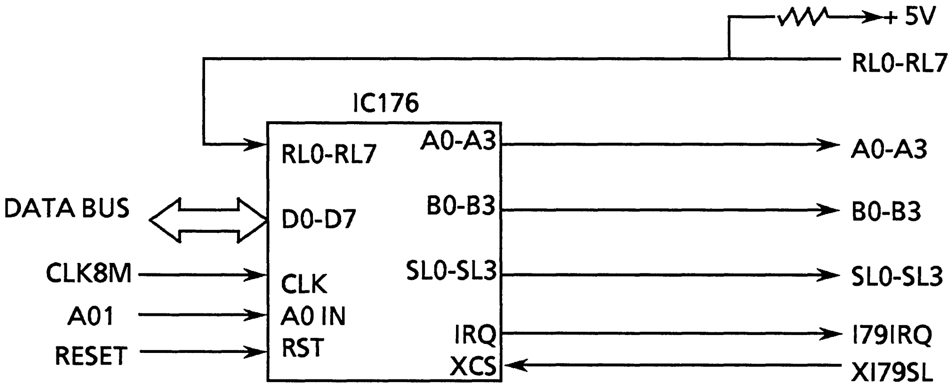
When a serial format data is received at Receive Data terminal RxD, the data is converted to parallel data for the MPU. When the data reception is completed, Receive Ready terminal RxRDY is set to High so as to interrupt MPU operation and request the reception of the parallel data to the MPU.

• Programmable Interval Timer (IC173), µPD71054C

The IC173 consists of three sets of 16-bit counters controlled by software. The IC173 is used for the following purpose.

- to control baud rate for RS232C communication
- to generate periodic interrupt to the MPU (10 msec interval)
- to synchronize data transfer timing with wave display timing on CRTC board (UP-0262) by counting 8 msec interval clock, I54CLK1.

◆ Key/Sound Control Circuit

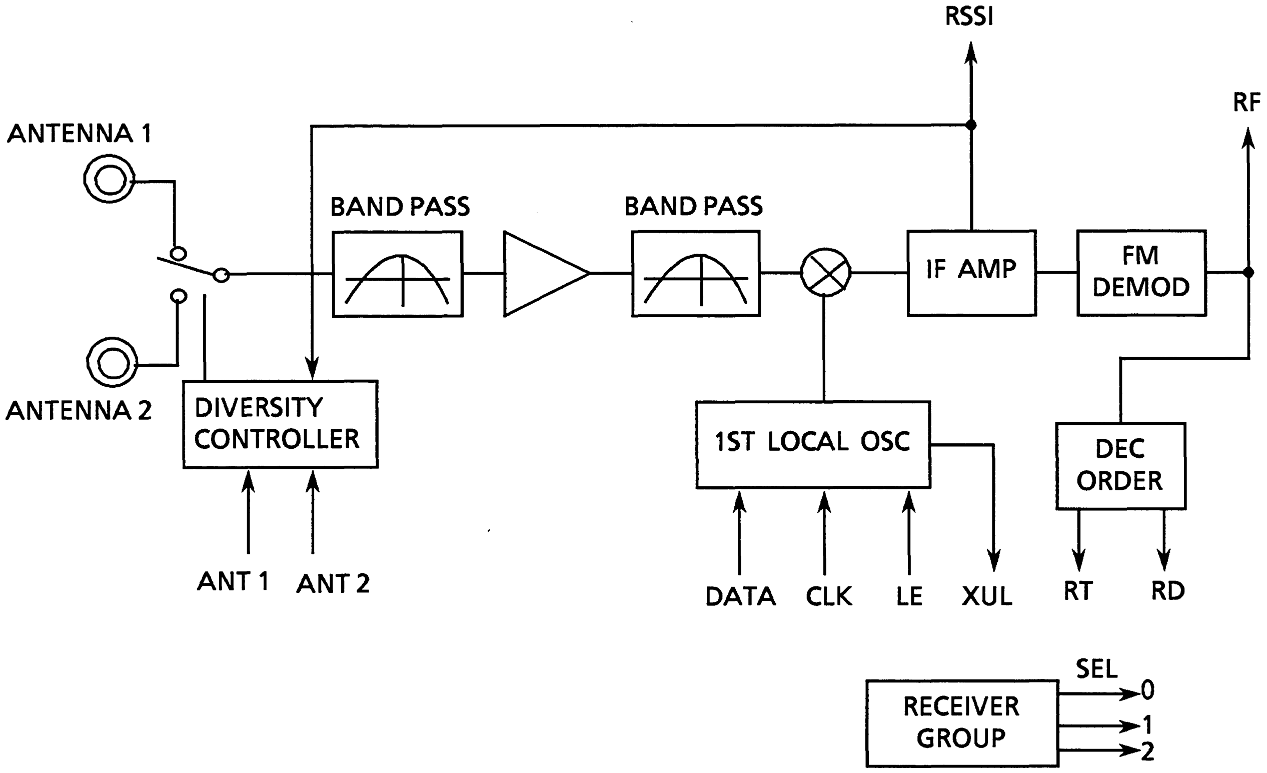

+ 5V
RL0-RL7
IC176
RL0-RL7
A0-A3
A0-A3
DATA BUS
D0-D7
B0-B3
B0-B3
CLK8M
CLK
SL0-SL3
SL0-SL3
A01
A0 IN
RESET
RST
IRQ
I79IRQ
XCS
XI79SL

The keyboard /display controller (IC176) 8279 controls I/O board's sound generation circuit.

The operation mode is controlled by software. In BSM-8800, the operation mode is fixed as Decode, Scan and Sensor Matrix mode. SL0 ~ 3 signals are branched to latch B0 ~ 3 on the UP-0797 board.

3-2-7 Receiver, ZR-800P

Block Diagram


RSSI
RF
ANTENNA 1
ANTENNA 2
BAND PASS
BAND PASS
IF AMP
FM
DEMOD
DIVERSITY
CONTROLLER
1ST LOCAL OSC
DEC
ORDER
ANT 1
ANT 2
DATA
CLK
LE
XUL
RT
RD
SEL
RECEIVER
GROUP
0
1
2

◆ Operation of Diversity Antenna

Two antennas (ANT1, ANT2) are provided.
Operation of diversity antenna is determined by 2 bit signals (ANT1, ANT2).
The relation between signal condition and operating status for ANT1/ANT2 are shown in below;

ANT1	ANT2	Operating status
L	L	Diversity
L	H	ANT2 only
H	L	ANT1 only
H	H	Unfixed

L: Poor (low) signal condition
H: Good (high) signal condition

◆ Output of SEL

The output of SEL is 3 bit output same as receiving group of transmitters.
Type of output is open collector type.

Group	Channel	SEL		
		0	1	2
1	7001 – 7201	H	L	L
2	7202 – 7387	L	H	L
3	7388 – 7574	H	H	L
4	7575 – 7785	L	L	H
5	7786 – 7997	H	L	H

◆ Setting of Receiving Channel

3 input lines (DATA, CLK, LE) are used for receiving channel setting.
Timing chart for DATA, CLK. LE are shown in next page.
The chart contains following two information.

(1) Reference clock setting information
The upper part of DATA,CLKA,LE is for setting reference clock of receiver's synthesizer to 12.5 kHz.
This information is always written for any channel.

(2) Receiving frequency setting information
The lower part of DATA,CLKA,LE is for receiving channel setting.
D15~D0 shown in the chart is 16 bit data (= 65536 data) for determining receiving channel (I.E., receiving frequency).

Assuming that "f (MHz)" is a desired receiving frequency and "n" is a data for 16bit of D15~D0, following equation can be presented;

$$(f-45) \times \frac{1000}{12.5} = n$$

Example; When "f" = 457.5125 MHz, "n" is calculated as 33001.
33001 is converted to hexia code and expressed in 16bit data by D15~D0.

According to the above equation, rather wide range frequency can be set. However, only the channels on the table of above section 3.11.3 can be set actually for guaranteeing firm receiving condition.
When setting of receiving channel is not possible due to malfunction, "L0" is output on XUL.

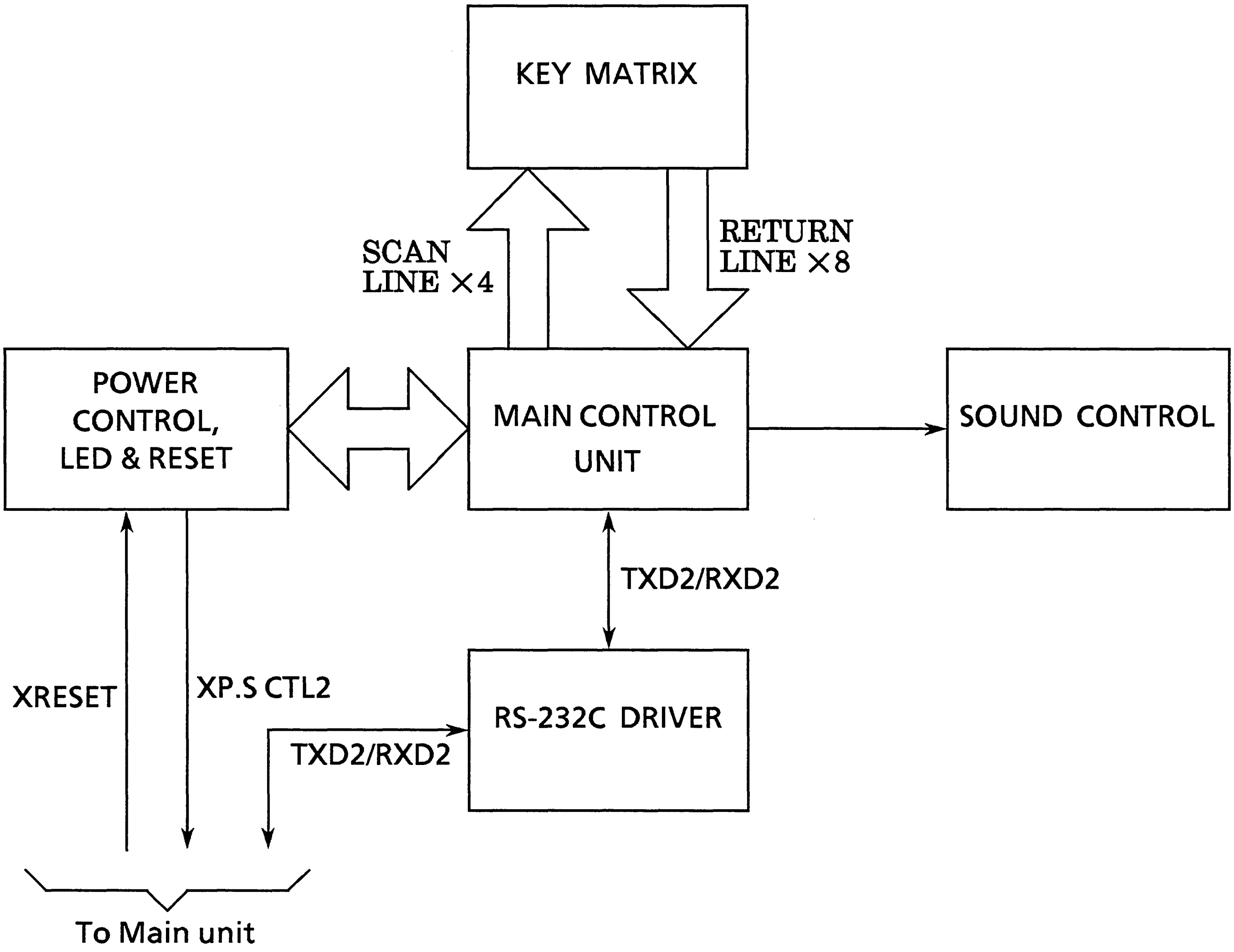
3-2-8 Transmitter

Internal operation of transmitter is not explained because specifications of transmitter can not be guaranteed if the repair is done locally.
Please see Section 6-6 for details.

3-3 Keypad, RY-881PA

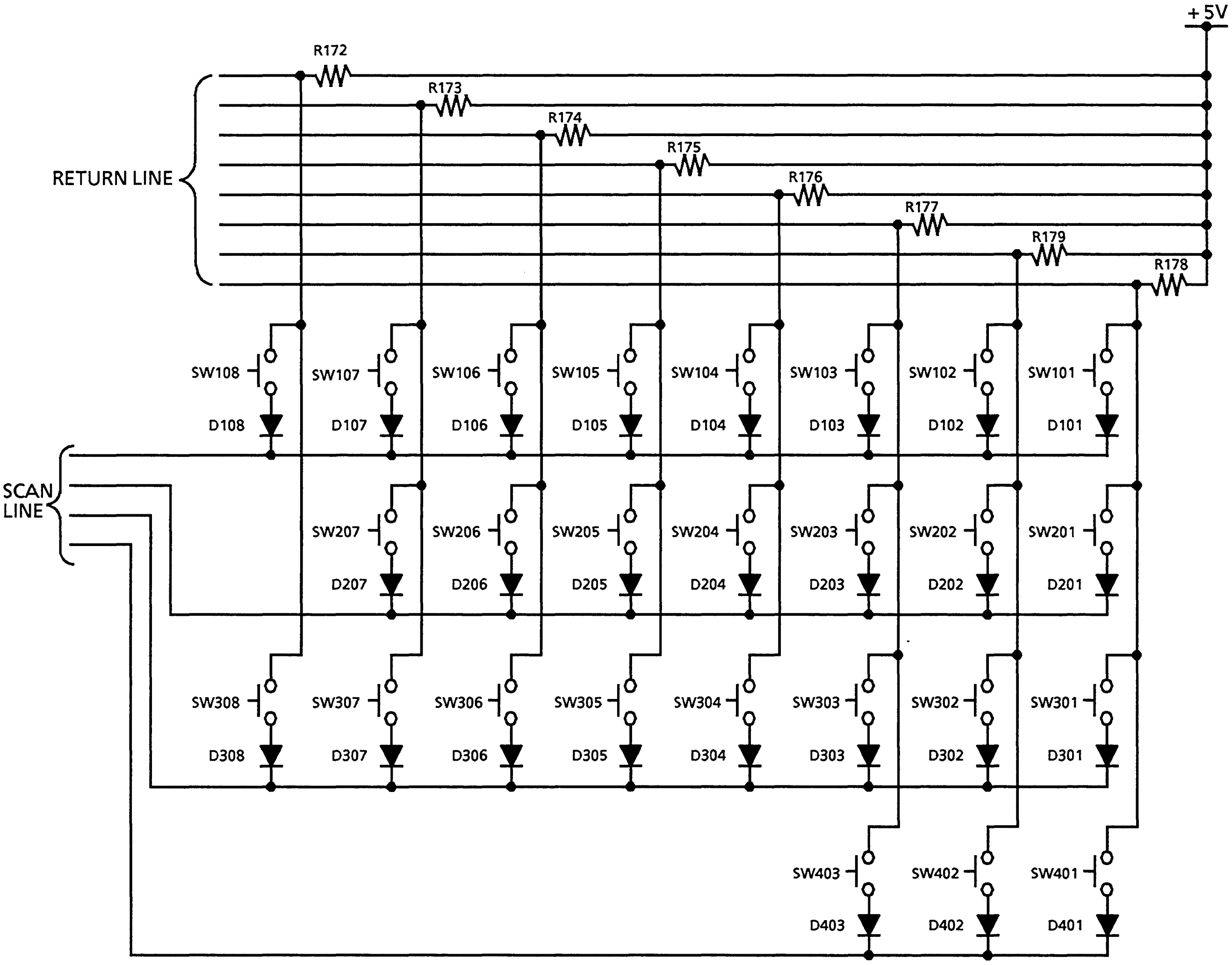
3-3-1 OPERATION RY Board, UR-3025

◆ **Keypad Operation Block Diagram**


KEY MATRIX
SCAN LINE ×4
RETURN LINE ×8
POWER CONTROL, LED & RESET
MAIN CONTROL UNIT
SOUND CONTROL
TXD2/RXD2
XRESET
XP.S CTL2
TXD2/RXD2
RS-232C DRIVER
To Main unit

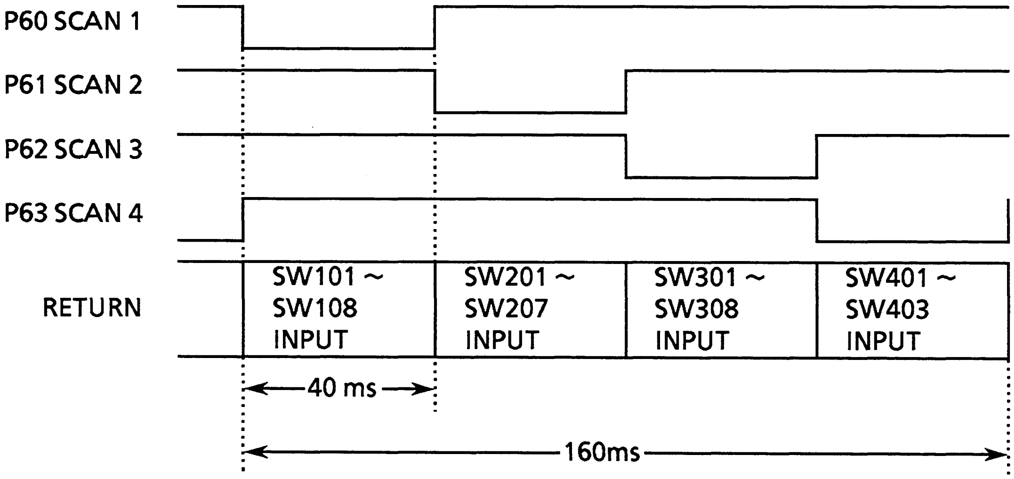
◆ Hardware Composition

The 26 keys on the keypad are arranged in matrix formation. The statuses of these keys are read by 8 return lines.


+5V
RETURN LINE
R172
R173
R174
R175
R176
R177
R179
R178
SCAN LINE
SW108
SW107
SW106
SW105
SW104
SW103
SW102
SW101
D108
D107
D106
D105
D104
D103
D102
D101
SW207
SW206
SW205
SW204
SW203
SW202
SW201
D207
D206
D205
D204
D203
D202
D201
SW308
SW307
SW306
SW305
SW304
SW303
SW302
SW301
D308
D307
D306
D305
D304
D303
D302
D301
SW403
SW402
SW401
D403
D402
D401

◆ Key Scanning Timing

The inputs of all the keys on the keypad are time-shared by the timings provided by SCAN1 - 4. These timings are shown below.



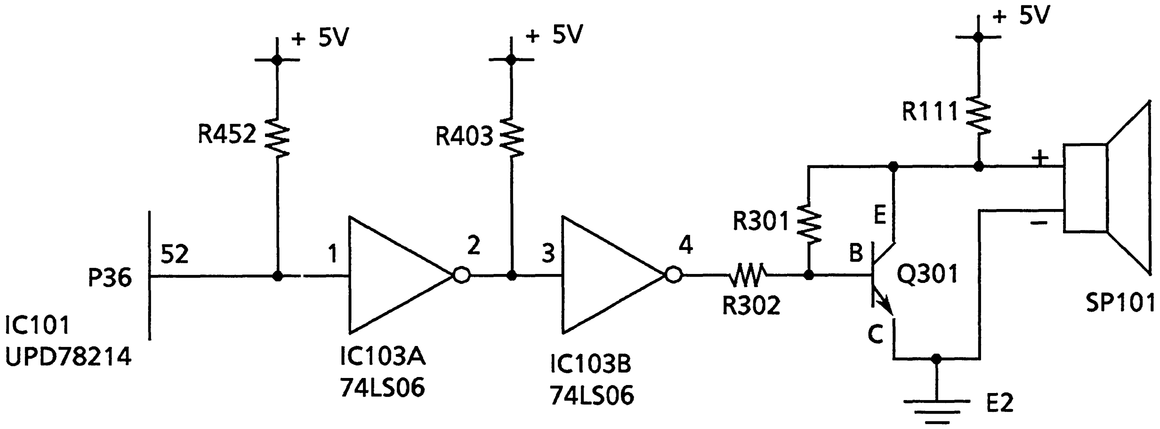
◆ Serial Communication

The serial communication with the bedside monitor main unit is controlled by the bus driver. The serial communication mainly consists of the key code data, and the control signals for the LED and key sound. The specification of this serial communication is :

*RS-232C Communication
* Baud Rate: 4800 or 9600 bps
* Character Length: 8 Bit
* Stop Bit Frequency: 1 Bit
* Operation Mode: ASYNCHRONOUS
* Parity: None

The baud rate depends on the setting of the dip switch SW501. The IC101 begins its transmission when the READY signal is asserted (HIGH).

◆ Sound Control



There are two types of key sound generated by the piezoelectric crystal speaker SP101. The type of key sound generated depends on the control data it received from the bedside monitor main unit via the IC102 and IC101. The frequency and the output time of the key sound type is shown in the table below.

Key sound type	Frequency	Output time
Key sound 1	3.0 kHz	50~60 msec
Key sound 2	2.0~1.4 kHz	3.0~3.6 msec

◆ Power Supply Control

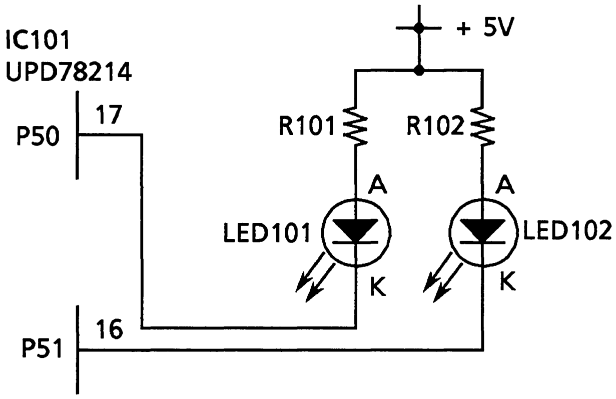
The IC101 outputs the power supply control signal pulse, P.S CTL2, via its port P43 when one of the following conditions is observed.

* When the SW101 key is pressed for more than 120 msec.

* When the status of the M/S SEL signal is LOW.

◆ LED Control

IC101 controls the LED101 and LED102 according to the instruction received from the bedside monitor main unit via IC102. The LED lights up when the connected port of IC101 is LOW and goes off when the port is HIGH.

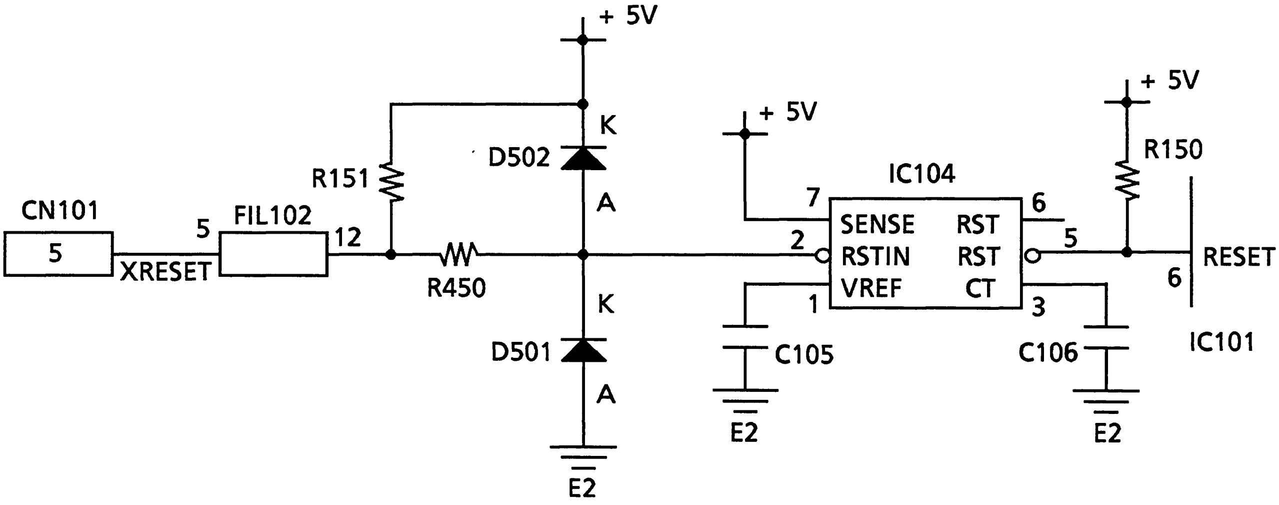

IC101
UPD78214
+ 5V
P50
17
R101
R102
A
A
LED101
LED102
K
K
16
P51

◆ RESET

IC101 is reset under one of the following conditions :

* When it received the reset signal from pin No.5 of connector CN101 via IC104.

* When the + 5 V voltage drops below 4.8 V.


+ 5V
+ 5V
+ 5V
K
D502
A
R151
R150
IC104
CN101
5
FIL102
12
5
XRESET
R450
K
D501
A
E2
7
SENSE
2
RSTIN
VREF
1
RST
RST
CT
6
5
3
C105
C106
E2
E2
RESET
6
IC101

3-4 Head Amplifiers

3-4-1 ECG Head Amp (AC-800P) Board, UP-0272

◆ General

The Hybrid IC (IC007) "ISOLATE" is mounted on not only this ECG head amplifier but also the others. In IC007, the F-CLK Generator supplies the power to the floating circuit, and the Switching Circuit SW1 demodulates the modulated signal from the floating circuit.

The Hybrid IC (IC009 ~ 012) "ECG BUF" buffers the ECG input signal and detects any electrode disconnection.

The Hybrid IC (IC008) "ECG SEL" selects an ECG lead. In IC008, the Switching Circuit SW3 modulates the selected ECG signal.

The S-P Converter (IC005) outputs the ECG lead selection signal to the Multiplexer (MPX1) in IC008 and the neutral electrode selection signal (for negative feed back) to the analog switch SW2(IC003B) or IC009 ~ 011.

The Counter (IC006) controls IC005 and the multiplexer (IC004) "MPX2" for time-sharing electrode disconnection signals.

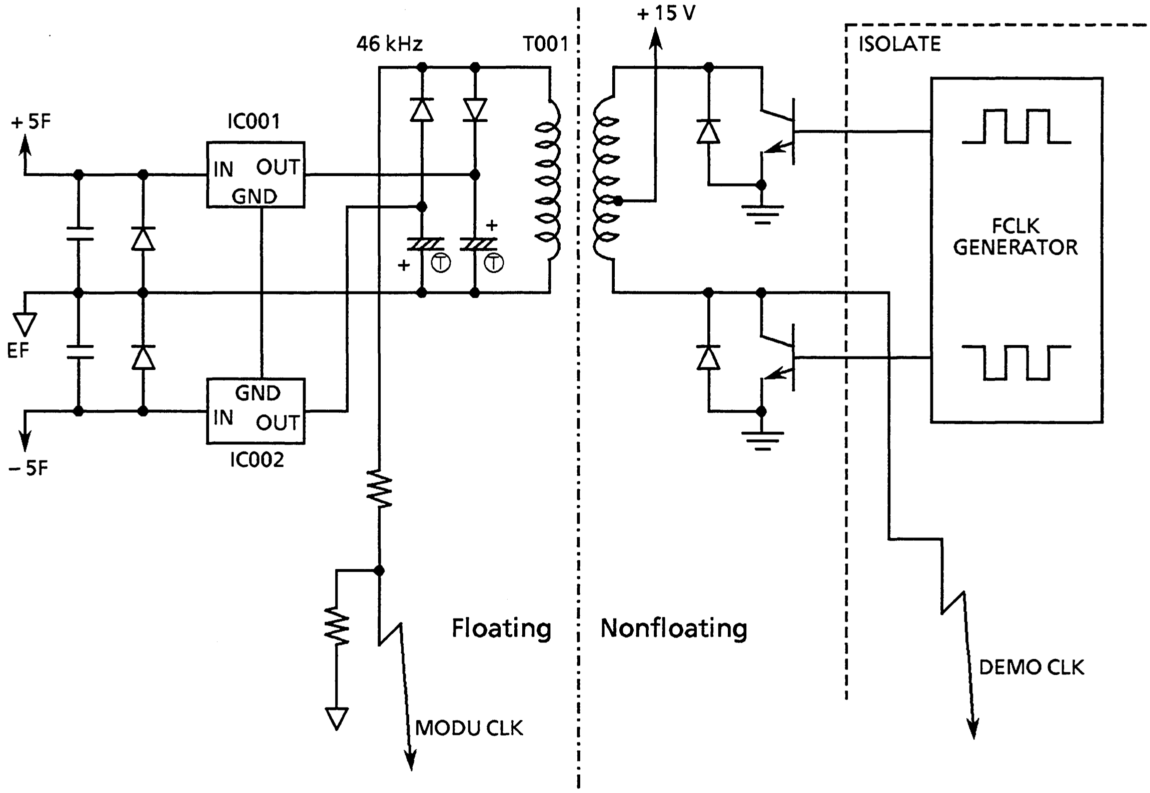
◆ Floating Power Circuit

On the following circuit, the DC-DC converter circuit supplies the power(+5F,EF, −5F) to the floating circuit.

The MODU CLK signal is a 64kHz chopping signal to modulate the time-shared signal so as to transfer the time-shared signal from the floating circuit to the nonfloating circuit.

The DEMO CLK signal is a 64kHz chopping signal to demodulate the chopped signal.

The MODU CLK and DEMO CLK are synchronized with opposite polarity.


+15 V
46 kHz
T001
ISOLATE
+5F
IC001
IN OUT
GND
FCLK GENERATOR
EF
GND
IN OUT
IC002
−5F
Floating
Nonfloating
DEMO CLK
MODU CLK

NOTE

The floating power circuit for the other Head Amp board is the same as the above circuit.

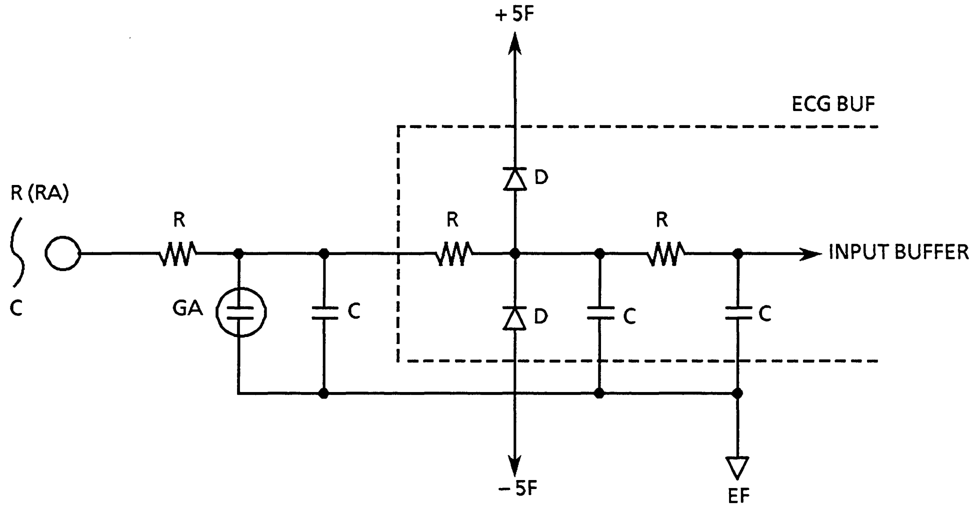
◆ Input Protection Circuit

• Electrosurgery Interference Elimination Filter

On the following circuit, the low-pass filter composed of the 3-stage R-C connection attenuates the high frequency component (100 dB down or more between 300kHz and 5MHz) of Electrosurgery Interference. The low-pass filter is intended to monitor ECG, to protect the input circuit and to reduce heat in case of simultaneous use of an electrosurgery unit.

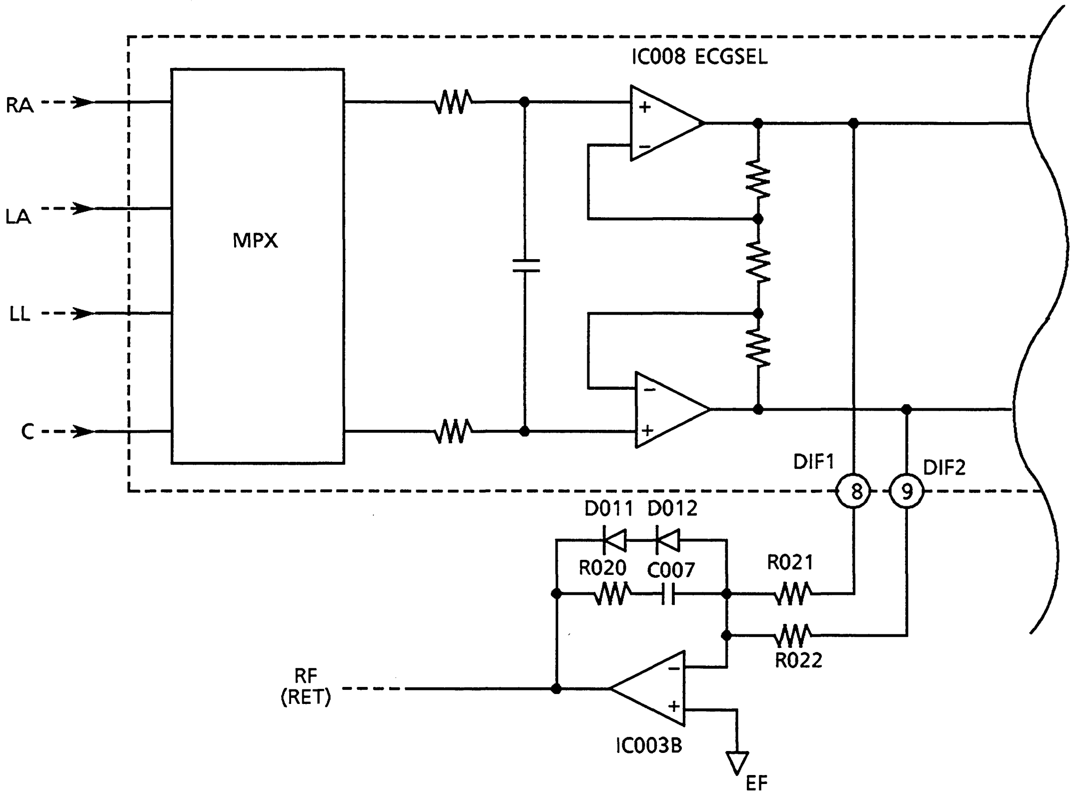
• Defibrillator Discharge Protector

On the following circuit, the series-connected resistors limit the discharge current to protect the input circuit against an excessive-voltage input signal, and the gas arrestor and diodes limit the discharge voltage when a discharge is started with a defibrillator.



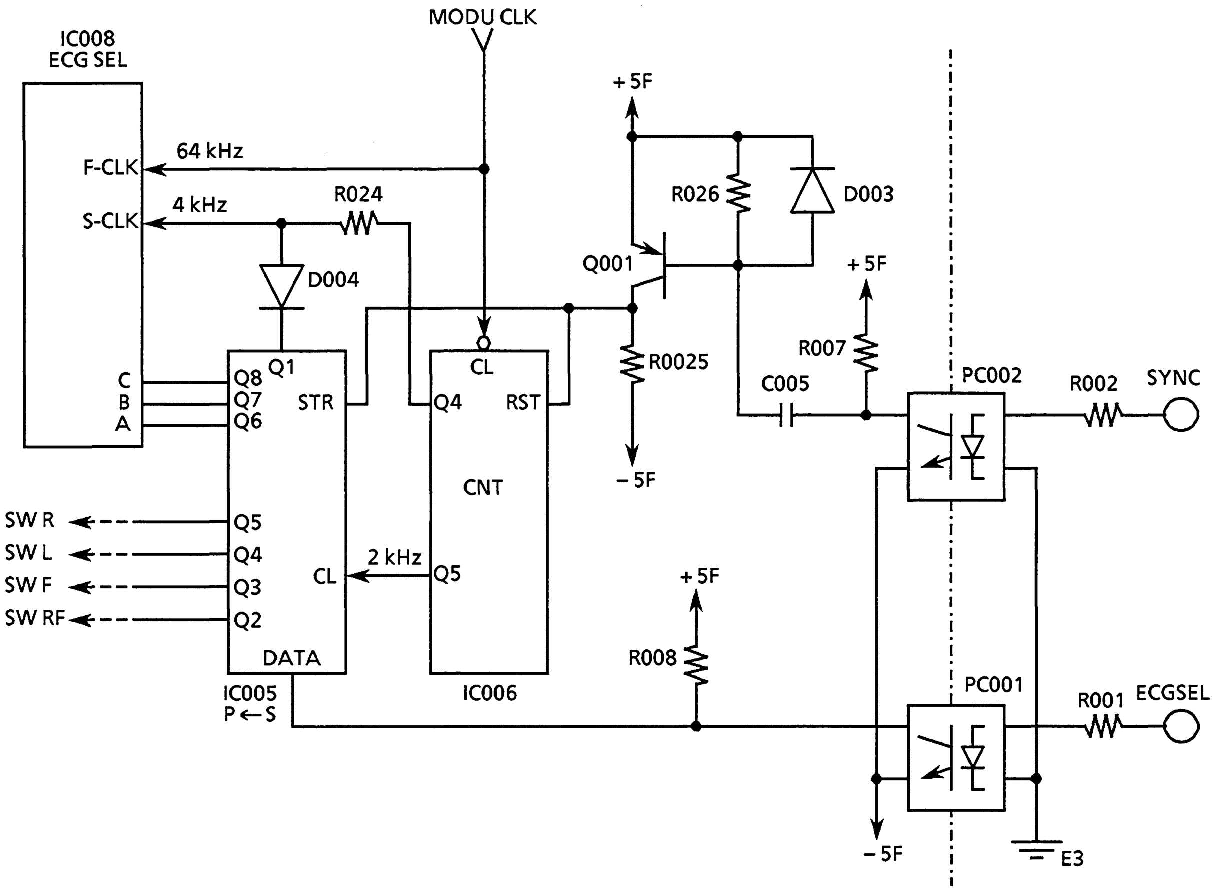
◆ Negative Feed-back Circuit

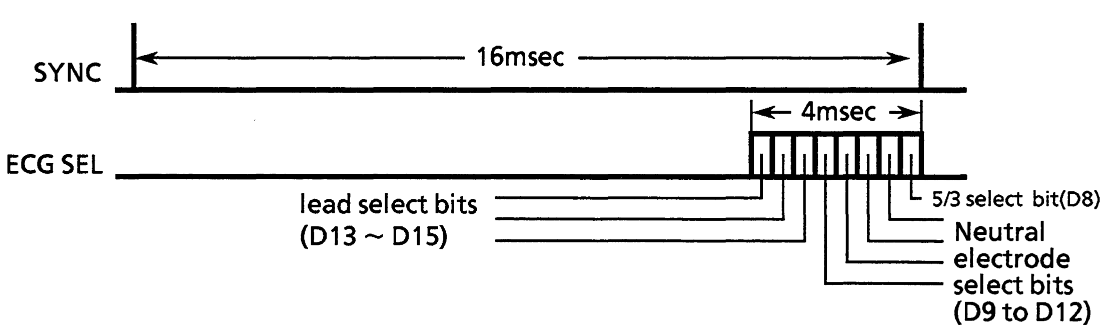
In theory, an in-phase artifact included in an ECG wave should not interfere with the ECG wave signal since the ECG signal is pre-amplified with the differential amplifier. However, in actuality, an ECG signal with an in-phase artifact appears between DIF1 and DIF2 since the in-phase signal changes to a signal with some phase difference due to the impedance unbalance between electrodes. To overcome this, the output signals from the differential amplifier are branched to the negative feed-back circuit for neutral electrode (DIF1 & DIF2). The negative feed-back circuit attenuates the in-phase component based on the Floating Ground (EF) and obtains a high Common Mode Rejection Ratio (CMRR).



◆ ECG Lead Selecting Circuit

The following ECG SEL signal through the photocoupler (PC001) selects an ECG lead and a neutral electrode line for negative feed-back from input signal lines. The ECG SEL signal is converted with the S-P converter (IC005) to parallel signals. SW R, SW L, SW F, or SW RF of the parallel signals controls each ECG BUF (IC009 ~ 012) to select a neutral electrode from the four electrodes.


IC008
ECG SEL
F-CLK
S-CLK
C
B
A
64 kHz
4 kHz
R024
D004
MODU CLK
+5F
R026
D003
Q001
+5F
R007
R0025
C005
-5F
PC002
R002
SYNC
Q8
Q7
Q6
Q1
STR
Q5
Q4
Q3
Q2
CL
DATA
IC005
P←S
CL
Q4
RST
CNT
Q5
2 kHz
IC006
SW R
SW L
SW F
SW RF
+5F
R008
PC001
R001
ECGSEL
-5F
E3


SYNC
16msec
4msec
ECG SEL
lead select bits
(D13 ~ D15)
5/3 select bit(D8)
Neutral
electrode
select bits
(D9 to D12)

Each bit combination of an ECG SEL signal and an ECG lead is related as follows:

[3 Electrode leads]

Lead	Electrodes				ECG SEL bits							
	ECG1			ECG2	D15	D14	D13	D12	D11	D10	D9	D8
	+	N	−	(= ECG1)								
I	L	F	R	(The same as the left)	1	1	1	1	1	0	1	1
II	F	L	R		1	1	0	1	0	1	1	1
III	F	R	L		1	0	1	0	1	1	1	1

[5 Electrode leads]

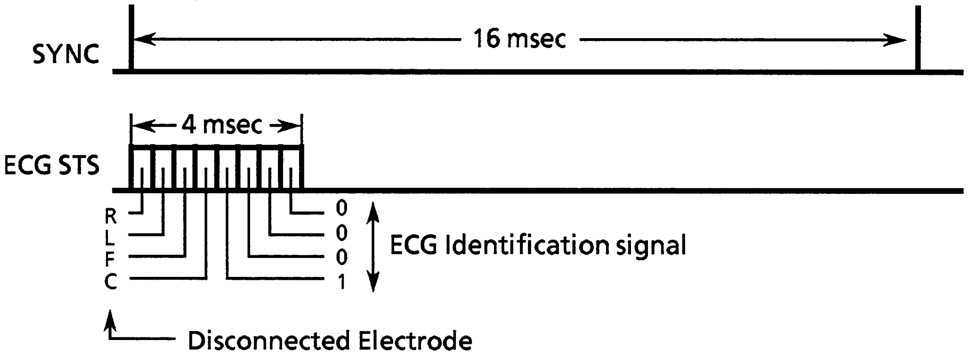
Lead	Electrodes						ECG SEL bits							
	ECG1			ECG2(Lead-II)			D15	D14	D13	D12	D11	D10	D9	D8
	+	N	−	+	N	−								
I	L	RF	R	F	RF	R	1	1	1	1	1	1	0	0
II	F		R				1	1	0	1	1	1	0	0
III	F		L				1	0	1	1	1	1	0	0
aVR	R		(L + F)/2				1	0	0	1	1	1	0	0
aVL	L		(R + F)/2				0	1	1	1	1	1	0	0
aVF	F		(R + L)/2				0	1	0	1	1	1	0	0
V	C		(R + L + F)/2				0	0	1	1	1	1	0	0
MCL	C	↓	L	↓	↓	↓	0	0	0	1	1	1	0	0

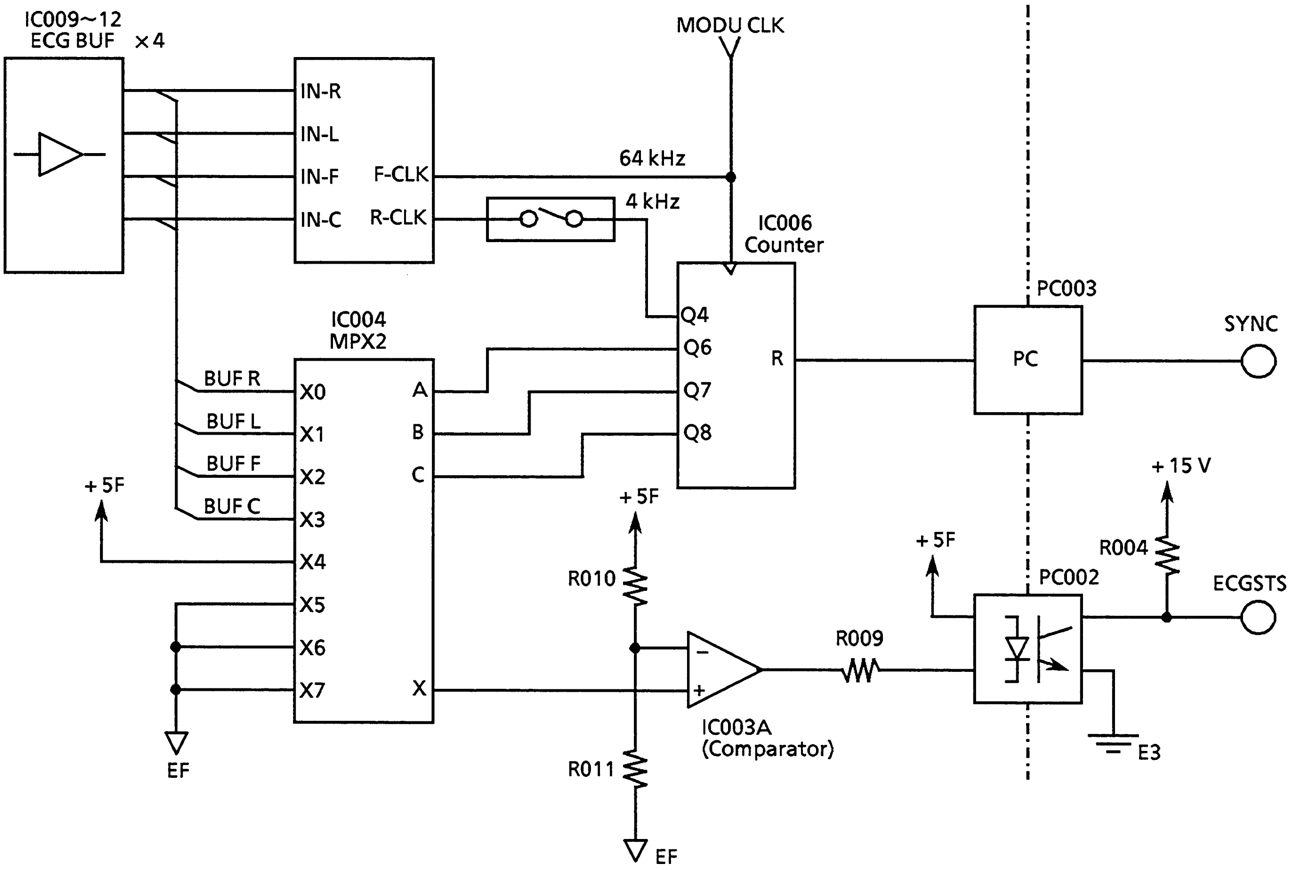
◆ Electrode Disconnection Detecting Circuit

The loop circuit between a patient and the input circuit is closed through a negative feed-back circuit when the electrode leads are connected to the patient. However, the loop circuit is opened and the related ECG BUF output (BUF R, BUF L, BUF F or BUF C) is drawn to the floating power voltage when an electrode or a lead wire is disconnected.

The Multiplexer (IC004) ”MPX2” time-shares the BUF R, L, F or C signal to be a serial format signal (ECG STS signal).

The comparator (IC003A) compares the time-shared signal with the reference voltage and outputs an ECG STS signal to the nonfloating circuit.


SYNC
16 msec
4 msec
ECG STS
R
L
F
C
0
0
0
1
ECG Identification signal
Disconnected Electrode


IC009~12
ECG BUF ×4
IN-R
IN-L
IN-F
IN-C
F-CLK
R-CLK
MODU CLK
64 kHz
4 kHz
IC006
Counter
Q4
Q6
Q7
Q8
R
IC004
MPX2
BUF R
BUF L
BUF F
BUF C
X0
X1
X2
X3
X4
X5
X6
X7
A
B
C
X
+5F
EF
R010
R011
IC003A
(Comparator)
R009
PC003
PC
SYNC
+15 V
R004
PC002
ECGSTS
E3

A disconnected electrode and the bits combination of the ECG STS signal are related as follows:

[3 Electrode leads]

Lead	Neutral Electrode	Electrode Condition	ECG STS bits			
			D7	D6	D5	D4
			R	L	F	C
I	F	Normal	0	0	0	1
		R: disconnect	1	0	0	1
		L: disconnect	0	1	0	1
		F: disconnect	1	1	0	1
		Open	1	1	0	1
II	L	Normal	0	0	0	1
		R: disconnect	1	0	0	1
		L: disconnect	1	0	1	1
		F: disconnect	0	0	1	1
		Open	1	0	1	1
III	R	Normal	0	0	0	1
		R: disconnect	0	1	1	1
		L: disconnect	0	1	0	1
		F: disconnect	0	0	1	1
		Open	0	1	1	1

[5 Electrode leads]

Lead	Neutral Electrode	Electrode Condition	ECG STS bits			
			D7	D6	D5	D4
			R	L	F	C
All	RF	Normal	0	0	0	0
		R: disconnect	1	0	0	0
		L: disconnect	0	1	0	0
		F: disconnect	0	0	1	0
		C: disconnect	0	0	0	1
		RF:disconnect	1	1	1	1
		Open	1	1	1	1

◆ ECG signal Modulation/Demodulation Circuit

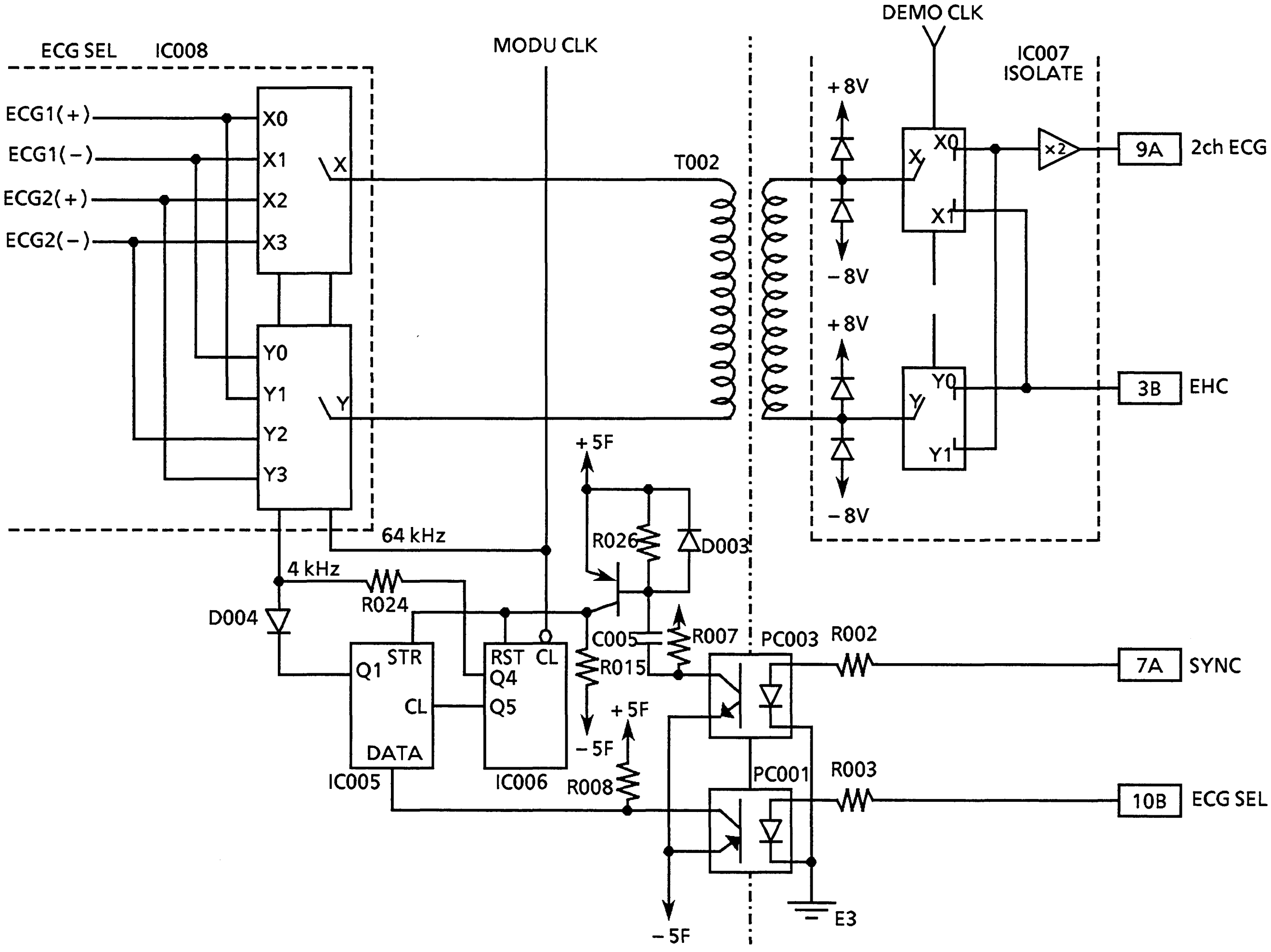
When the 3-electrode lead mode is selected in the main unit, only ECG1 is modulated with the MODU CLK signal on the floating circuit and demodulated with the DEMO CLK signal on the nonfloating circuit since IC005-Q1 is set to low level.

When the 5-electrode lead mode is selected in the main unit, ECG1 and ECG2 are alternately time-shared every 125μsec with the 4kHz clock from IC006-Q4 and modulated with MODU CLK since IC005-Q1 is set to high level.

The time-shared signal 2ch ECG is divided into two signals, ECG1 and ECG2 on UP-0270.

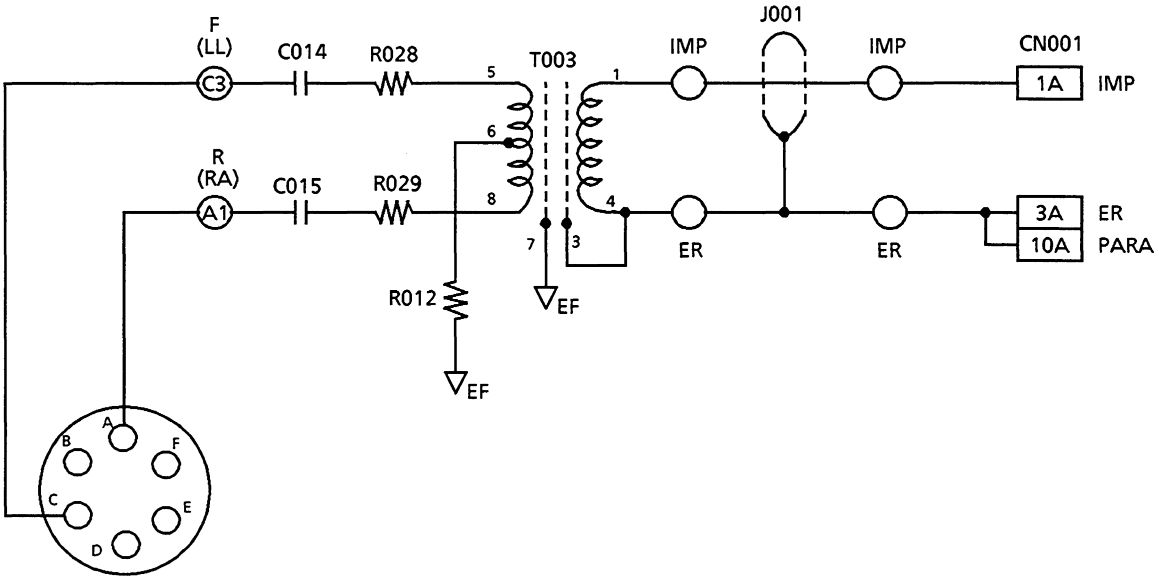
NOTE

Modulation with MODU CLK and Demodulation with the DEMO CLK circuit, which are provided on the other Head Amp board, are the same as the above circuit.


ECG SEL
IC008
ECG1(+)
ECG1(−)
ECG2(+)
ECG2(−)
X0
X1
X2
X3
X
Y0
Y1
Y2
Y3
Y
MODU CLK
T002
DEMO CLK
IC007
ISOLATE
+8V
−8V
X0
X1
Y0
Y1
x2
9A
2ch ECG
3B
EHC
64 kHz
4 kHz
R024
D004
Q1
STR
CL
DATA
IC005
RST
Q4
Q5
IC006
+5F
R026
D003
C005
R007
R015
−5F
R008
PC003
R002
PC001
R003
7A
SYNC
10B
ECG SEL
E3

◆ Respiration Signal Detecting Circuit

Respiration waveform is detected by means of the impedance method.
An impedance between two electrodes, R(RA) and F(LL), is excited with an 80kHz (respiration) carrier signal (10Vp-p) from UP-0271. The impedance is changed by respiration, inspiration and expiration.


F
(LL)
C3
C014
R028
5
T003
1
IMP
J001
IMP
CN001
1A
IMP
6
R
(RA)
C015
R029
8
A1
4
3A
ER
10A
PARA
7
3
ER
ER
R012
EF
EF
A
B
F
C
E
D

3-4-2 PRESS Head Amp (AP-800PA) Board, UP-0369

◆ General

The exciter (IC006) generates an excitation voltage to drive the Blood Pressure Transducer (BP1,BP2).

The blood pressure signals, P1 and P2, from the BP transducer are time-shared with the analog switch (IC003A) through a 200-times preamplifier (P1: IC007/008/011B, P2: IC009/010/012B) and 33Hz low-pass filter (P1: IC011A, P2: IC012A).

The analog switch (IC003A) is controlled with a 125Hz clock from the counter (IC004).

The comparator (IC013A/B) selects one of four states of the PARA signal according to the connection of BP1 or BP2.

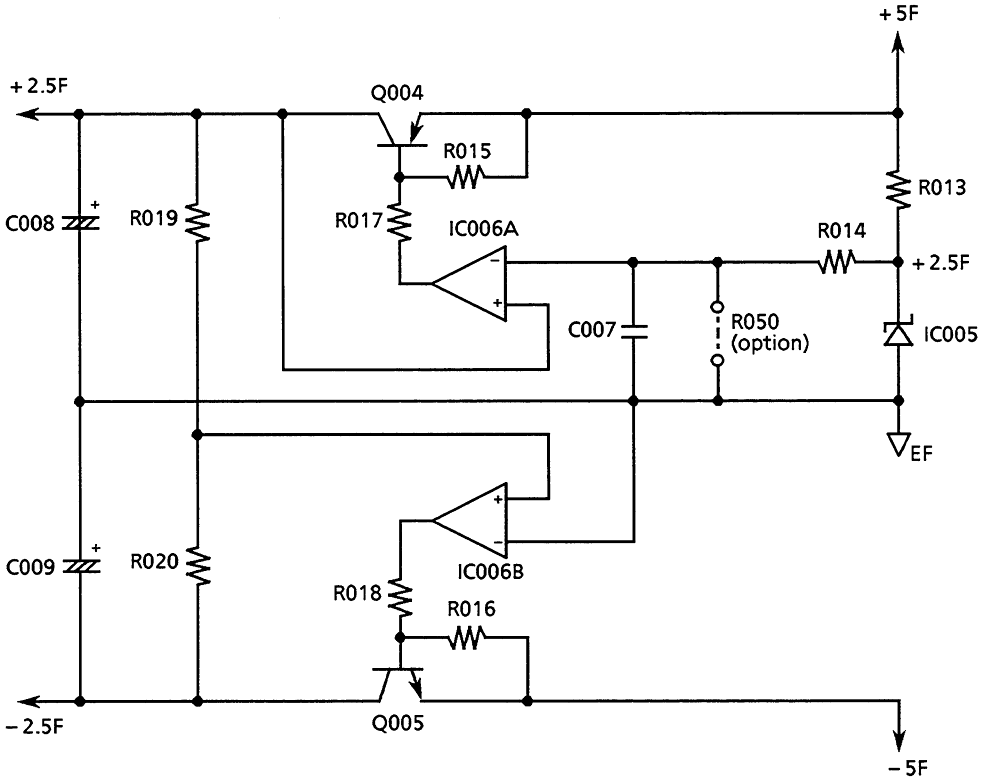
◆ Exciter Circuit

This circuit generates a ±2.5 V excitation voltage to excite the blood pressure transducers.

The ±2.5V excitation voltage is stabilized through the reference voltage generator (IC005).

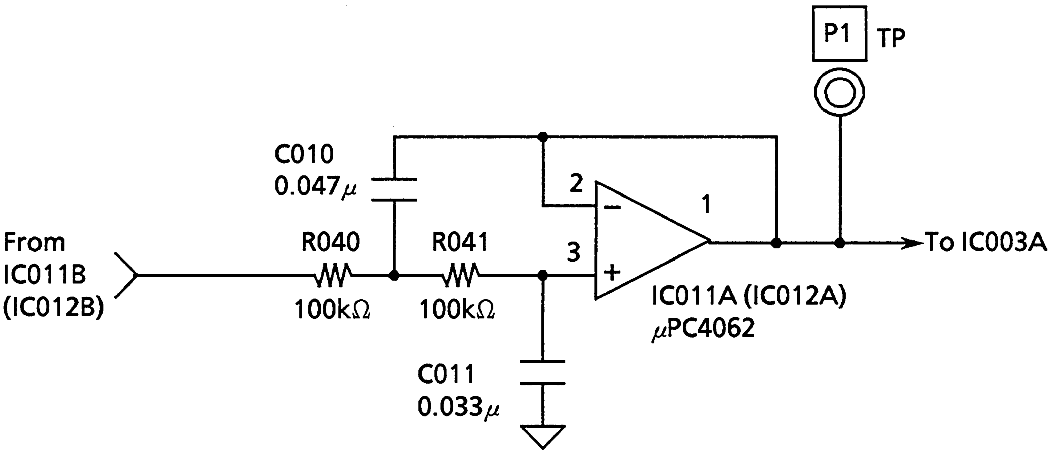
The excitation voltage can drive two transducers with an exciting load up to 200 Ω.

The excitation voltage can be attenuated by mounting a resistor on "R050" location and can be set to the proper voltage for a BP transducer by combining the resistor (R050) with 10 kΩ (R014).


+5F
+2.5F
Q004
R015
R013
C008
R019
R017
IC006A
R014
+2.5F
C007
R050
(option)
IC005
EF
C009
R020
IC006B
R018
R016
-2.5F
Q005
-5F

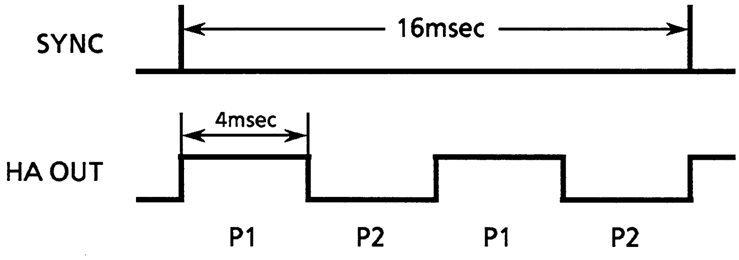
◆ 33Hz Low-pass Filter Circuit

The following 2-stage low-pass filter is provided through the preamplifier to pass the frequency component of the blood pressure waveform only.
In the following filter, the cut-off frequency is 33Hz. However, the total cut-off frequency is 20Hz or 10Hz (selectable on the System Setup display) by passing the software-filter in the Main unit.


P1
TP
C010
0.047μ
From
IC011B
(IC012B)
R040
100kΩ
R041
100kΩ
2
3
1
−
+
To IC003A
IC011A (IC012A)
μPC4062
C011
0.033μ

[Output timing]

The P1 and P2 signals are alternately outputted from HA OUT every 4msec synchronizing with the SYNC signal as follows:


SYNC
16msec
4msec
HA OUT
P1
P2
P1
P2

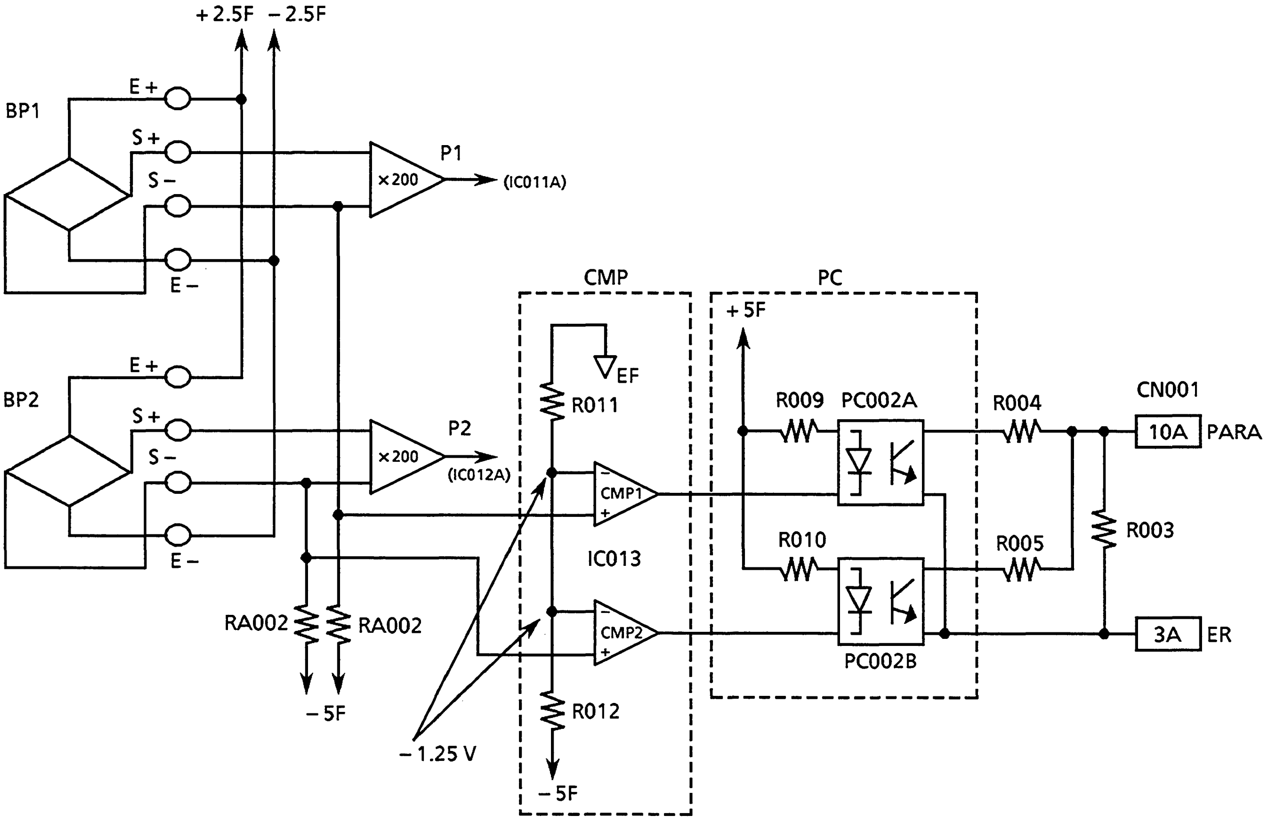
◆ PARA signal Generating Circuit

The following voltages for the PARA signal are generated according to the connection of Blood Pressure Transducers BP1 or BP2.

Connected BP Transducer	PARA Voltage
BP1 and BP2	1.5V ± 25mV
BP1	1.35V ± 25mV
BP2	1.2V ± 20mV
No connection	1.1V ± 20mV

When a transducer is not connected, the output from the comparator (IC013A/B) is low level since the positive terminal on IC013A/B is biased to 5V. The photocoupler (PC002A/B) is set to "ON". The generating voltage for the PARA signal is 1.1V since + 5V REF is divided between the pull-up resistor (10kΩ) for 5V REF and resistors (R003 ~ 005) in parallel.

When one or two transducers are connected, the output from IC013A/B is high level since the positive terminal on IC013A/B is approx. 0V. The PC002A/B is set to "OFF". The generating voltage for the PARA signal is different from 1.1V since resistors in parallel decrease according to the BP1 or BP2 connection.


+2.5F
-2.5F
BP1
E+
S+
S-
E-
×200
P1
(IC011A)
BP2
E+
S+
S-
E-
×200
P2
(IC012A)
RA002
RA002
-5F
-1.25 V
CMP
V_{EF}
R011
CMP1
IC013
CMP2
R012
-5F
PC
+5F
R009
PC002A
R010
PC002B
R004
R005
R003
CN001
10A
PARA
3A
ER

3-4-3 CO Head Amp (AH-800PA) Board, UP-0318

◆ General

The 16Hz Low-pass filter (R015&C009, R023&C011) eliminates only high frequency component, such as electrosurgery interference.

The Multiplexer (IC009) time-shares a Reference signal (REF), Injection fluid Temperature signal (Ti), Blood Temperature signal (Tb) and Blood Temperature variation signal (ΔTb).

The Auto-shift circuit (IC012) shifts the DC voltage of the baseline so as not to saturate the ΔTb signal due to 1000-times amplification.

The S-P converter (IC011) controls IC012.

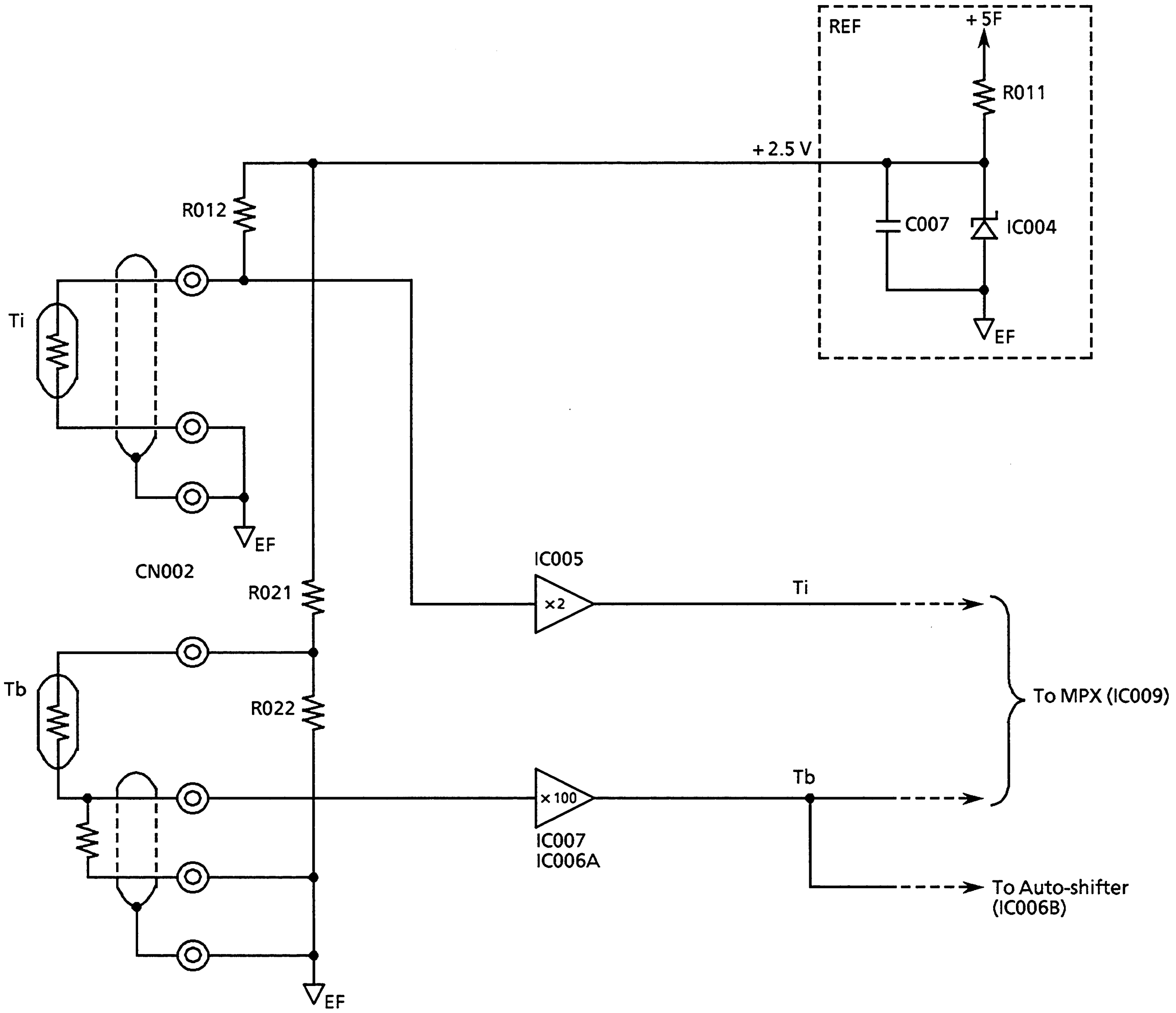
The Counter (IC010) generates a 250Hz clock for IC012 and control signals for IC009.

◆ **Resistance-Voltage (R-V) Converter Circuit**

The following IC004 generates a +2.5 V reference voltage.

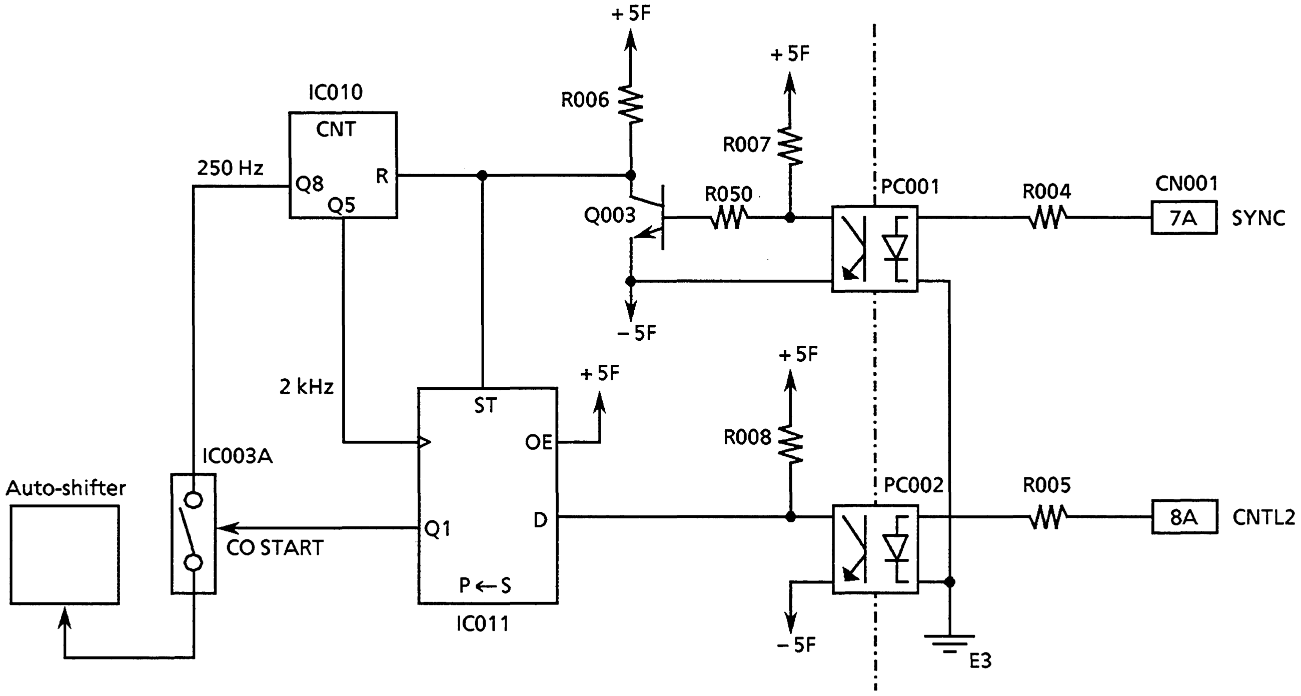
By dividing the reference voltage between R012 and Ti-thermistor resistance, the Ti-voltage is obtained according to the Ti-thermistor resistance variation caused by the injection fluid temperature.

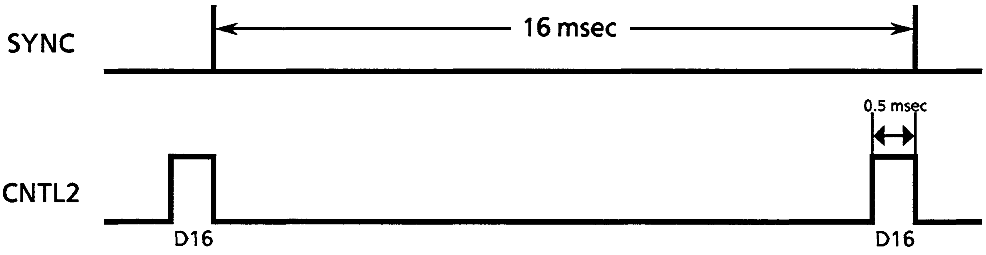
By dividing the reference voltage between R021 and R022 and shunting the Tb-catheter thermistor resistance to the R022, the Tb-voltage is obtained according to the Tb-resistance variation caused by the fluid injection.


REF
+5F
R011
+2.5 V
C007
IC004
EF
R012
Ti
EF
CN002
R021
IC005
×2
Ti
To MPX (IC009)
Tb
R022
Tb
×100
IC007
IC006A
To Auto-shifter
(IC006B)
EF

◆ **S-P Converter Circuit**

The "ST" terminal of the S-P converter (IC011) is set to High level when the SYNC signal varies from Low level to High level. Then analog switch (IC003A) is connected to 250 Hz clock to work the Auto-shifter (IC012) with Low signal from Q1 on IC011 after D16 on serial format signal CNTL2 is set to High level (CO Start signal) as follows:


+5F
+5F
IC010
CNT
R006
R007
250 Hz
Q8
R
Q5
R050
PC001
R004
CN001
Q003
7A
SYNC
-5F
+5F
+5F
2 kHz
ST
OE
R008
IC003A
Auto-shifter
PC002
R005
Q1
D
8A
CNTL2
CO START
P←S
IC011
-5F
E3


SYNC
16 msec
0.5 msec
CNTL2
D16
D16

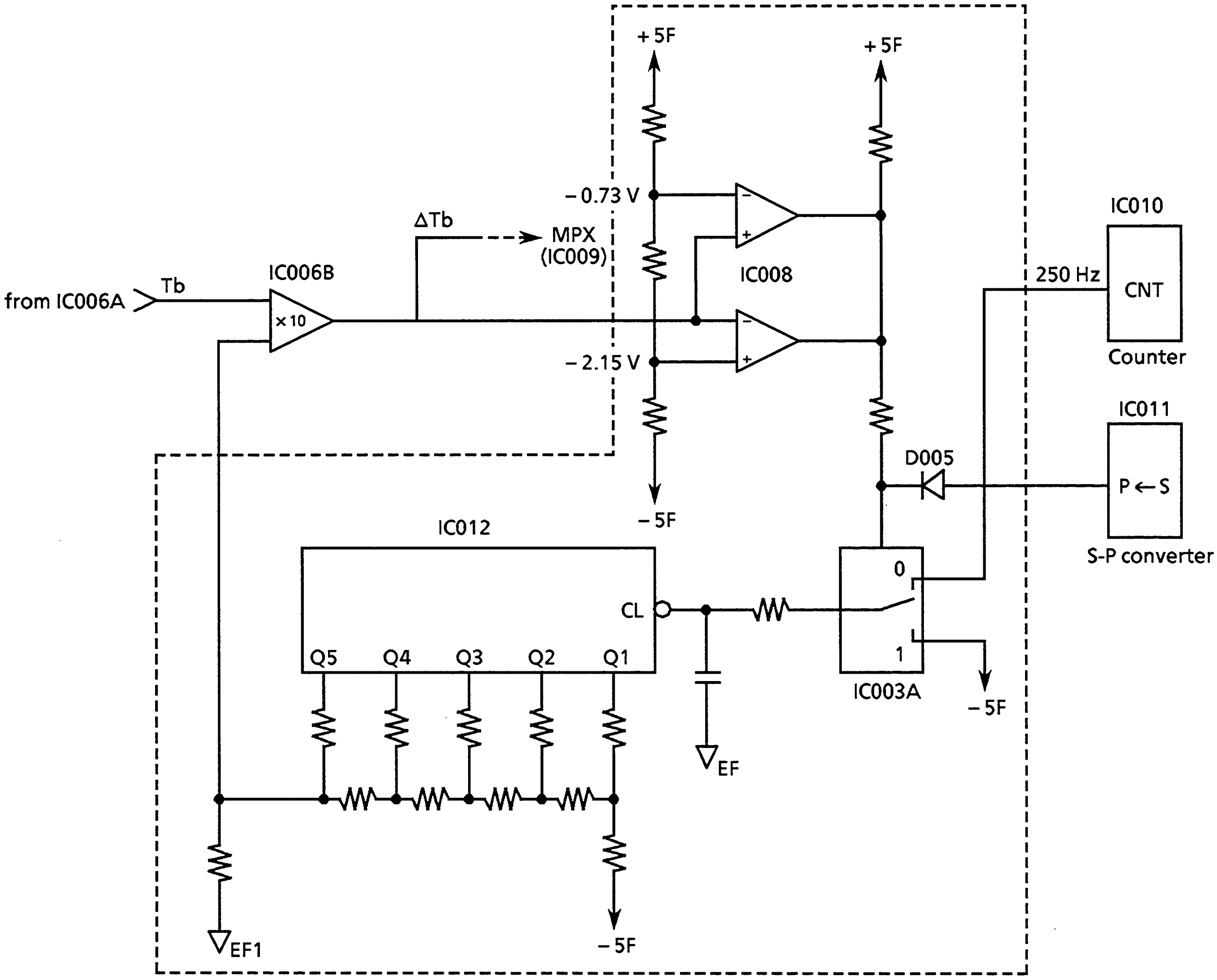
◆ Auto-shift Circuit

Blood Temperature Variation ΔTb needs more amplification than Ti or Tb since the ΔTb signal is a smaller signal variation than Ti or Tb.

The following auto-shift circuit shifts the ΔTb output voltage so as not to saturate the ΔTb output.

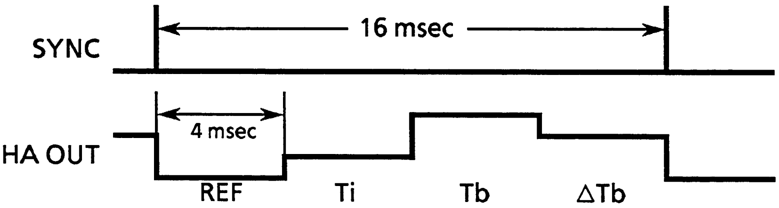
When the S-P converter (IC011) outputs a Low level signal to the analog switch (IC003A) after the CO start signal on serial format signal CNTL2 is inputted to IC011, IC003A connects the Counter (IC010) with the Auto-shifter Stair-type wave generator (IC012) to shift the ΔTb output voltage from the 10-times amplifier (IC006B).

When the output voltage falls within −2.15 V to −0.73 V, the comparator (IC008) outputs a High level signal to IC003A so as to complete the auto-shift function.


+5F
+5F
−0.73 V
ΔTb
MPX
(IC009)
IC008
IC010
CNT
Counter
250 Hz
from IC006A
Tb
IC006B
×10
−2.15 V
IC011
P←S
S-P converter
D005
IC012
−5F
CL
Q5
Q4
Q3
Q2
Q1
0
1
IC003A
−5F
EF
EF1
−5F

[Output timing]

REF, Ti, Tb and ΔTb are outputted from HA OUT every 4msec in the following order.


SYNC
16 msec
HA OUT
4 msec
REF
Ti
Tb
ΔTb

3-4-4 TEMP Head Amp (AW-800PA) Board, UP-0319

◆ General

The 160 Hz low-pass filter (R022&C007, R023&C008) eliminates any high frequency component, such as interference caused by an electrosurgery unit.

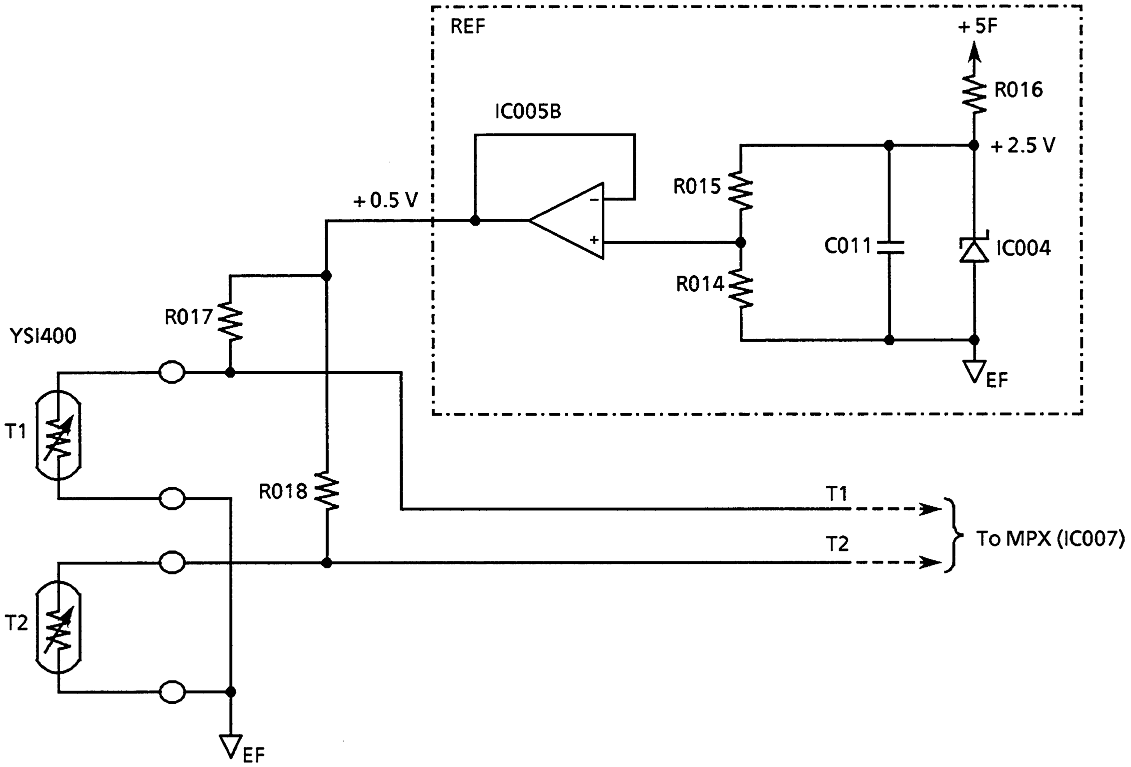
The multiplexer (IC007) time-shares the reference voltage for 27°C, REF0, calibration voltage for 37°C, CAL37 and body temperature T1 or T2.

The counter (IC008) generates control signals for IC007.

◆ **R-V Converter**

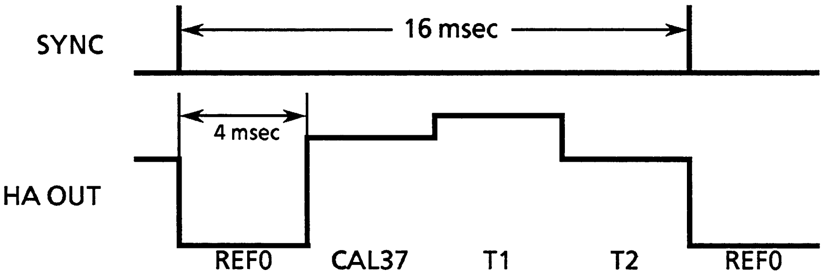
The following circuit composed of IC004/005B, R014 ~ 016 and C011 generates an + 0.5 V reference voltage.

T1 or T2 voltage is obtained according to temperature by dividing the 0.5 V reference voltage between R017 and T1-thermistor or R018 and T2-thermistor.


REF
+5F
R016
IC005B
+2.5 V
+0.5 V
R015
C011
IC004
R014
R017
YSI400
EF
T1
R018
T1
T2
To MPX (IC007)
T2
EF

[Output timing]

REF0, CAL37, T1 and T2 are outputted from HA OUT every 4msec in the following order.


SYNC
16 msec
4 msec
HA OUT
REF0
CAL37
T1
T2
REF0

3-4-5 Respiration Head Amp (AR-800PA) Board, UP0548

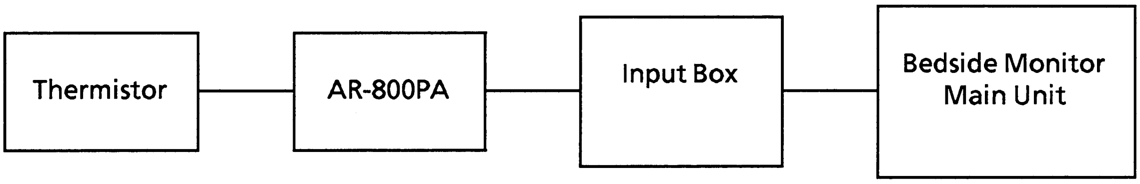
◆ Specifications

● General

AR-800PA is one of the head amplifiers for the BSM-8000 series bedside monitor to measure respiration with a thermistor pickup.

● System connection

Respiration head amplifier is inserted into the input box of the bedside monitor and a thermistor is connected to the head amplifier.



◆ General Description

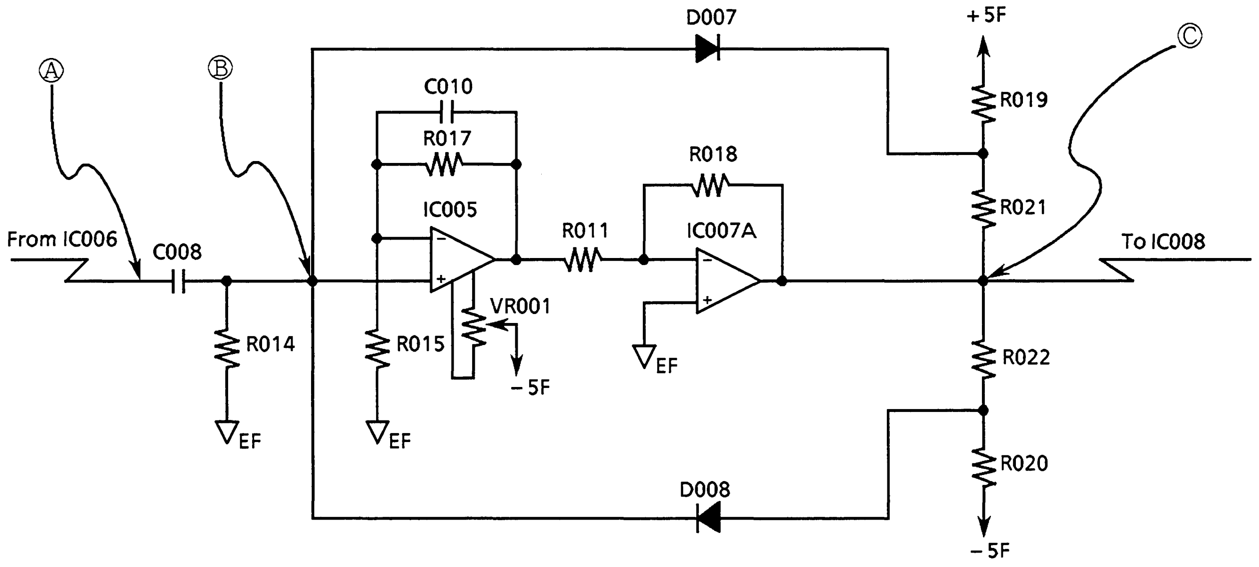
The AR-800PA consists of UP-0548 respiration board mounting floating power supply, respiration pickup exciter voltage (EXC) generator, input high-cut filter (3Hz), amplifier, auto inst (instantaneous baseline recovery) circuit, etc.

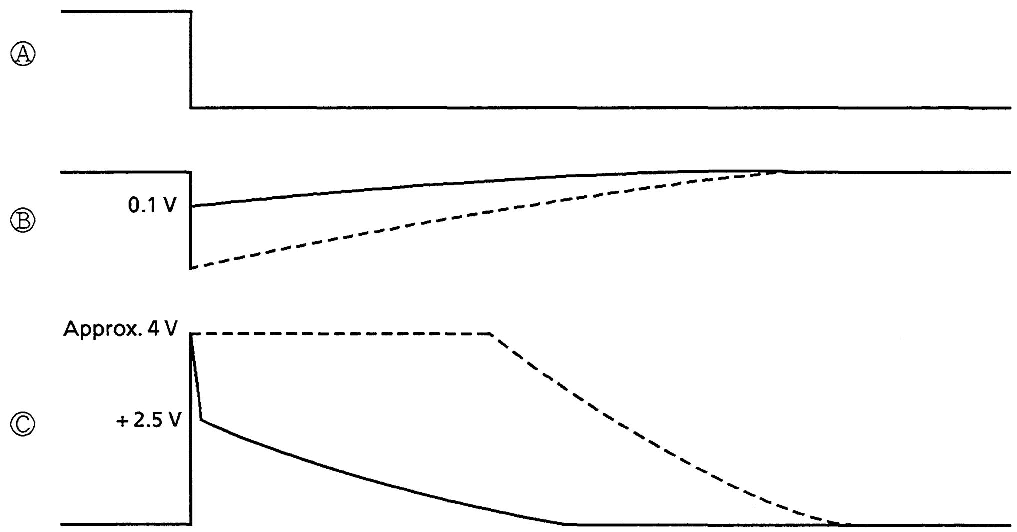
◆ Output

Analog signal is outputted without being time shared which is different from other head amplifiers.

◆ Auto Inst (Instantaneous Baseline Recovery) Circuit

Auto Inst function works when respiration waveform signal saturates in the circuit just after the pickup is connected to the amplifier or due to over-input.


Ⓐ
Ⓑ
Ⓒ
From IC006
C008
R014
EF
R015
EF
C010
R017
IC005
VR001
-5F
R011
R018
IC007A
EF
D007
D008
+5F
R019
R021
R022
R020
-5F
To IC008

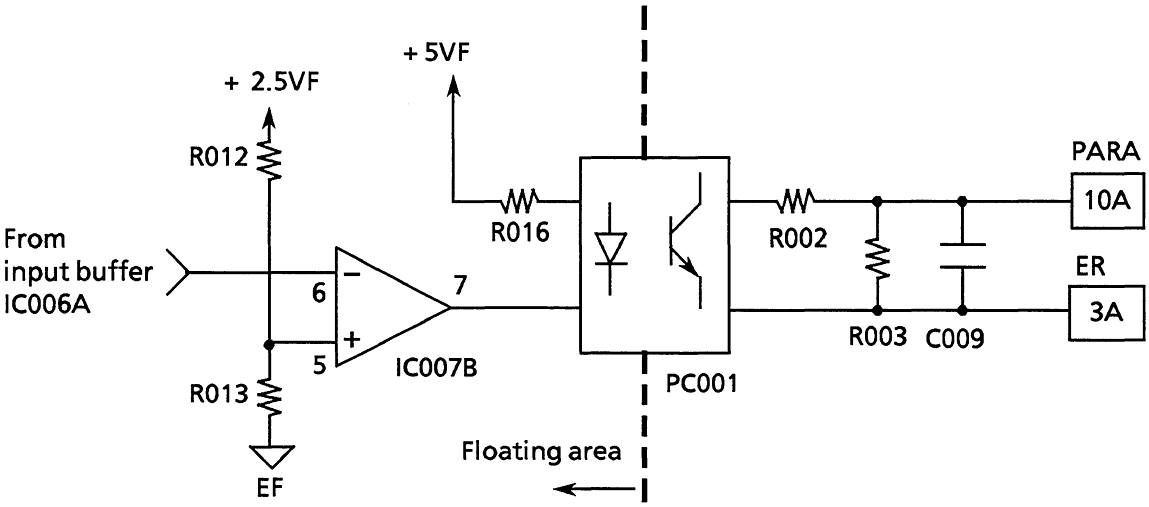


Straight lines indicate the voltages with the auto inst function and dotted lines indicate the voltages without diodes D007 and D008.

◆ PARA Signal Generating Circuit

Connection and disconnection of the respiration pickup change the PARA voltage as below:

+0.58V ±20mV .... no connection
+0.65V ±20mV .... connection


+ 2.5VF
+ 5VF
R012
R016
R002
PARA
10A
ER
3A
From
input buffer
IC006A
6
7
5
IC007B
R003
C009
R013
PC001
EF
Floating area

When the thermistor respiration pickup is not connected, comparator input pin-6 of the IC007B is approximately +2.5V and the comparator outputs level L. At this condition, PC001 photocoupler is conductive and +0.58V PARA output voltage is obtained. This voltage indicates no respiration measuring condition with the thermistor pickup.

When the pickup is connected, comparator pin-6 input is approximately +1V and the PC001 photocoupler becomes off, and +0.65V PARA voltage is obtained. This voltage indicates respiration measuring condition with the thermistor pickup.

3-4-6 SpO_2 Head Amp (AL-800PA) Boards, UP-0551 & 0552

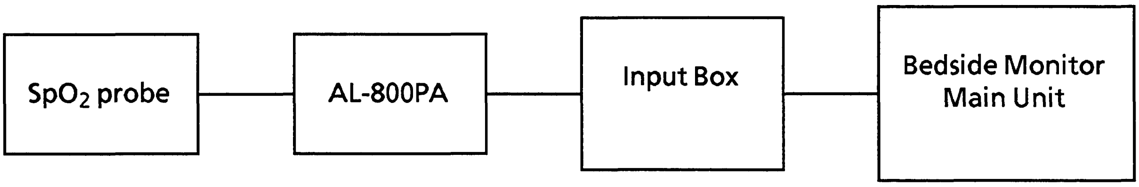
◆ Specifications

• General

AL-800PA is one of the head amplifiers for the BSM-8000 series bedside monitor to measure SpO_2 oxygen saturation.

• System connection

SpO_2 head amplifier is inserted into the input box of the bedside monitor and a SpO_2 probe is connected to the head amplifier.



◆ General Description

This unit has a function to detect the following four signals for calculation of % SpO_2 (oxygen saturation).

R	Transmitted red light intensity
ΔR	Transmitted red light intensity variation ($\Delta R1 = \Delta R2 \times 8$)
IR	Transmitted InfraRed light intensity
ΔIR	Transmitted InfraRed light intensity variation ($\Delta IR1 = \Delta IR2 \times 8$)

The SpO_2 head amplifier composes of UP-0551 Main board and UP-0552 Sub board. Block diagram on page 11.17 shows the major functions of each board.

• UP-0551 Main board

Red light and infrared light are emitted from the two LED lamps alternatively at 1kHz interval which is controlled by LED control circuit. Transmitted light through the subject are detected and converted into voltages by a photo detector and an amplifier, amplified to a specified level of signal by an auto gain controller, and then transferred to the Sub board.

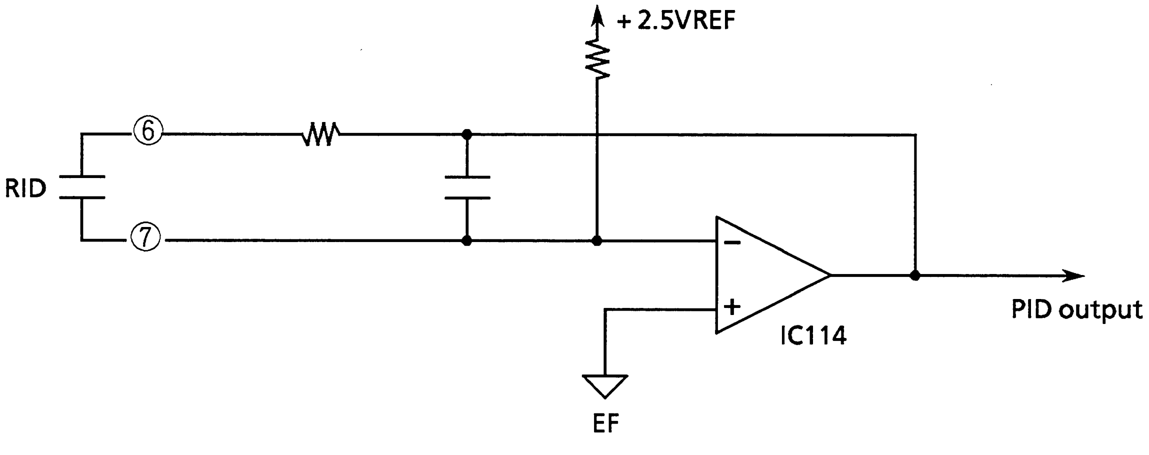
● UP-0552 Sub board

Noise in the transmitted light signal from the Main board is reduced by a time sharing filter. Base hold circuit holds the signal level while there is no light emission to the – 2.5V reference voltage (REF). R (Red light intensity signal) and IR (InfraRed light signal) are separately demodulated by two sample hold circuits and △R2 and △IR2 are outputted by AC amplifiers with auto inst (instantaneous baseline recovery) function. At the same time, △R1 and △IR1 are outputted by 8 time gain amplifiers. Finally these signals are converted into a time-shared signal by a multiplexer and then outputted through the UP-0551 Main board.

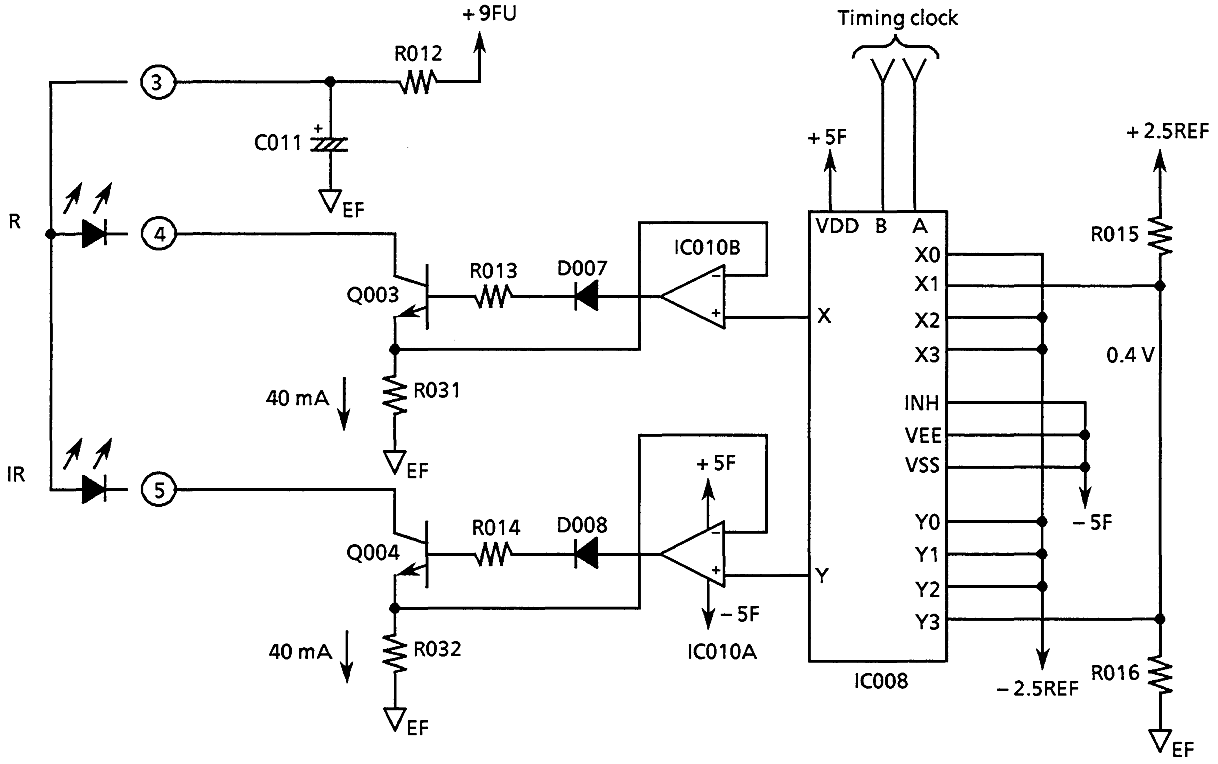
◆ Probe ID Amplifier

The probe ID amplifier compensates the variations of wavelength of light emitted from the LED lamps and also detects probe connection to the SpO_2 head amplifier.

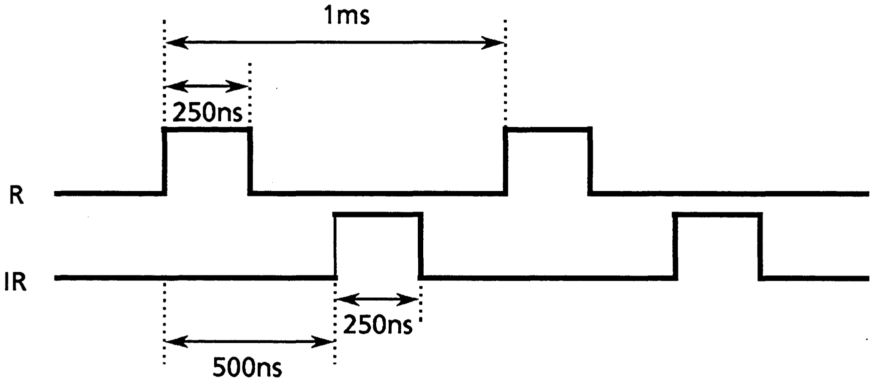
Each SpO_2 probe has its own ID (determined by the RID) which is converted into voltage signal (PID: Probe ID).



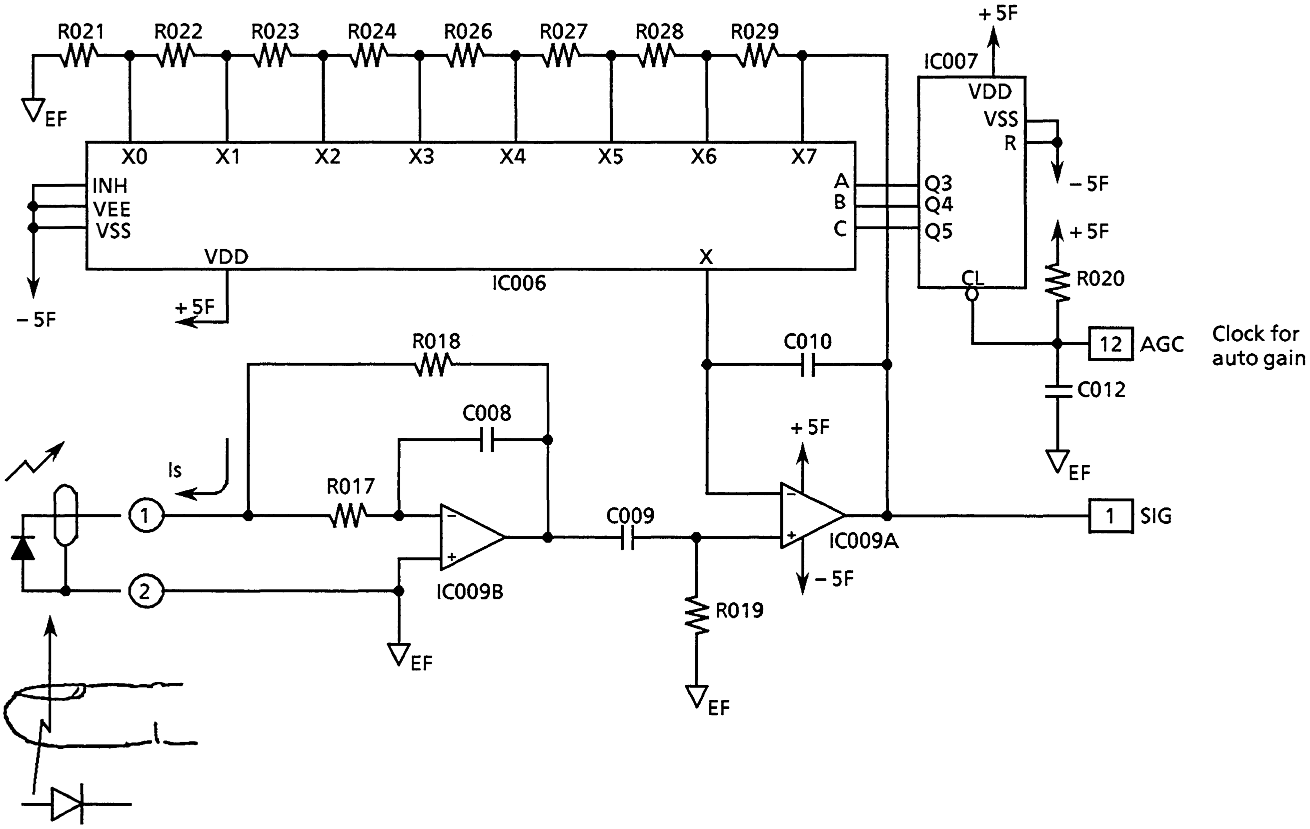
◆ LED Control Circuit


+9FU
R012
③
C011
EF
R
④
IR
⑤
Q003
R013
D007
IC010B
40 mA
R031
Q004
R014
D008
+5F
-5F
IC010A
R032
Timing clock
VDD B A
X0
X1
X2
X3
INH
VEE
VSS
Y0
Y1
Y2
Y3
X
Y
IC008
+5F
+2.5REF
R015
0.4 V
-5F
-2.5REF
R016
EF

Red light and infrared light are emitted from the two LED lamps alternatively at 1kHz interval controlled by above LED control circuit. Peak current flow of each LED is 40mA.


1ms
250ns
R
IR
250ns
500ns

◆ Input Amplifier and Auto Gain Control Circuit


R021
R022
R023
R024
R026
R027
R028
R029
EF
X0
X1
X2
X3
X4
X5
X6
X7
INH
VEE
VSS
VDD
X
A
B
C
IC006
-5F
+5F
+5F
IC007
VDD
VSS
R
Q3
Q4
Q5
CL
-5F
+5F
R020
12 AGC
Clock for auto gain
C012
EF
R018
C010
C008
+5F
Is
R017
1
2
C009
IC009B
IC009A
-5F
R019
EF
EF
1 SIG

Transmitted light detected by the photodiode and the detection current "Is" is converted into voltage signal by the amplifier and the feedback resistor R018.

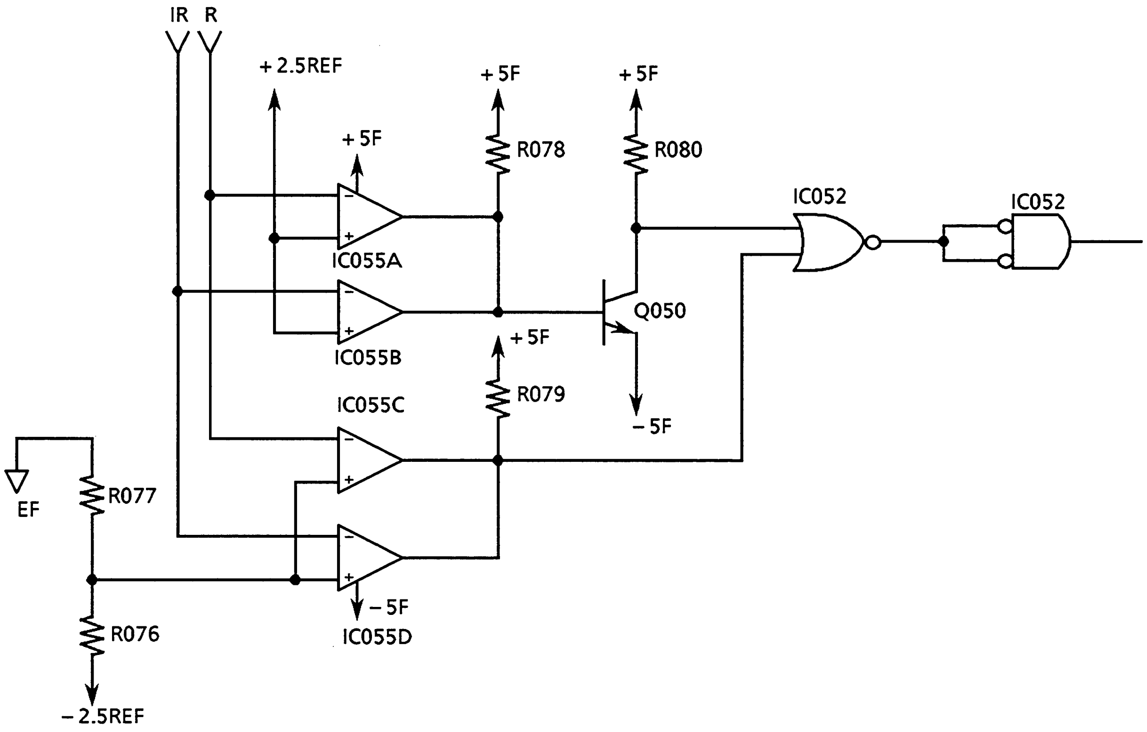
After being DC cut by the capacitor C009, voltage signal is amplified to a specified level by the auto gain control circuit consists of the IC switch IC006 and resistors.

AGC (Auto Gain Clock signal) stops which is triggered by the auto gain control circuit when R or IR signal comes into a specified range.

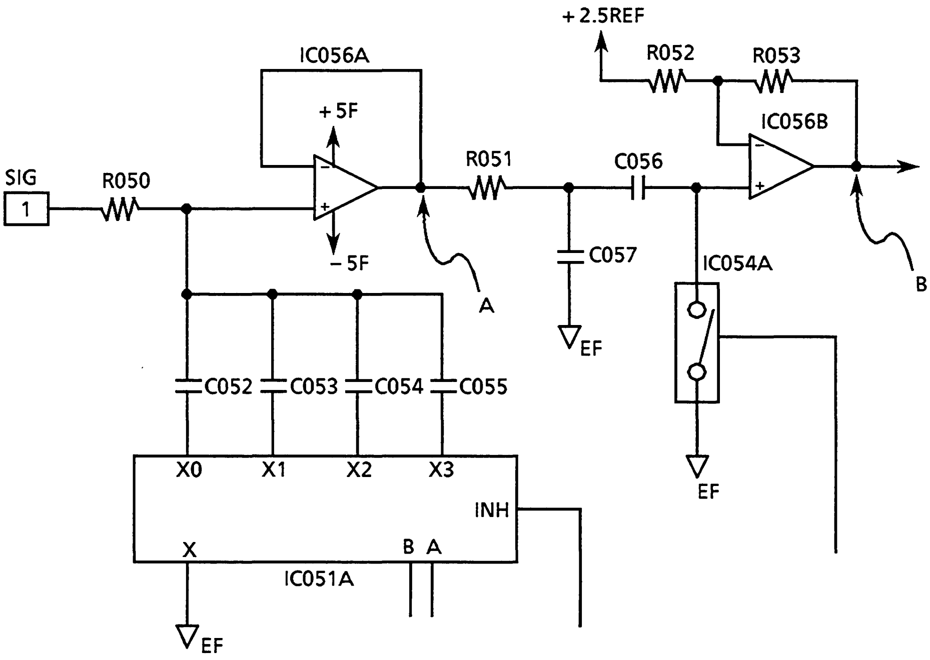
◆ Comparator for Auto Gain Control

The comparator controls the AGC (Auto Gain Clock signal) on/off or the auto gain control circuit.

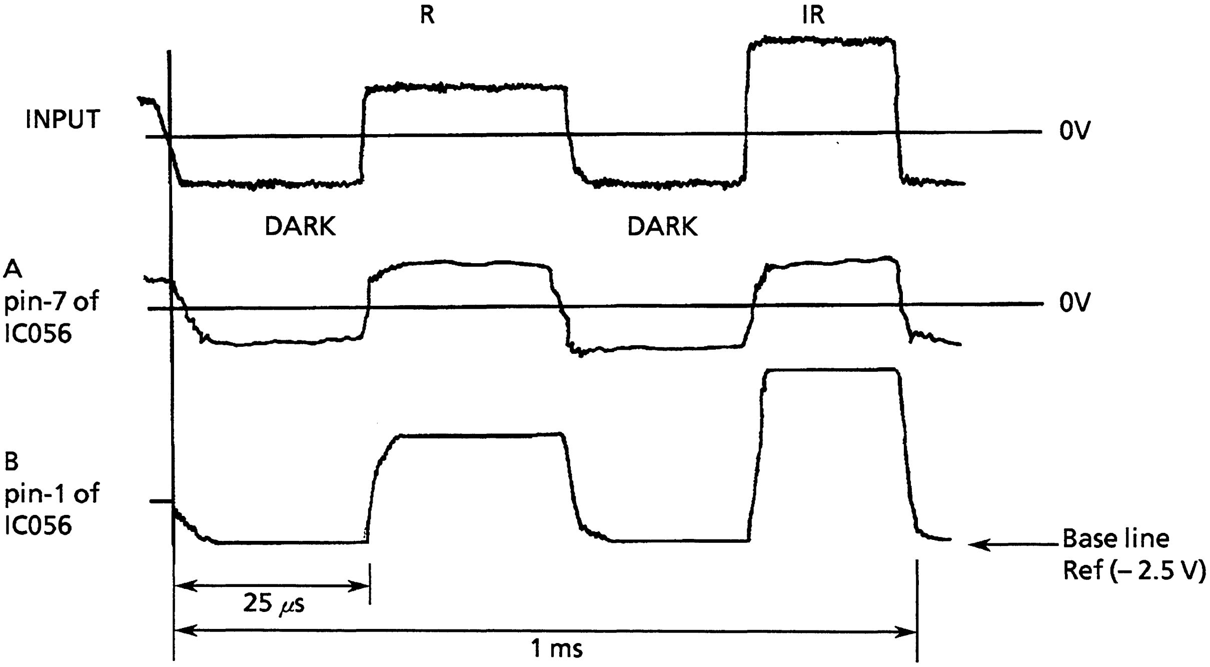
When either R or IR signal comes into a range from −1 V to +2.5 V, the output pin-4 of the IC052 turns to LOW to stop the AGC signal.


IR
R
+2.5REF
+5F
+5F
+5F
R078
R080
IC052
IC052
IC055A
IC055B
Q050
+5F
R079
IC055C
-5F
EF
R077
R076
-5F
IC055D
-2.5REF

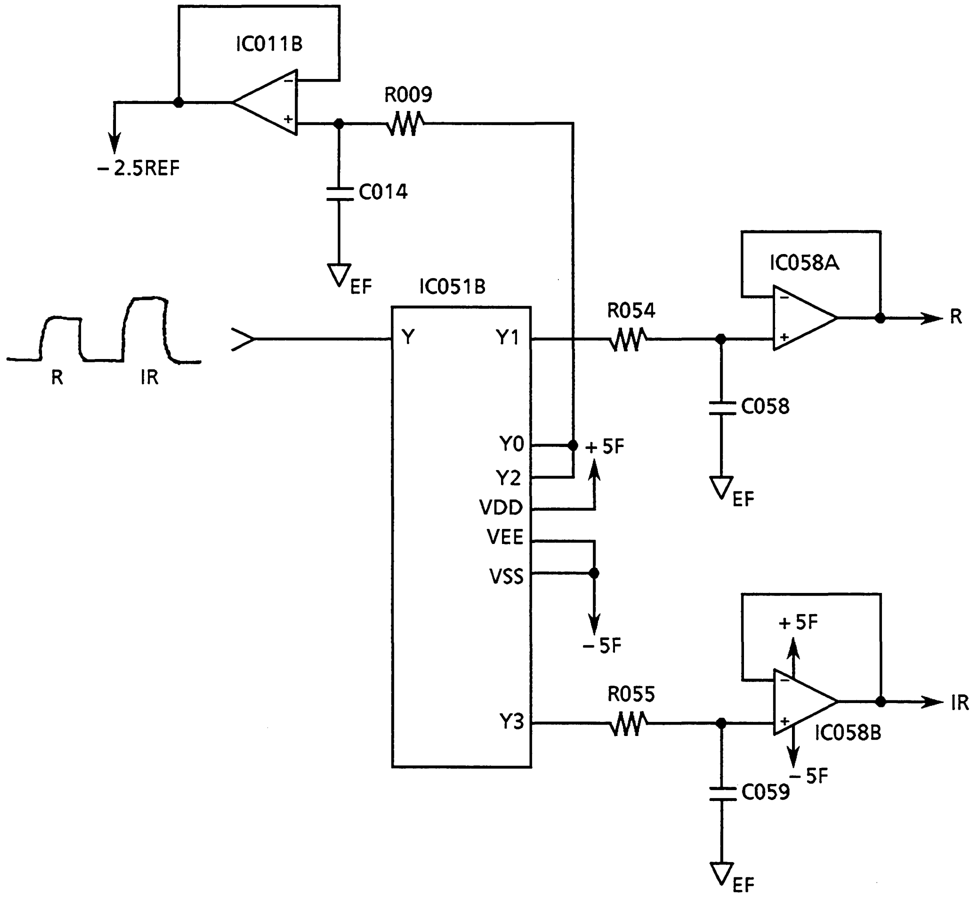
◆ Time Sharing Filter with Base Hold Circuit (Sub Board)


+2.5REF
IC056A
R052
R053
+5F
IC056B
R051
C056
SIG
R050
1
-5F
C057
IC054A
B
A
EF
C052
C053
C054
C055
X0
X1
X2
X3
INH
EF
X
B A
IC051A
EF

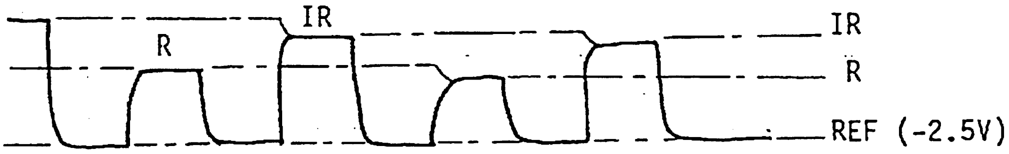
This circuit reduces noise component in the signal from the Main board and holds the baseline (signal level while there is no light emission) of the signal to −2.5V reference voltage (REF).



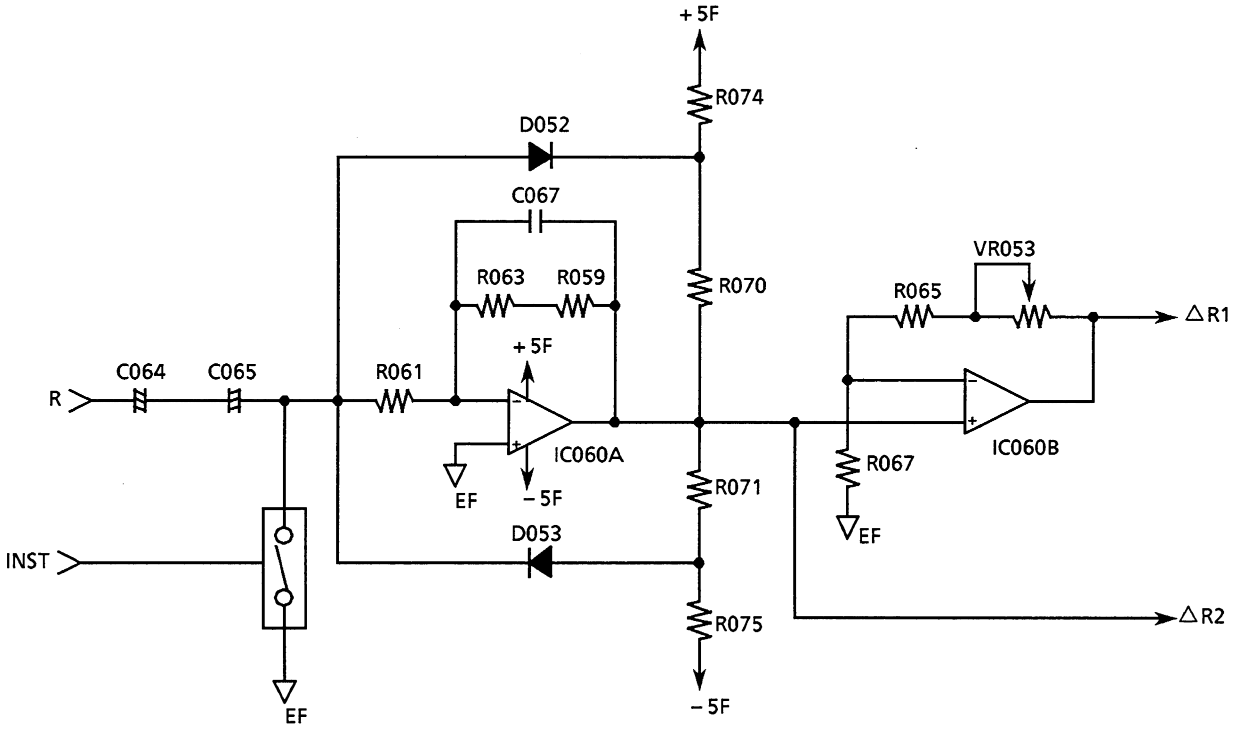
◆ Sample Hold Circuit


IC011B
R009
-2.5REF
C014
EF
IC051B
IC058A
R054
R
R
IR
Y
Y1
C058
Y0
+5F
Y2
VDD
VEE
VSS
EF
+5F
-5F
R055
IR
Y3
IC058B
-5F
C059
EF

This circuit sample holds the R, IR, and REF (baseline) signals of the base held signal as below:


IR
R
IR
R
REF (-2.5V)

◆ AC Amplifier with Auto Inst Function


+5F
R074
D052
C067
VR053
R063
R059
R070
R065
△R1
+5F
C064
C065
R061
R
IC060A
IC060B
R067
EF
-5F
R071
D053
INST
EF
R075
△R2
EF
-5F

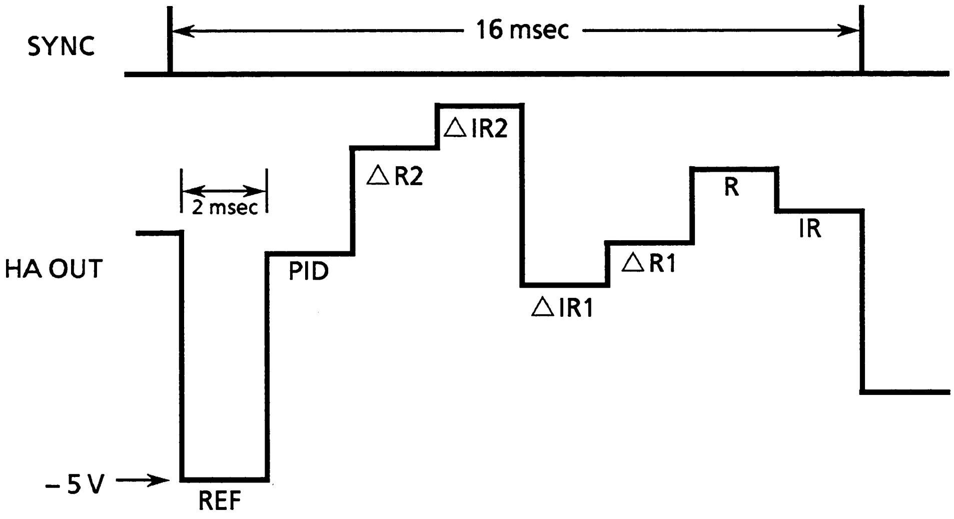
After being DC cut by the capacitors C062 and C063, the sample-held R signal is 5 times amplified by the IC059A to be the △R2 signal.

The diodes D050 and D051 recover the baseline when the signal level is saturated in the circuit (auto inso function).

The analog switch IC054B shortens the input line of the amplifier IC059A during auto gain control so that the signal level can quickly recover after the auto gain control is released. △R2 signal is 8 times amplified by the IC059B into the △R1 signal.

Above operations are applied to the IR signal in the same manner applied to the R signal.

◆ Output Timing


SYNC
16 msec
HA OUT
2 msec
PID
△R2
△IR2
△IR1
△R1
R
IR
-5V
REF

◆Adjustment

Volume on the PC boards are for gain adjustment of amplifiers. If you replace resistors concerning amplification gain, volumes should be readjusted.

There is no need to adjust the volumes when IC chips are replaced.

3-4-7 EEG Head Amp (AE-800PA) Boards, UP-0421 & 0422

The AE-800PA consists of UP-0421 EEG main board mounting, an EEG, control, output and floating power supply circuits, and UP-0422 EEG sub board mounting an amplifier processing circuit.

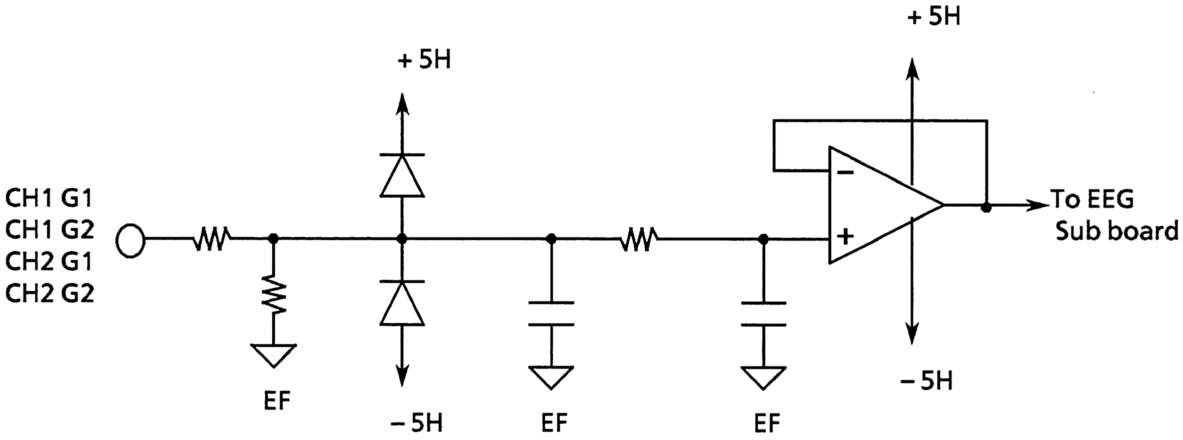
● UP-0421 EEG main board

Protection filters protect the circuits against large input generated by an ESU and defibrillator, etc. EEG input signals after the protection filters are transferred to the EEG sub board, and amplified, filtered and then returned to the EEG main board. Two EEG signals are time shared every 4msec into EEG1 and EEG2 output signals of the AE-800PA EEG head amplifier. Each buffer output is fed back to the EEG neutral electrode terminal (N) to increase the CMRR(Common Mode Rejection Ratio) to be called Reference Feedback for later descriptions.

● UP-0422 EEG sub board

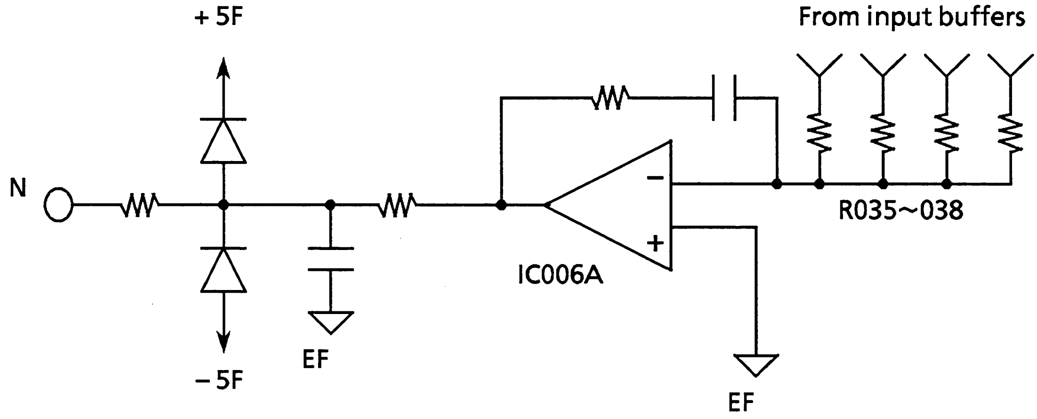
The UP-0422 consists of pairs of total 5000 gain amplifiers, 35Hz high-cut filters and AC interference filters. 0.3sec time constant is determined in this block.

◆ Input Buffer on the UP0421 Main Board



Two CR high-cut filters attenuate noise component in the EEG signal. Resistors limit large current and diodes limit large voltage (from ESU, defibrillator, etc.) to protect against damage of the circuit.

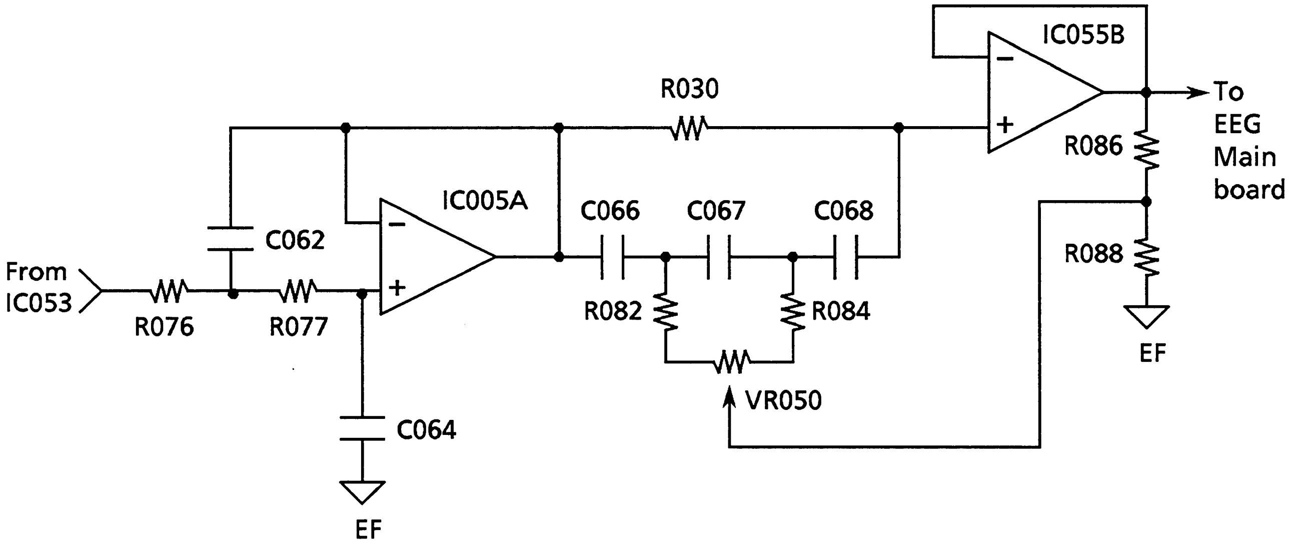
◆ Reference Feedback



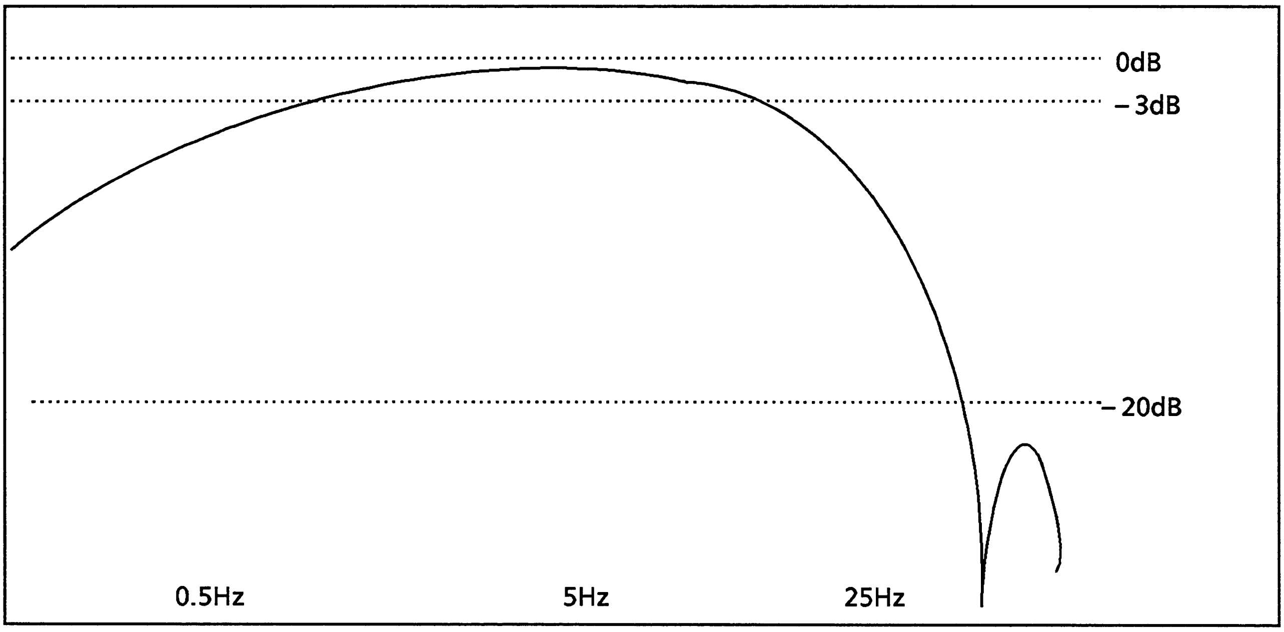
As the EEG signal is amplified by the differential amplifier, theoretically it is not interfered by common mode noise. However, due to variation in electrode impedance and electronic devices used, difference between the phases of the common mode component appears at the EEG amplifier output as noise.

By feeding back (negatively) each buffer output to the neutral electrode terminal(N), common mode component referred to the floating ground (EF) is reduced and the CMRR is increased.

◆ High-cut Filter and AVC Filter on the UP-0422 EEG Sub Board

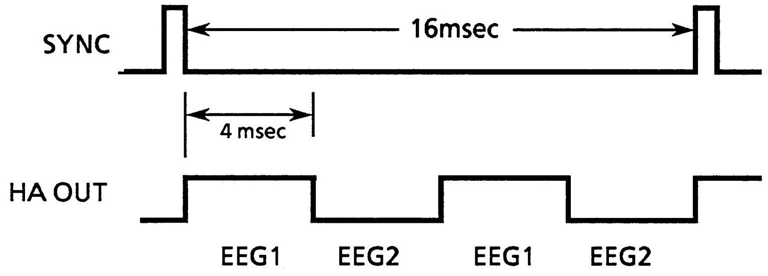

From IC053
R076
R077
C062
C064
EF
IC005A
R030
C066
C067
C068
R082
R084
VR050
IC055B
R086
R088
EF
To EEG Main board

Two stage high-cut filters consisting of IC055A, C062, C064, R076 and R077, and AC filter consisting of IC005B, C066, C067, C068, R080, R082, R084, R086, R088 and VR050 filter high frequency components and AC noise in the EEG signal. Total frequency characteristics of the filters is shown below.



◆ Timing of the Output Signals

This EEG head amplifier outputs in the following timing

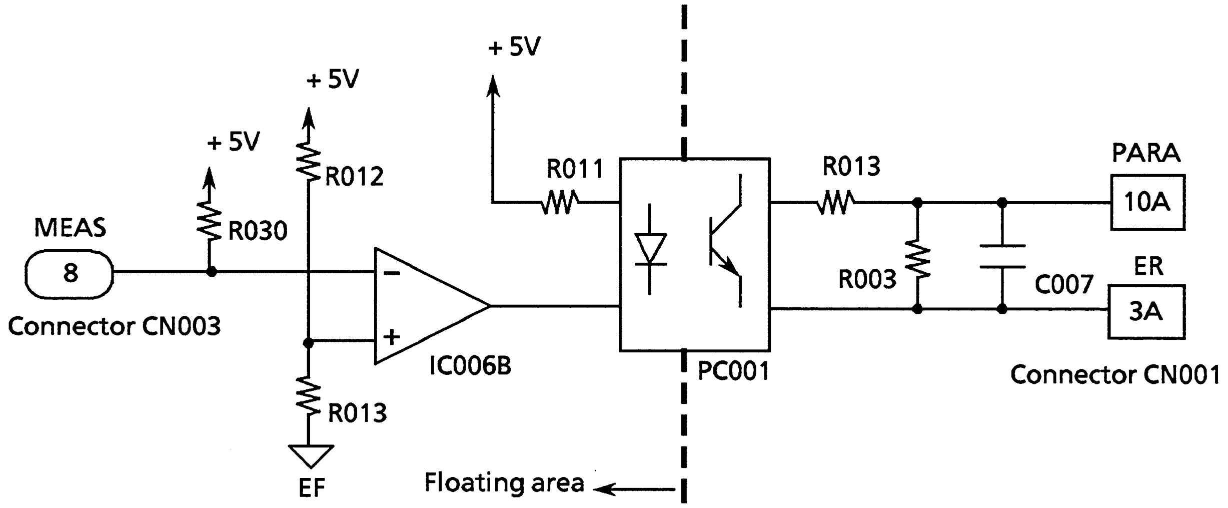

SYNC
16msec
4 msec
HA OUT
EEG1
EEG2
EEG1
EEG2

* Refer to the pages of BP head amplifier for signal signal modulation/demodulation between the floating area and grounded area.

◆ PAPA Signal Generating Circuit

Connection and disconnection of the EEG cable change the PARA voltage as below:

+1.7V ±40mV .... not connected
+1.9V ±40mV .... connected


+5V
+5V
+5V
R012
R030
MEAS
8
Connector CN003
R011
R013
PARA
10A
R003
C007
ER
3A
IC006B
PC001
Connector CN001
R013
EF
Floating area

When the EEG cable is not connected, comparator input pin-6 of the IC006B is pulled up to +5F through the R030, and the comparator outputs level L.
At this condition, the PC001 photocoupler is conductive and the resistance (PARA resistance) across the PARA and ER terminals is a parallel value of the R004 and R003, and the PARA voltage reads +1.7V. This voltage indicates EEG non measuring condition.

When the cable is connected, the PC001 is not conductive, the PARA resistance is R003 only, and PARA voltage reads +1.9V. This voltage indicates EEG measuring condition.

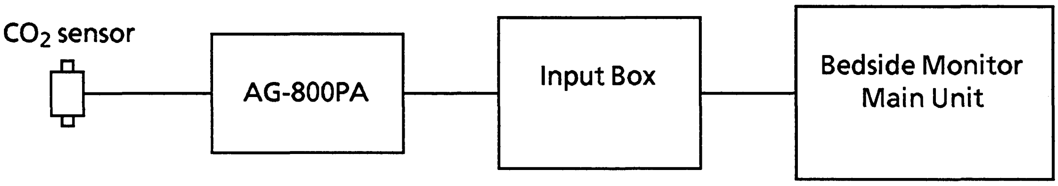
3-4-8 CO_2 Head Amp (AG-800PA) Boards, UP-0588 & 0589 and TG-706P

◆ General

AG-800PA is one of the head amplifiers for the BSM-8000 series bedside monitors to measure CO_2 partial pressure of expired gas of a patient with TG-706P CO_2 sensor.

◆ System Connection

CO_2 head amplifier is inserted into the input box of the bedside monitor and the CO_2 sensor is connected to the head amplifier.



◆ Description of Each Function Block

• UP-0588 CO_2 Main board

Power (DC-DC) line is a power to drive the CO_2 sensor TG-706P and DRIVER is a electrical current driver of a motor in the sensor.

S-P and D/A circuit reads the linearization data (compensation factor for CO_2 calculation, differs in each sensor) which written in the ROM in the sensor.

TIMING CONTL 1 circuit controls output timing for reading linearization data, and HAOUT output timing.

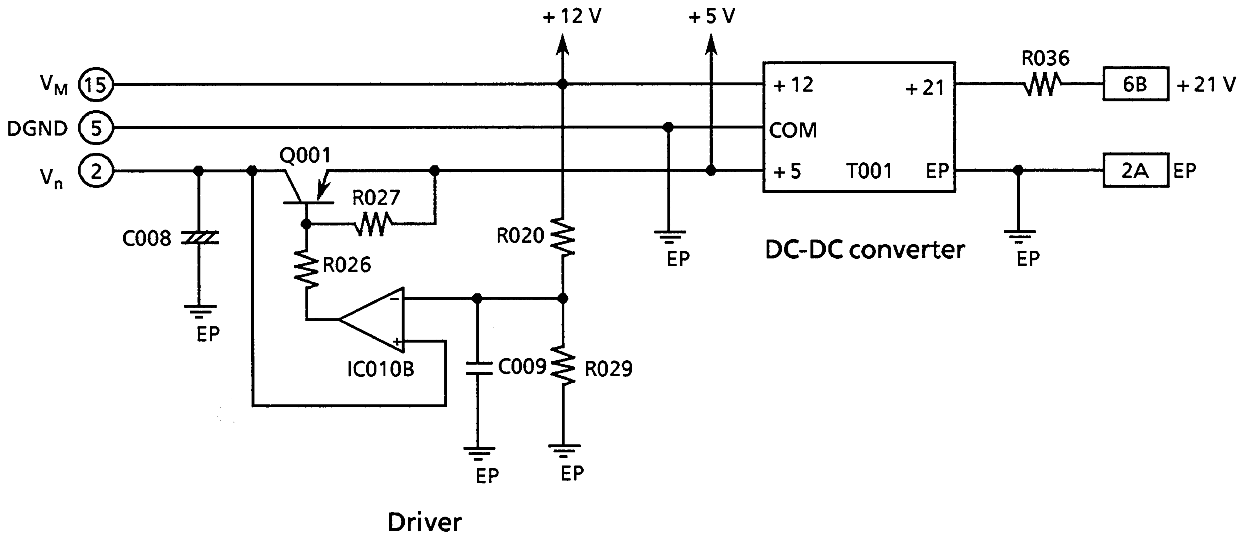
• UP-0589 CO_2 Sub board

ZERO SHIFT circuit shifts the VAC sensor signal baseline to – 5REF (-4.75V) in order to widen dynamic range of the signal.

P/H (peak-hold) circuit holds amplitude of the signal based on – 5REF reference voltage.

3.75S/H (Sample and hold) and 4.3S/H circuits sample each V3.7 signal and V4.3 signal in the VAC signal.

◆ Sensor Driver Power (DC-DC, DRIVER on CO_2 Main Board)

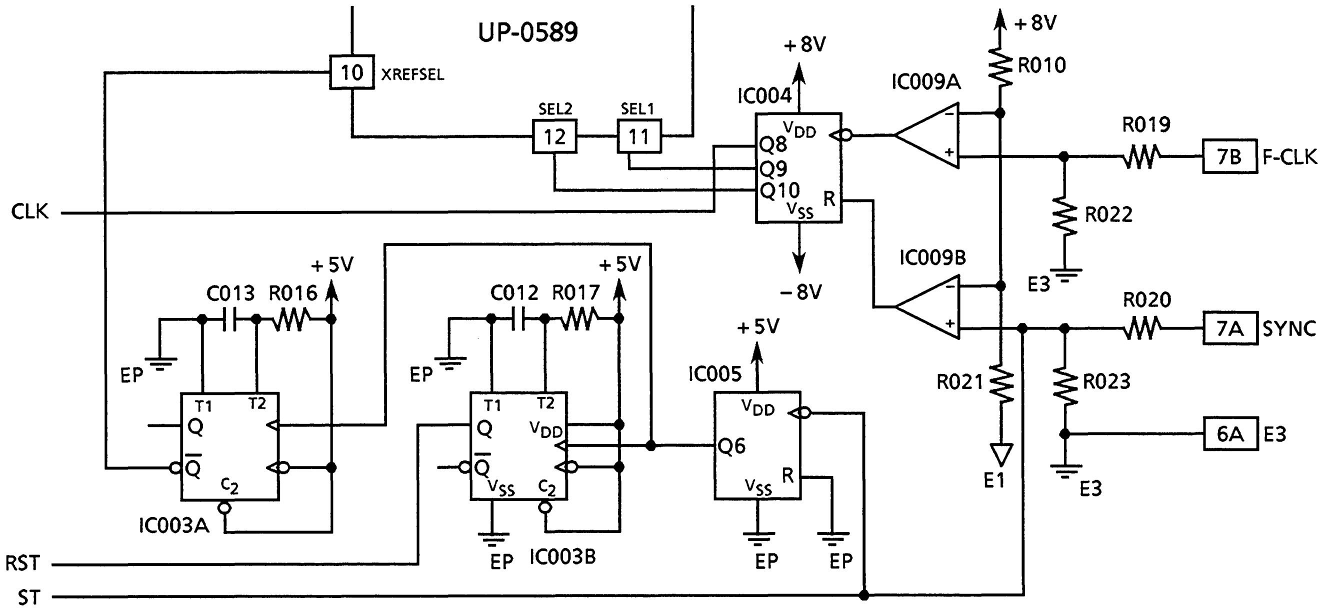

+12 V
+5 V
V_M 15
DGND 5
V_n 2
Q001
R027
C008
R026
EP
IC010B
C009
R020
R029
+12
+21
COM
+5
T001
EP
R036
6B
+21 V
2A
EP
DC-DC converter
Driver

DC-DC (T001) is a DC-DC converter that generates +12 V and +5 V voltages from +21 V unregulated power.

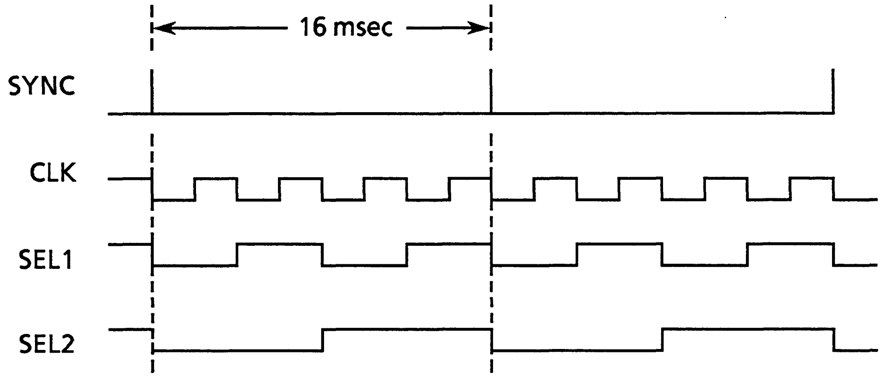
+12 V is a power for an infrared ray lamp in the CO_2 sensor of 120mA continuous load current and +12 V ±1% stability.

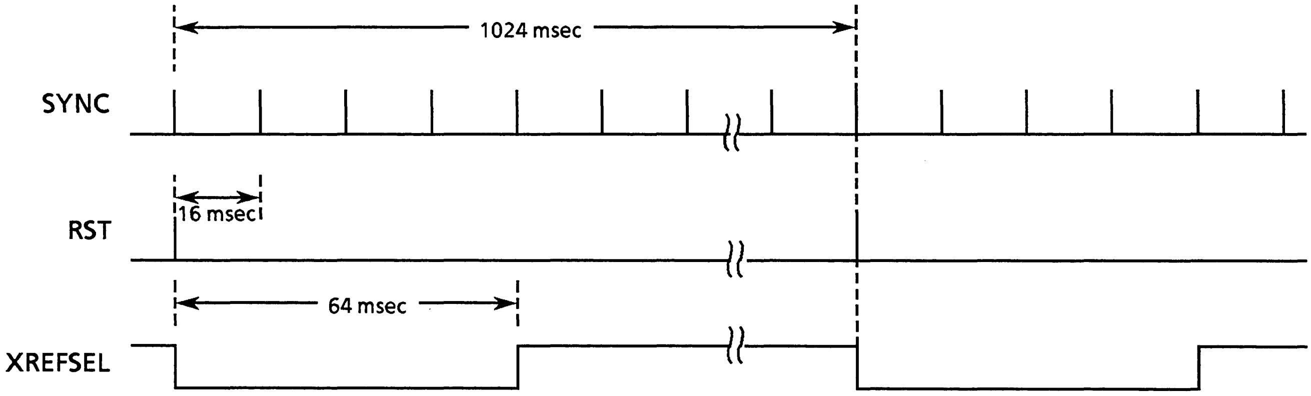
+5V drives a motor and digital IC devices in the sensor. The circuit indicated with DRIVER drives the motor.

◆ TIMING CNTL 1 (CO_2 Main Board)

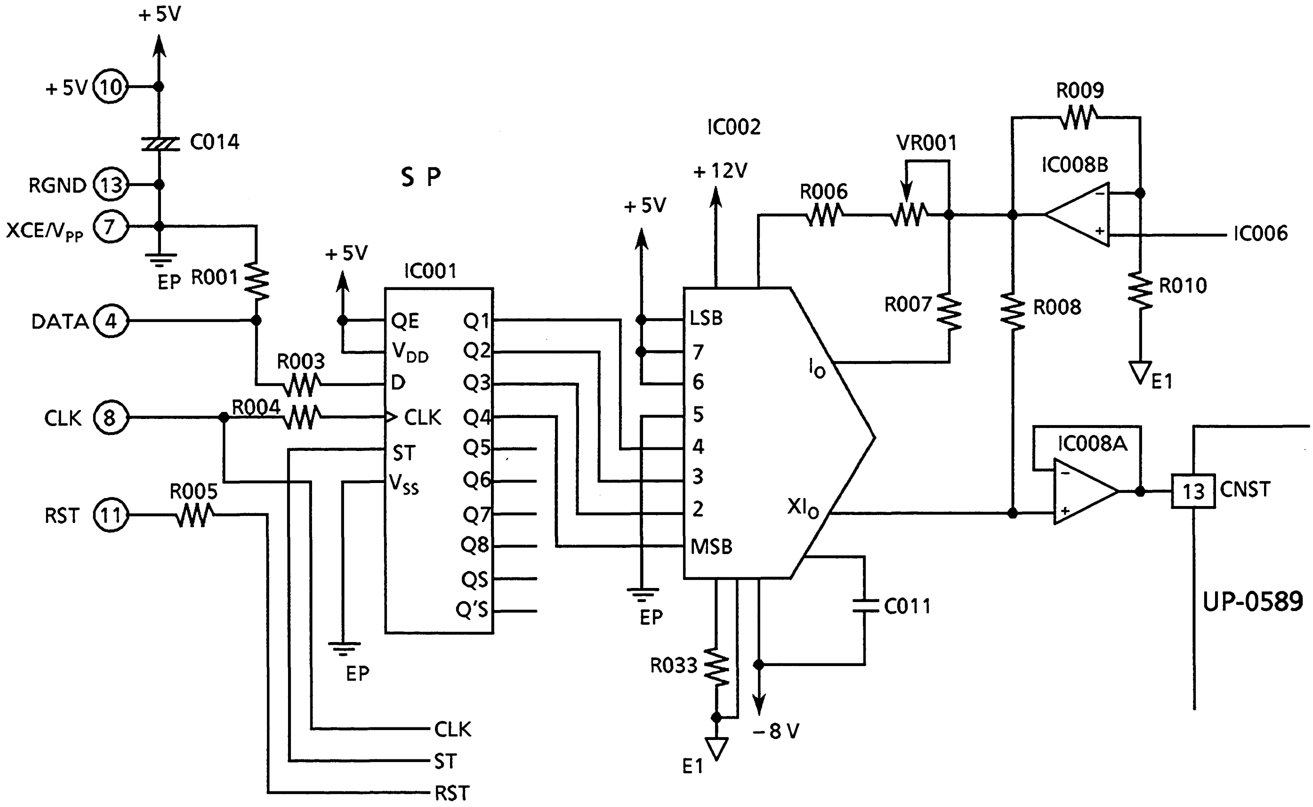

UP-0589
10
XREFSEL
SEL2
SEL1
12
11
+8V
IC004
Q8
Q9
Q10
VDD
VSS
R
-8V
IC009A
IC009B
+8V
R010
R019
7B
F-CLK
R022
E3
R020
7A
SYNC
R021
R023
6A
E3
E1
E3
CLK
+5V
C013
R016
EP
T1
T2
Q
Q̄
C2
IC003A
+5V
C012
R017
EP
T1
T2
Q
VDD
Q̄
VSS
C2
EP
IC003B
+5V
IC005
VDD
Q6
VSS
R
EP
EP
RST
ST

* SEL1, SEL2	Clock signals to control HAOUT signal output timing.
* XREFSEL	Control signal to output data to HAOUT by switching -5REF signal and linearization data.
* CLK	Clock signal to control ROM and S/P (Serial to Parallel) converter in the sensor.
* RST	Signal to reset the ROM in the sensor.
* ST	Signal to control S/P conversion.


16 msec
SYNC
CLK
SEL1
SEL2


1024 msec
SYNC
RST
16 msec
64 msec
XREFSEL

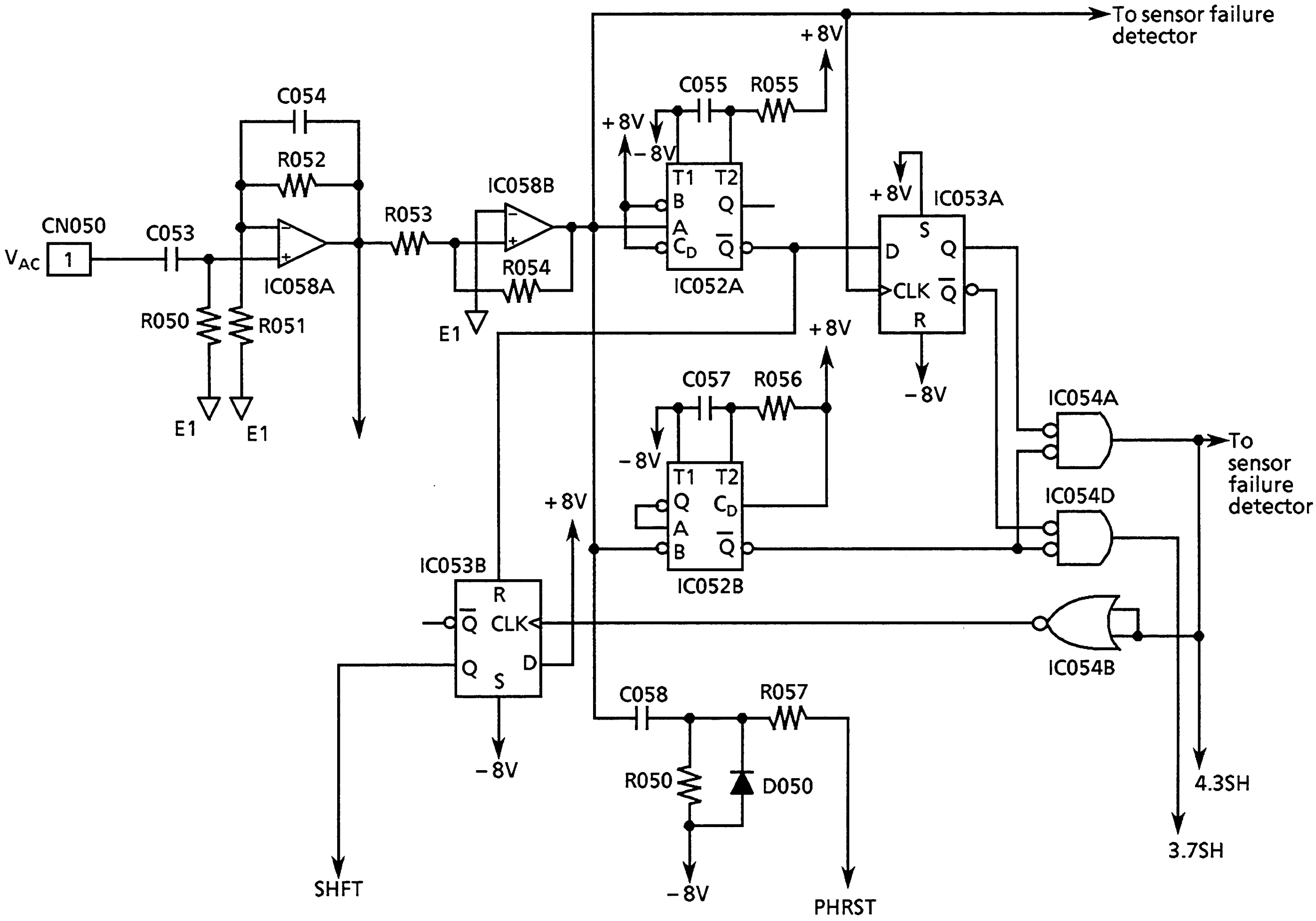
◆ S/P Conversion and D/A Conversion (CO_2 Main Board)


+5V
+5V ⑩
C014
RGND ⑬
XCE/VPP ⑦
EP
R001
DATA ④
R003
CLK ⑧
R004
R005
RST ⑪
S P
+5V
IC001
QE
VDD
D
CLK
ST
VSS
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
QS
Q'S
EP
CLK
ST
RST
+5V
EP
IC002
+12V
LSB
7
6
5
4
3
2
MSB
Io
XIo
R033
E1
-8V
C011
R006
VR001
R007
R008
R009
IC008B
R010
E1
IC006
IC008A
13
CNST
UP-0589

Linearization data (DATA) stored in the ROM in the sensor is output from the ROM in synchronization with CLK signal in serial format data. This serial format data is S/P converted into parallel format data in synchronization with ST signal.
Relation between the linearization data and D/A output is as below.

Linearized data	D/A out (V)	Linearized data	D/A out (V)
0 0 0 0	−4.80	1 0 0 0	+0.32
0 0 0 1	−4.16	1 0 0 1	+0.96
0 0 1 0	−3.52	1 0 1 0	+1.60
0 0 1 1	−2.88	1 0 1 1	+2.24
0 1 0 0	−2.24	1 1 0 0	+2.88
0 1 0 1	−1.60	1 1 0 1	+3.52
0 1 1 0	−0.96	1 1 1 0	+4.16
0 1 1 1	−0.32	1 1 1 1	+4.80

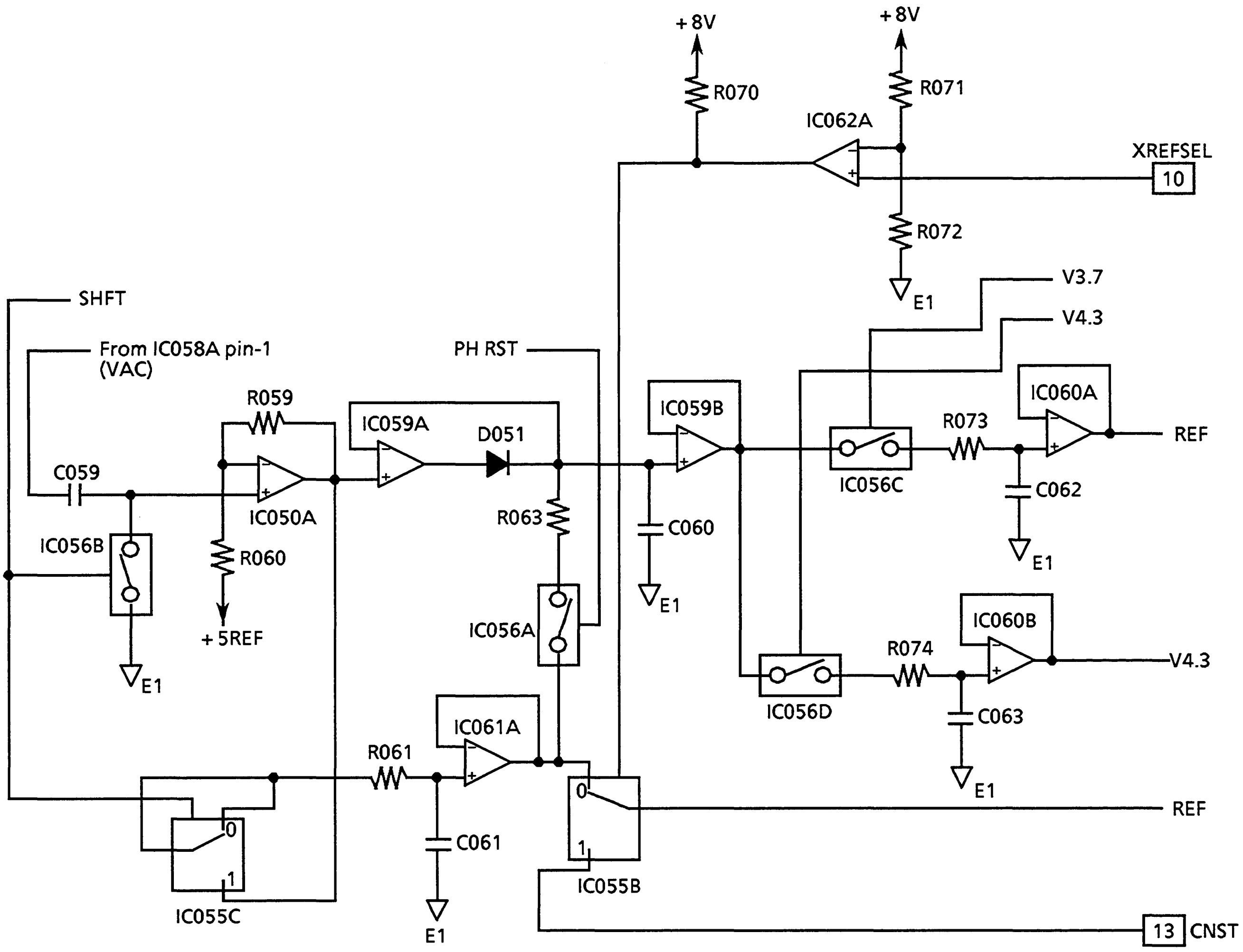
◆ TIMING CONTL 2 (CO_2 Sub Board)


To sensor failure detector
+8V
C054
C055
R055
R052
+8V
-8V
IC058B
T1
T2
B
Q
A
C_D
$\overline{Q}$
+8V
IC053A
S
D
Q
CLK
$\overline{Q}$
R
CN050
C053
R053
V_{AC}
1
IC058A
R054
IC052A
R050
R051
E1
E1
E1
+8V
C057
R056
-8V
IC054A
-8V
To sensor failure detector
T1
T2
Q
C_D
A
B
$\overline{Q}$
+8V
IC054D
IC052B
IC053B
R
$\overline{Q}$
CLK
Q
D
S
IC054B
C058
R057
-8V
R050
D050
4.3SH
3.7SH
SHFT
-8V
PHRST

* SHFT	Control signal to shift V_{AC} signal baseline in the ZERO SHIFT circuit to −5REF (−4.75 V) level.
* PH RST	Pulse to reset Peak-Hold circuit following the ZERO SHIFT circuit.
* 3.7SH	Sampling pulse of V3.7 signal in the V_{AC} signal.
* 4.3SH	Sampling pulse of V4.3 signal in the V_{AC} signal.

Refer to page 3.155 for CO_2 signal demodulation timing.

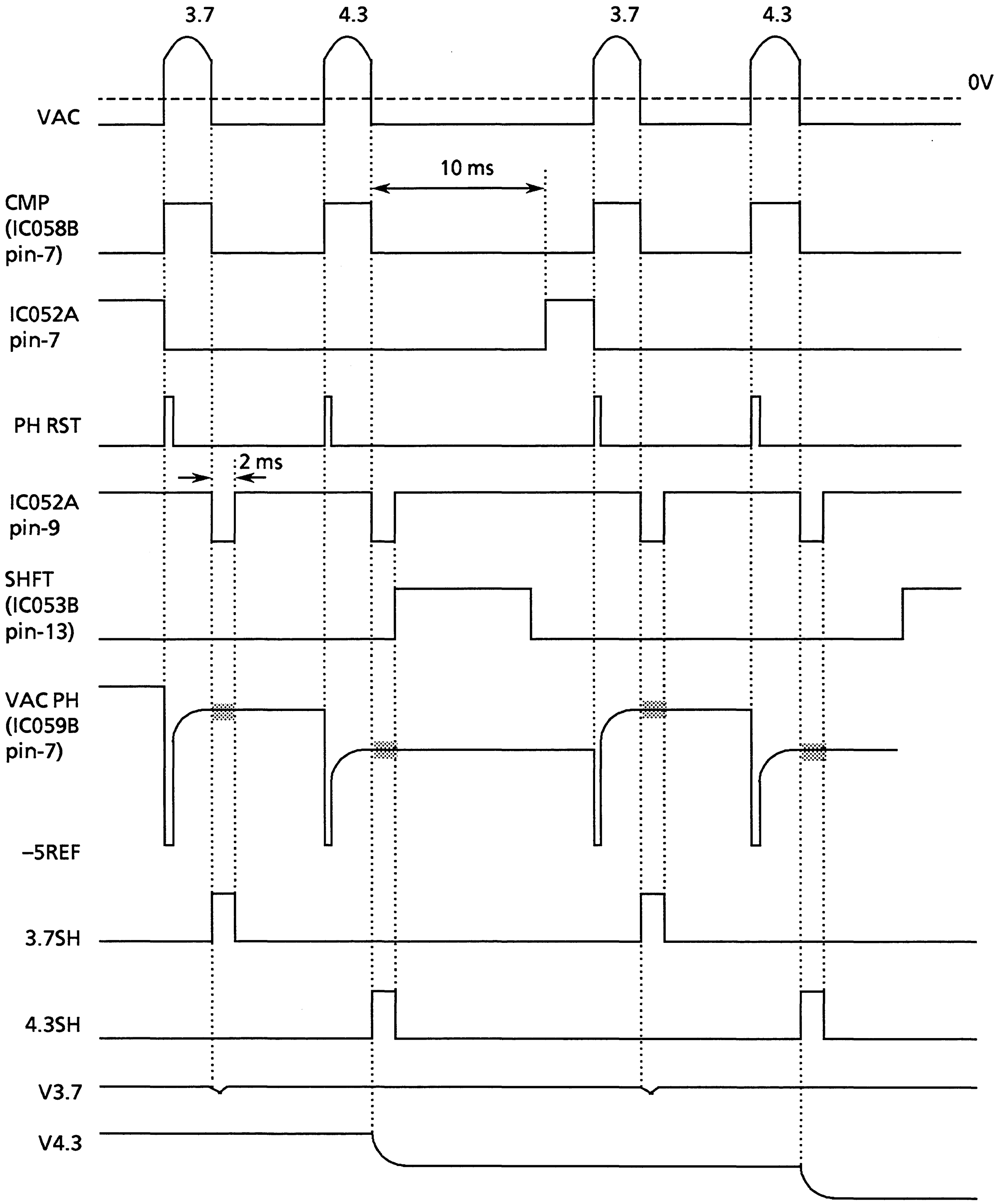
◆ V3.7, V4.3 and REF Signal Detection Circuit (CO_2 Sub Board)


+8V
+8V
R070
R071
IC062A
XREFSEL
10
R072
E1
V3.7
V4.3
SHFT
From IC058A pin-1
(VAC)
PH RST
R059
IC059A
D051
IC059B
IC060A
R073
REF
C059
IC050A
R063
IC056C
C062
C060
IC056B
R060
E1
E1
+5REF
IC056A
IC060B
R074
V4.3
E1
IC056D
C063
IC061A
R061
E1
0
1
REF
0
1
C061
IC055B
IC055C
E1
13
CNST

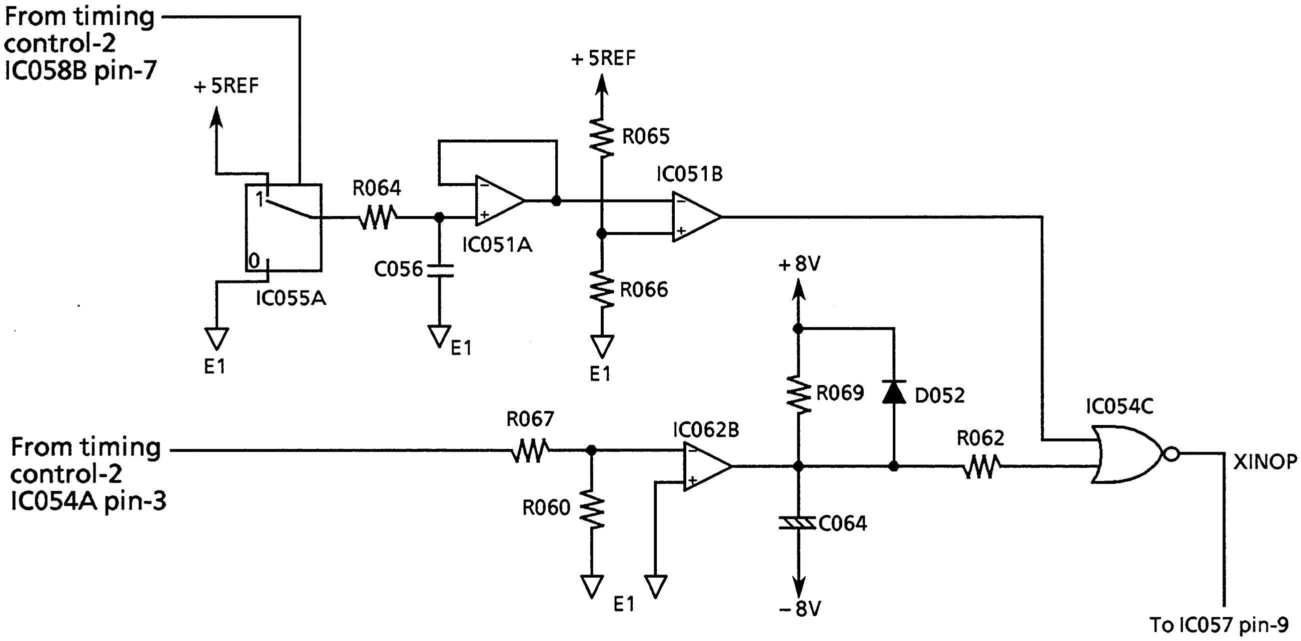
VAC signal baseline is shifted (IC050A pin-1) into – 5REF signal (IC061A pin-1) by SHFT pulse. CNST signal is D/A converted linearized data. This CNST and – REF signal output as REF signal by switching CNST signal and – 5REF signal by XRESET signal.

The IC059A peak-holds the amplitude of V_{AC} signal based on – 5REF signal and the IC060A and IC060B sample hold V3.7 and V4.3 signals composing of V_{AC} signal and output the signals as V3.7 and V4.3.

◆ CO_2 Signal Demodulation Timing


3.7
4.3
3.7
4.3
0V
VAC
10 ms
CMP (IC058B pin-7)
IC052A pin-7
PH RST
2 ms
IC052A pin-9
SHFT (IC053B pin-13)
VAC PH (IC059B pin-7)
–5REF
3.7SH
4.3SH
V3.7
V4.3

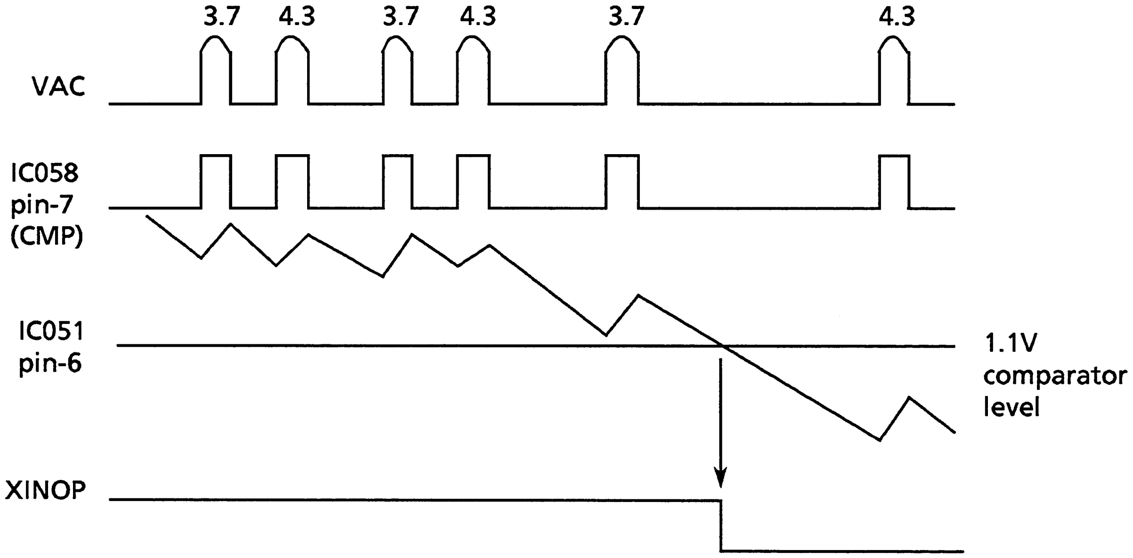
◆ Operation of Sensor Failure Detection


From timing control-2 IC058B pin-7
+5REF
+5REF
R065
IC051B
R064
IC051A
C056
IC055A
+8V
R066
E1
E1
E1
R069
D052
IC054C
R067
IC062B
R062
From timing control-2 IC054A pin-3
XINOP
R060
C064
E1
-8V
To IC057 pin-9

In normal operation, both IC054 pin-8 and pin-9 are "L" (-8V) logic level and pin-10 XINOP (Inoperative) output is "H" level.

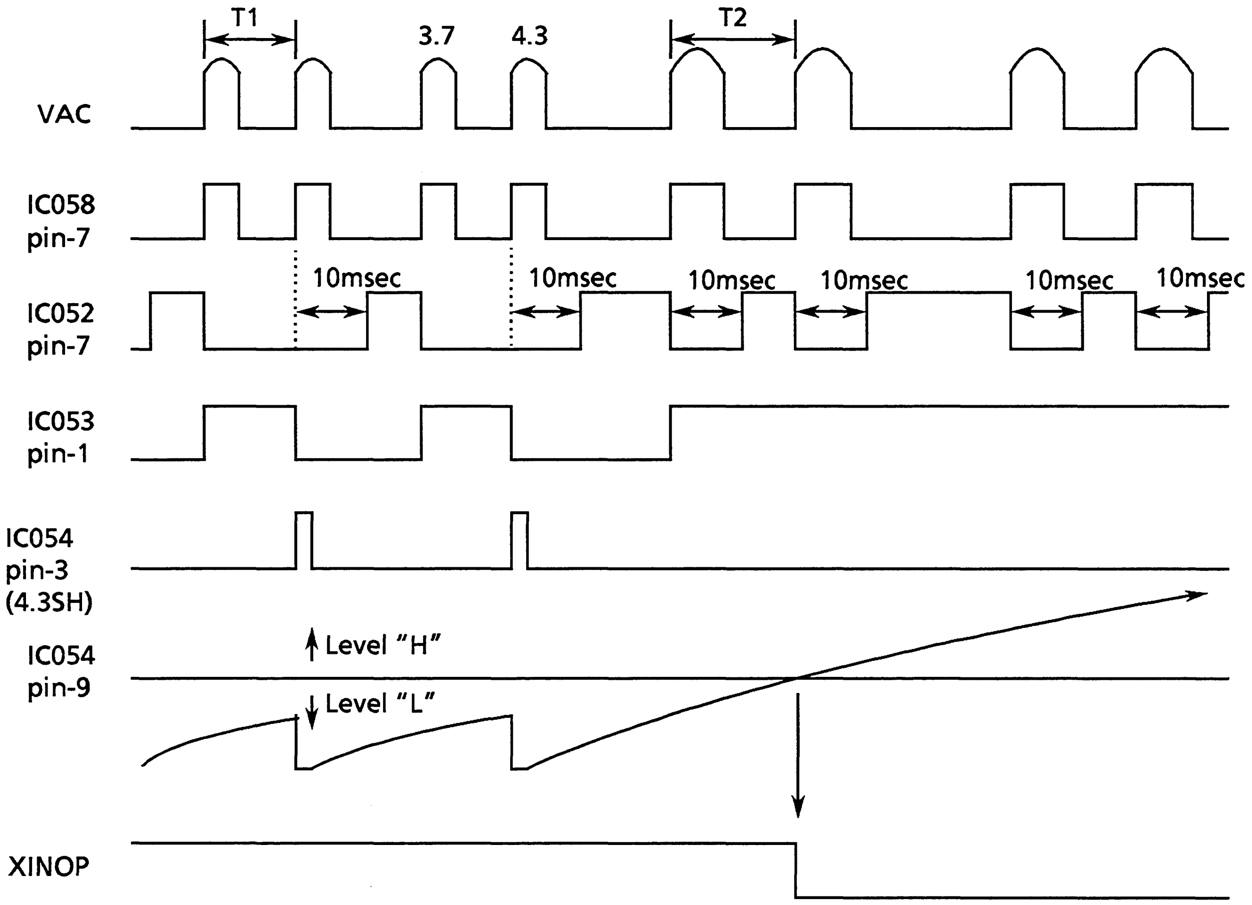
• When there is no 3.7 or 4.3 or both in the V_{AC} signal

When there is no 3.7 or 4.3 or both in the V_{AC} signal, CMP pulse is not generated or number of pulses decreases to half, and charging time of the C056 becomes short, then the comparator (IC051B) outputs "H" level and XINOP signal becomes "L". The head amplifier output signal HAOUT is – 5V in this condition.


3.7
4.3
3.7
4.3
3.7
4.3
VAC
IC058 pin-7 (CMP)
IC051 pin-6
1.1V comparator level
XINOP

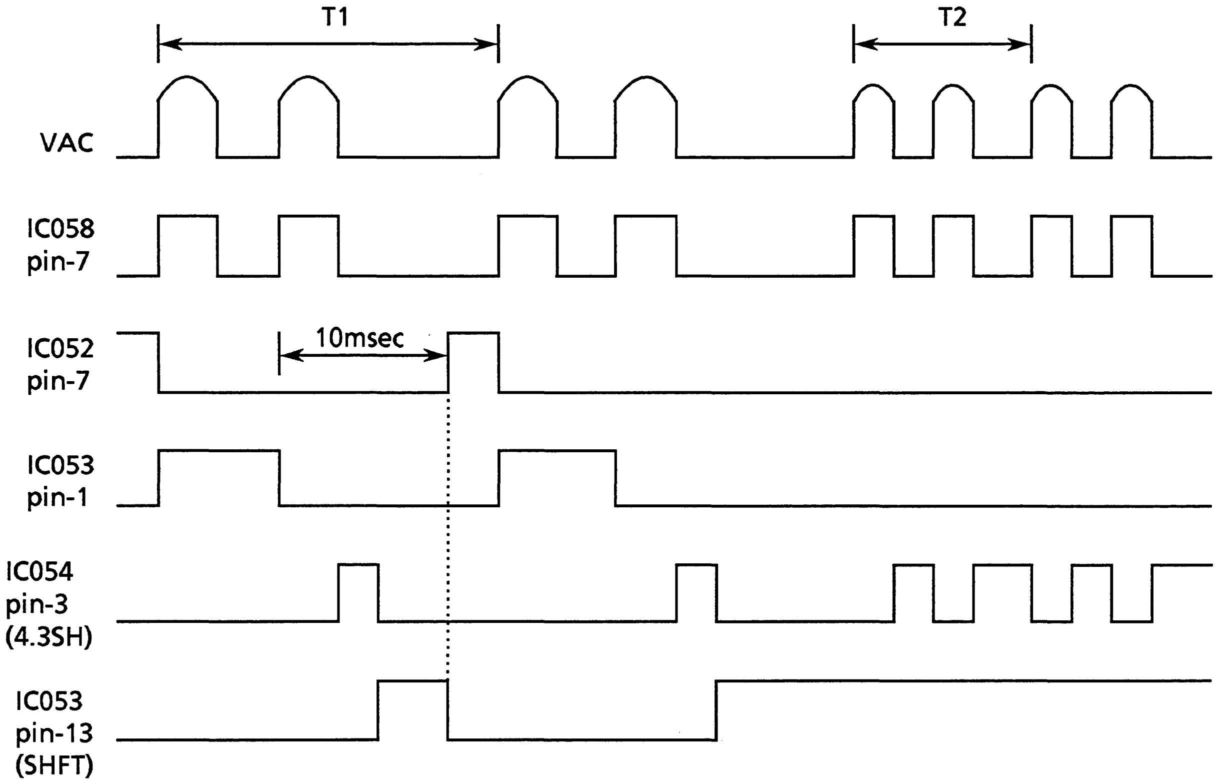
• When the V_{AC} output interval is prolonged (decrease of motor revolution)

When the V_{AC} output interval T1 between 3.7 and 4.3 is prolonged it exceeds 10msec of one-shot time of IC052A, output of the IC053A (pin-1) becomes always "H" and the C064 is charged up by +8V, then XINOP signal turns to "L" and HAOUT head amplifier output becomes - 5V.

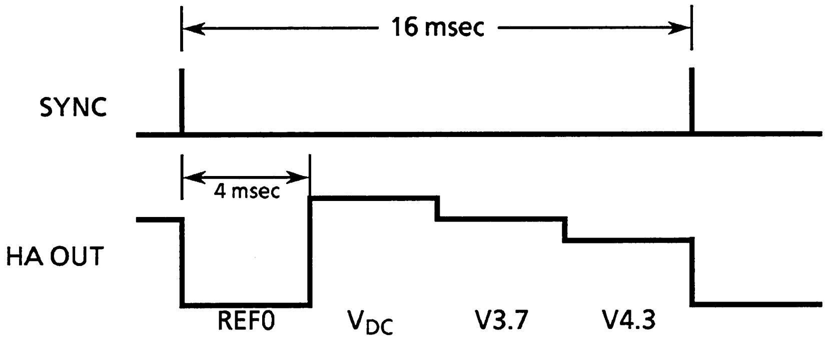

T1
3.7
4.3
T2
VAC
IC058 pin-7
10msec
10msec
10msec
10msec
10msec
10msec
IC052 pin-7
IC053 pin-1
IC054 pin-3 (4.3SH)
IC054 pin-9
Level "H"
Level "L"
XINOP

• When the V_{AC} output interval is shortened (increase of motor revolution)

When the interval T2 between the 3.7 and next 3.7, it becomes shorter than 10msec one-shot time of the IC052A output (pin-7) becomes "L" and SHFT pulse (IC053 pin-13 is fixed to "H". Then IC050A input pin-3 is fixed to E1 (ground) and head amplifier output HA4.3 becomes equal to – 5REF voltage.

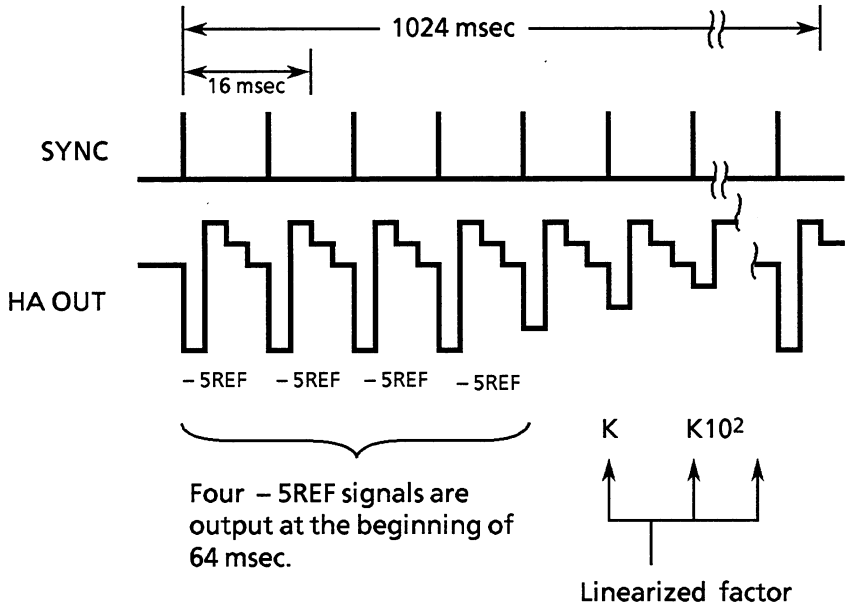

T1
T2
VAC
IC058 pin-7
IC052 pin-7
10msec
IC053 pin-1
IC054 pin-3 (4.3SH)
IC053 pin-13 (SHFT)

◆ **Timing of Output Signal**

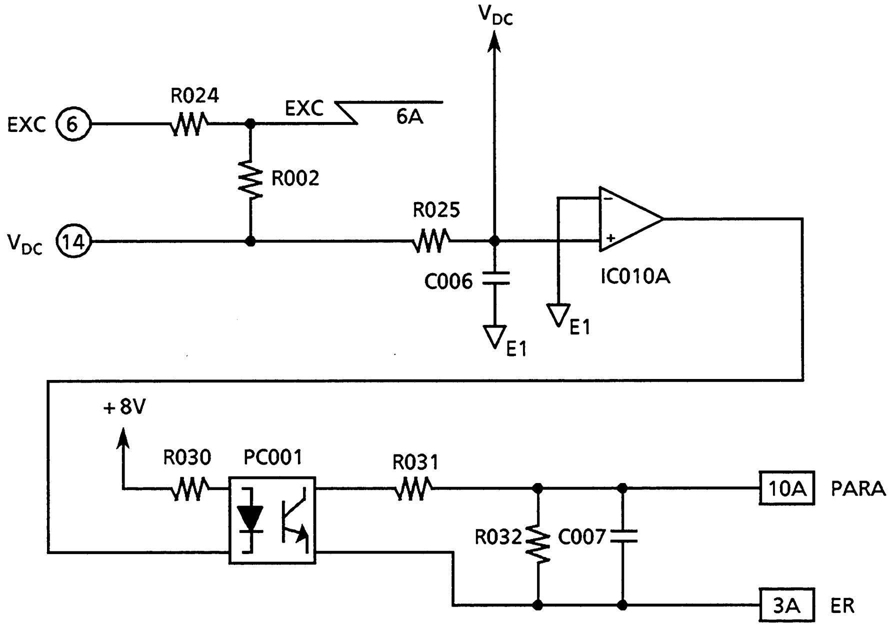

16 msec
SYNC
4 msec
HA OUT
REF0
V_{DC}
V3.7
V4.3

REF: -REF signal which is a reference of V3.7 and V4.3 signals and linearization data of each sensor required for CO_2 calculation are output for 4msec from the SYNC pulse every 16msec in a cycle of 1204msec.

- 5REF output range: - 4.75V ±0.2V


1024 msec
16 msec
SYNC
HA OUT
- 5REF
- 5REF
- 5REF
- 5REF
Four - 5REF signals are output at the beginning of 64 msec.
K
K10²
Linearized factor

◆ Unit Discrimination Signal (PARA Voltage)


VDC
R024
EXC
6A
EXC 6
R002
R025
VDC 14
C006
IC010A
E1
E1
+8V
R030
PC001
R031
10A
PARA
R032
C007
3A
ER

PARA (parameter) voltage changes when the CO_2 sensor is connected and disconnected as below.

Sensor	PARA voltage (V)
Connection	2.40 ±0.05
Disconnection	2.10 ±0.05

When the sensor is not connected, EXC (−5 V) is applied to the comparator input terminal (IC101A pin-3) and comparator output is "L". With this voltage, the photocoupler PC001 is conductive and 2.1V voltage attenuated with R031 and R032 resisters appears as PARA voltage at no sensor connection.

When the sensor is connected, +1 V to +5 V voltage is applied to the comparator input terminal (IC101A pin-3) and comparator output turns to "H". With this voltage PC001 becomes off and 2.4V appears as PARA voltage at sensor connection.

◆ TG-706P CO_2 Sensor

• General

The infrared ray which is absorbed by CO_2 gas (4.3um wavelength) and the infrared ray which is not affected by CO_2 gas (3.7us wave length) are used in the CO_2 sensor.

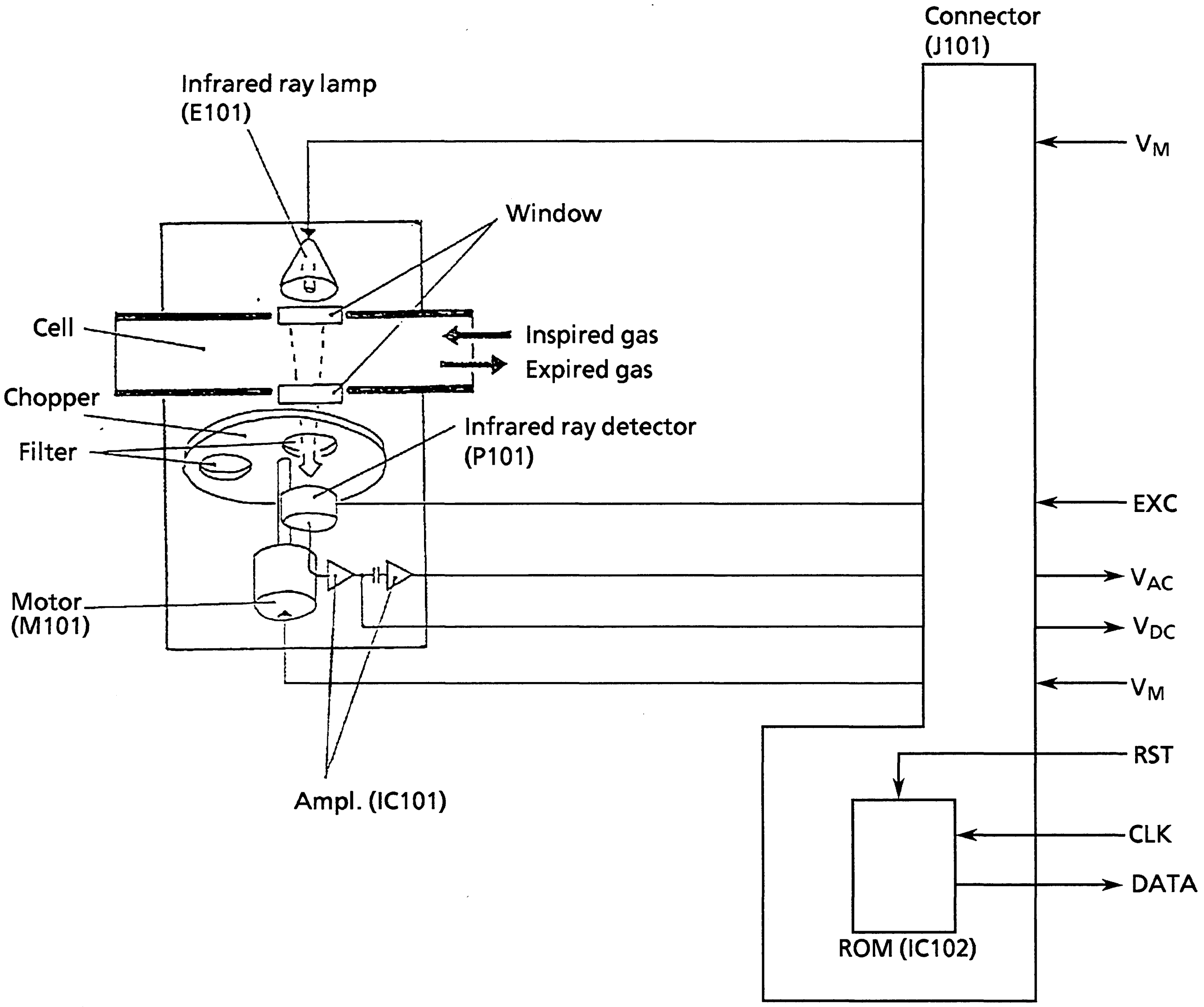
• Sensor output signals

The CO_2 sensor outputs three signals.

VDC	DC voltage for compensating signal drift due to temperature change of the sensor. It corresponds to resister value of the infrared ray detector.
VAC	AC voltage of light strength signal. The infrared ray that passes through respiratory gas in the cell and the filter is converted into a light strength signal after being converted to a resistance signal and then to an electrical signal. One rotation of the chopper is taken to be one cycle, and the signal (V4.3) through the 4.3um filter (altered CO_2 partial pressure) and the signal (V3.7) through the 3.7um filter (not affected by CO_2 gas, used for reference), are output alternatively. VAC signal is a mixture of the V4.3 and V3.7 signals.
DATA	Compensation coefficient to calculate CO_2 value, 256 bit serial data stored in ROM chip inside each CO_2 sensor.

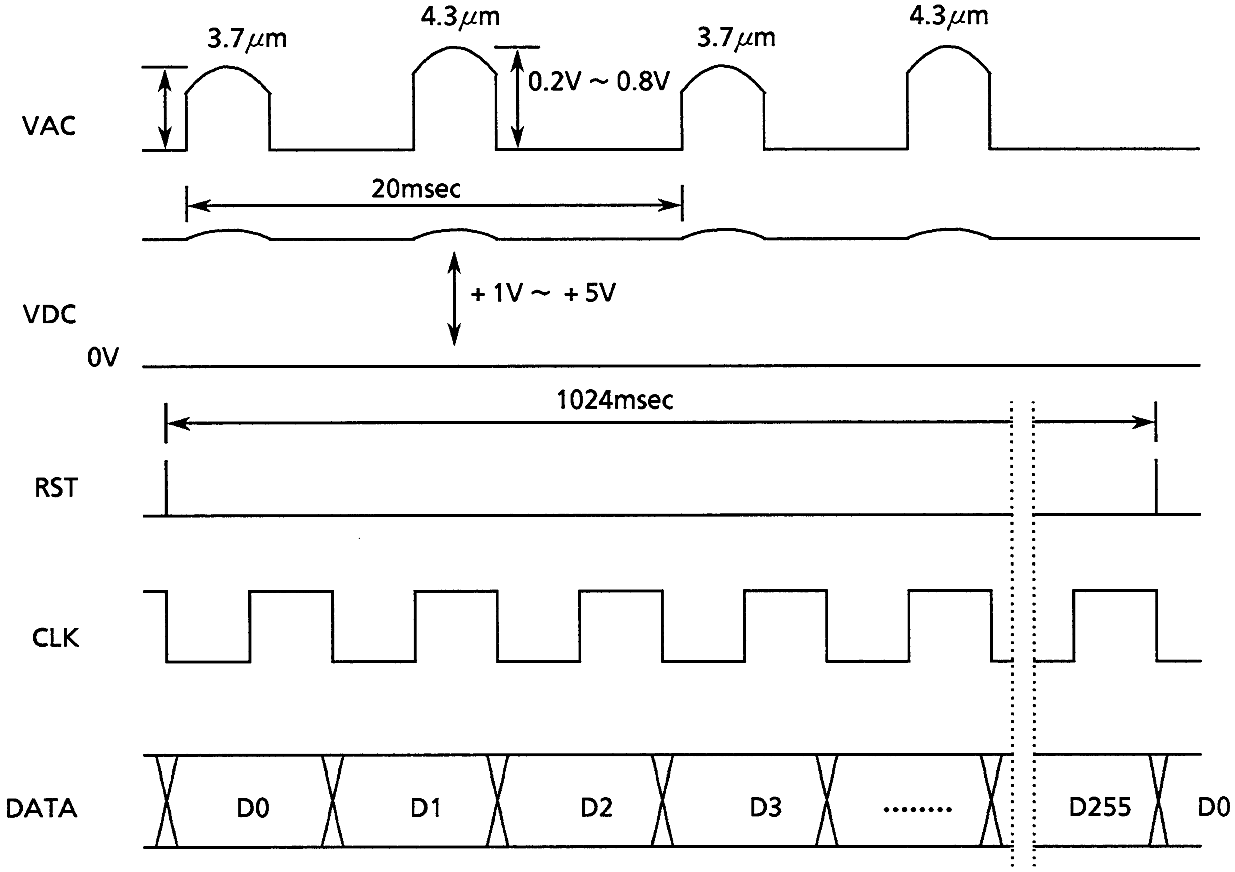
• Head amplifier output signals

The AG-800PA CO_2 head amplifier separates V4.3 and V3.7 signals from VAC signal and outputs DATA, VDC, V3.7 and V4.3 signals in order successively. DC voltage indicating infrared ray detector resistance value.


Connector
(J101)
Infrared ray lamp
(E101)
V_M
Window
Cell
Inspired gas
Expired gas
Chopper
Filter
Infrared ray detector
(P101)
EXC
V_{AC}
Motor
(M101)
V_{DC}
V_M
RST
Ampl. (IC101)
CLK
DATA
ROM (IC102)

VAC	AC voltage including V4.3 signal (altered by CO_2 partial pressure) and V3.7 signal (not affected by CO_2 gas, used for reference).
DATA	Compensation coefficient to calculate CO_2 value, 256 bit serial data stored in chip inside each CO_2 sensor (linearization data).
EXC	−5 V ±2% power voltage to drive (excite) the infrared ray detector.
VH	+12 V ± power voltage to drive (heat) the infrared ray lamp.
VM	+2.4 V ±2% power voltage to drive the motor for chopper disc.
RST	ROM reset pulse, 1024 msec interval.
CLK	250 Hz clock signal.

- **CO2 Sensor Input/Output Signal Timing**


3.7μm
4.3μm
3.7μm
4.3μm
0.2V ~ 0.8V
VAC
20msec
VDC
+1V ~ +5V
0V
1024msec
RST
CLK
DATA
D0
D1
D2
D3
....
D255
D0

NOTE
VAC and DATA are asynchronous.

3-4-9 O_2 Head Amp (AG-820PA), UP-0592

◆ General

The AG-820PA is one of the head amplifiers of BSM-8000 series bedside monitors to measure fraction of inspired oxygen (FiO_2) using an O_2 sensor connected with a ventilator, etc.

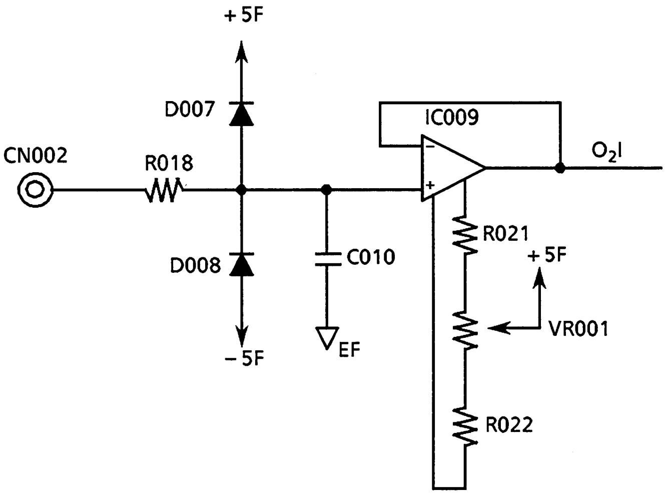
Diodes for over-voltage protection and high-cut filter for noise reduction are employed in the input circuit block.

• Composition

After filtering, signal is buffed with IC009 and IC010 and then multiplexed with IC007 multiplexer device. Multiplexer output signals are Ref0, O_2I, and O_2II. Multiplexing is controlled by clock signal generated by IC006 counter.

• Input buffer

There are two similar circuits of input buffer for O_2I and O_2II. Description below is for O_2I.

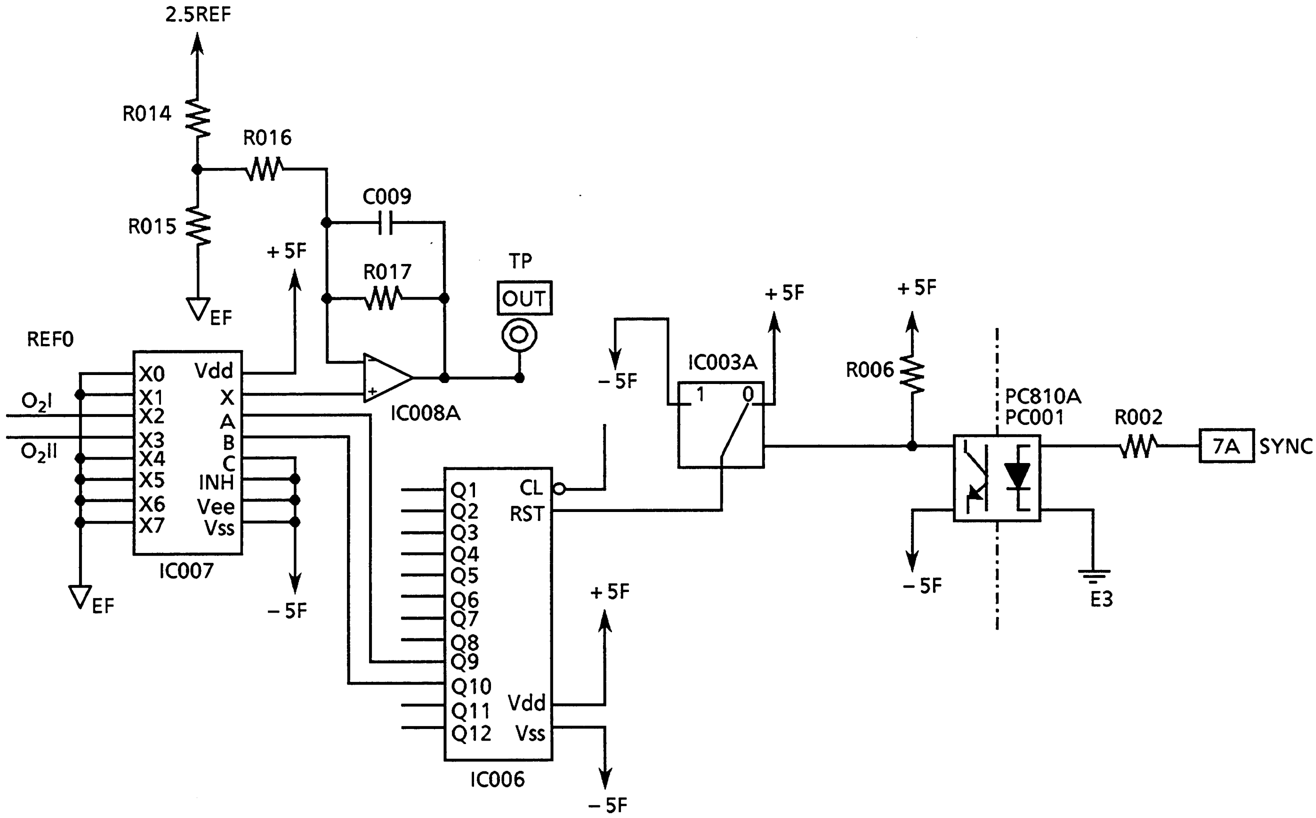


Voltage generated by the O_2 sensor in proportion to O_2 density is inputted to the IC009 through the D007 and D008 protective diodes and low-pass filter composed of R018 and C010. This low impedance signal is outputted to the multiplexer.

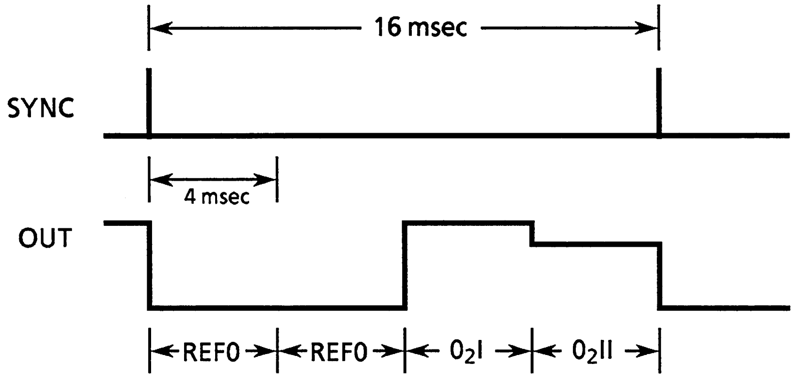
The VR001 is for offset adjustment of IC009 buffer amplifier. When the IC009 is replaced, VR001 adjustment is required.

• Output signal timing

Time-shared output signal is amplified and transmitted by a circuit shown below.


2.5REF
R014
R016
R015
C009
R017
+5F
TP
OUT
EF
REF0
O2I
O2II
X0
X1
X2
X3
X4
X5
X6
X7
Vdd
X
A
B
C
INH
Vee
Vss
IC007
EF
-5F
IC008A
-5F
IC003A
1
0
+5F
+5F
R006
PC810A
PC001
R002
7A
SYNC
-5F
E3
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
CL
RST
Vdd
Vss
IC006
+5F
-5F

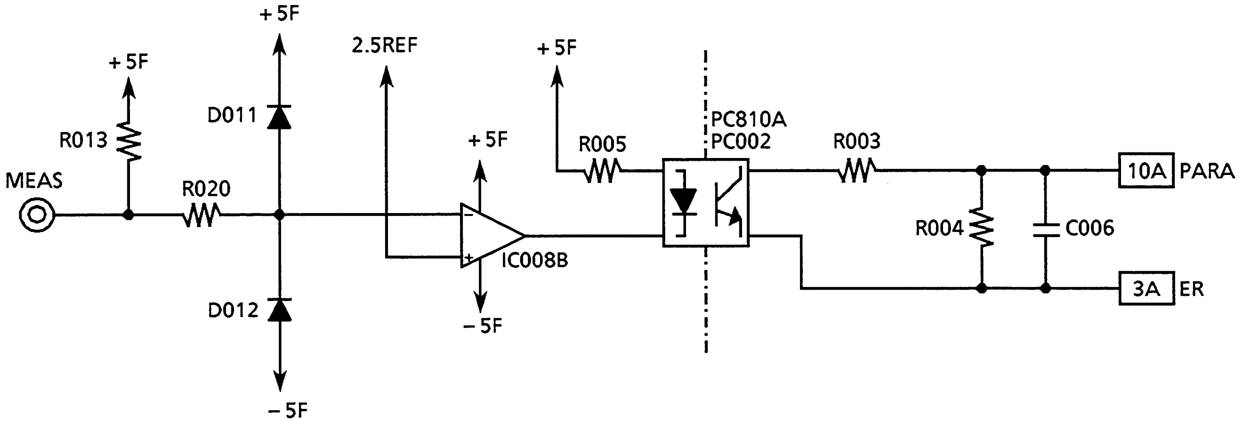
Multiplexer IC007 outputs Ref0, O_2I and O_2II signals in the timing below by the control signal from IC006 counter.


16 msec
SYNC
4 msec
OUT
REF0
REF0
O2I
O2II

Multiplexed output signal is 35 times amplified with IC008A and level shifted (output is -4.8 ± 0.25 V when input is shortened) and then transferred to a modulation circuit.

Refer to the pages for BP head amplifier output signal modulation and demodulation of descriptions for timing from floating area to the non-floating area.

● Unit discrimination signal (PARA voltage)


+5F
R013
MEAS
R020
+5F
D011
D012
-5F
2.5REF
+5F
IC008B
-5F
+5F
R005
PC810A
PC002
R003
R004
C006
10A
PARA
3A
ER

PARA (parameter) voltage changes when the O_2 sensor is connected and disconnected as below.

Sensor	PARA voltage (V)
Connection	0.45 ±0.02
Disconnection	0.40 ±0.02

When the sensor is not connected, IC008A comparator output is LOW level. With this voltage, the photocoupler PC002 is conductive and 0.4 ± 0.02 V voltage attenuated with R003 and R004 resisters appears as PARA voltage at no sensor connection.

When the sensor is connected, comparator output is HI. With this voltage, PC002 becomes off and 0.45 ±0.02 V appears as PARA voltage at sensor connection.

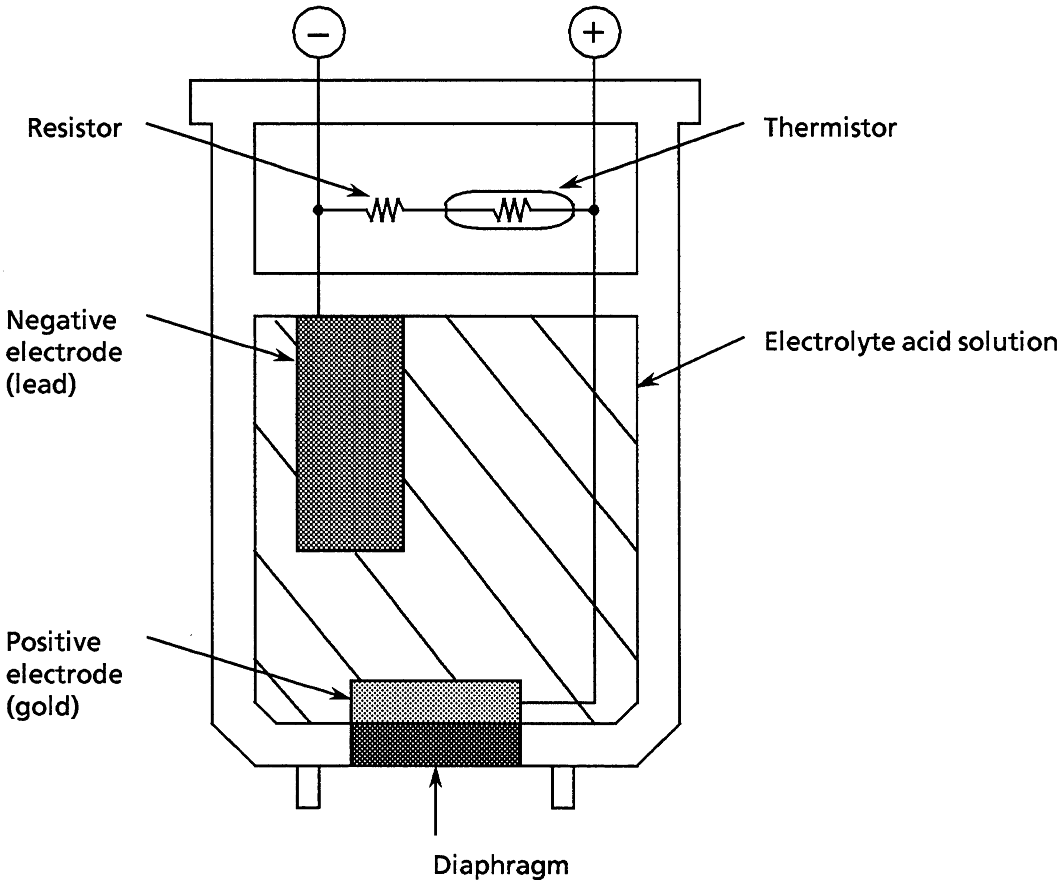
◆ OS-1000 O_2 Sensor (AIKA, Japan)

• Measuring principle of O_2 and construction of the O_2 sensor

As figured, O_2 sensor is an oxygen-lead battery composed of gold as positive electrode, lead as negative electrode and special electrolyte acid solution.

Oxygen in O_2 measurement atmosphere diffuses to gold electrode through a non porous fluororesin diaphragm and deoxidized by electrolysis and current which is proportional to oxygen density flows in the electrodes.

Voltage across a resistor and a thermistor for temperature compensation serially connected is obtained to measure oxygen density.


−
+
Resistor
Thermistor
Negative electrode (lead)
Electrolyte acid solution
Positive electrode (gold)
Diaphragm

• Life time of the O_2 sensor

The O_2 sensor has a life time as it is an oxygen battery which generates voltage in response to oxygen in atmosphere. Life time depends upon oxygen density of measuring gas. The higher oxygen density, the shorter life time of the O_2 sensor.

It is not sure to define life time of the O_2 sensor as measurement will be done with various oxygen density.

End of life of the O_2 sensor means that the sensor does not generate voltage which is high enough for O_2 measurement.

Figure on the next page shows relation between oxygen density and output voltage of O_2 sensor model OS-1000, a product of AIKA, Japan. When O_2 sensor is exposed in oxygen for a long time of period, slope of the output voltage curve becomes small.

Nihon Kohden O_2 measurement is designed to define the end of life of the O_2 sensor when output voltage corresponding to that of 100% oxygen shows less than 35mV.

When an exhausted sensor is used, measurement error goes out of specified normal range. When such condition is detected at calibration, message "INOP" (inoperative) is displayed on the screen and "CAL??" remains on the screen without measurement.

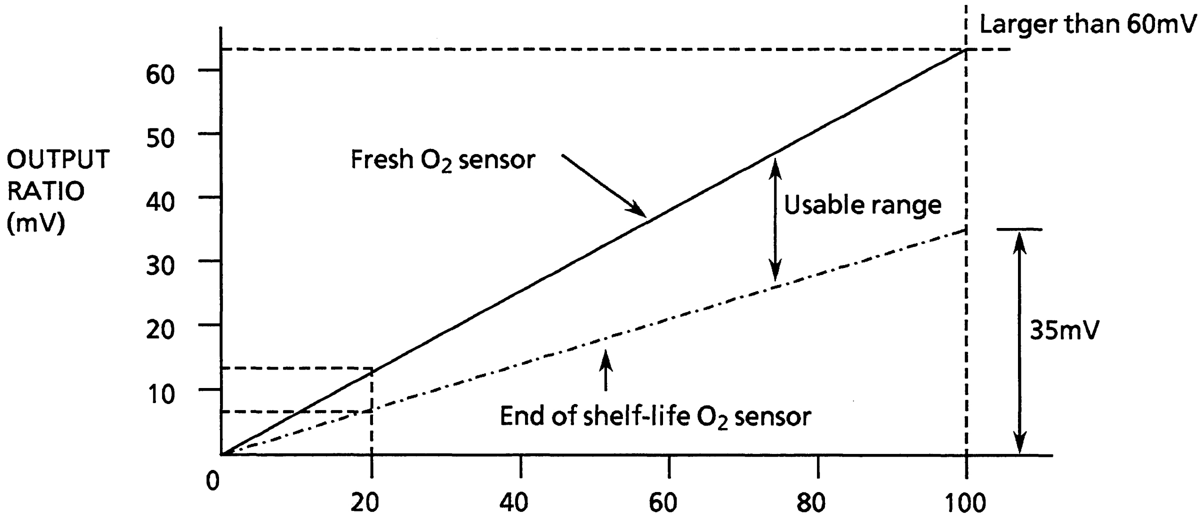
It is estimated that life time of the O_2 sensor is three to five years.

- **Precautions when handling the O_2 sensor**

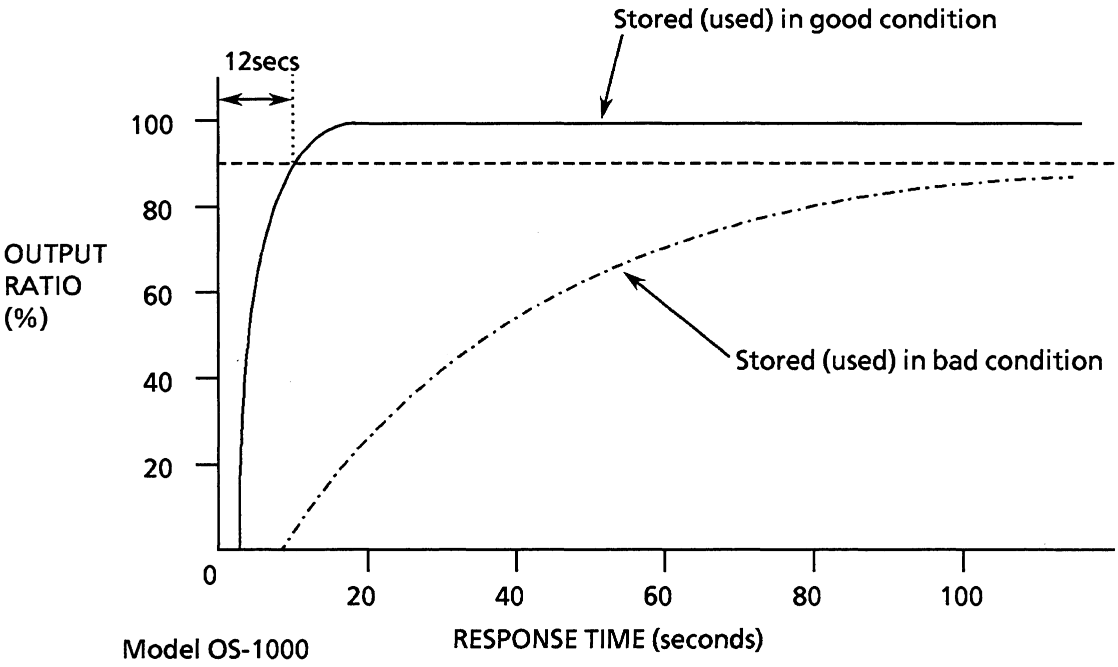
In order to avoid influence by pressure change inside the sensor due to change of atmospheric pressure, gas is filled in the sensor chamber. Therefore, when sensing part is located upwards, gas bubble will be placed on the diaphragm or electrode which will prevent electrolysis inside the chamber and correct data cannot be obtained.

Be sure to put the sensor so that the sensing part is facing downwards for correct measurement. When storing the O_2 sensor, it is recommended to put the sensing part downwards.

If the sensing part is kept upwards it takes several minutes for the sensor to become stabilized before calibration. Be sure to calibrate the sensor after several minutes.



Model OS-1000


Stored (used) in good condition
12secs
100
80
OUTPUT
RATIO
(%)
60
40
20
0
Stored (used) in bad condition
20
40
60
80
100
Model OS-1000
RESPONSE TIME (seconds)

3-4-10 NIBP Head Amp (AP-860PA), UP-0629 & UP-0630

◆ General

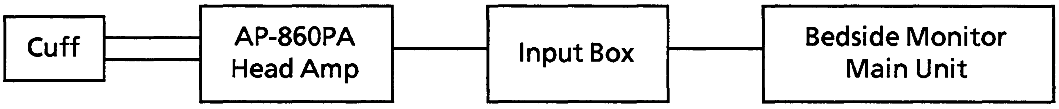
AP-860PA is one of the two types of head amplifiers for the bedside monitor used to measure Noninvasive Blood Pressure (NIBP) of a patient. This head amplifier uses the double air hose method.

NOTE

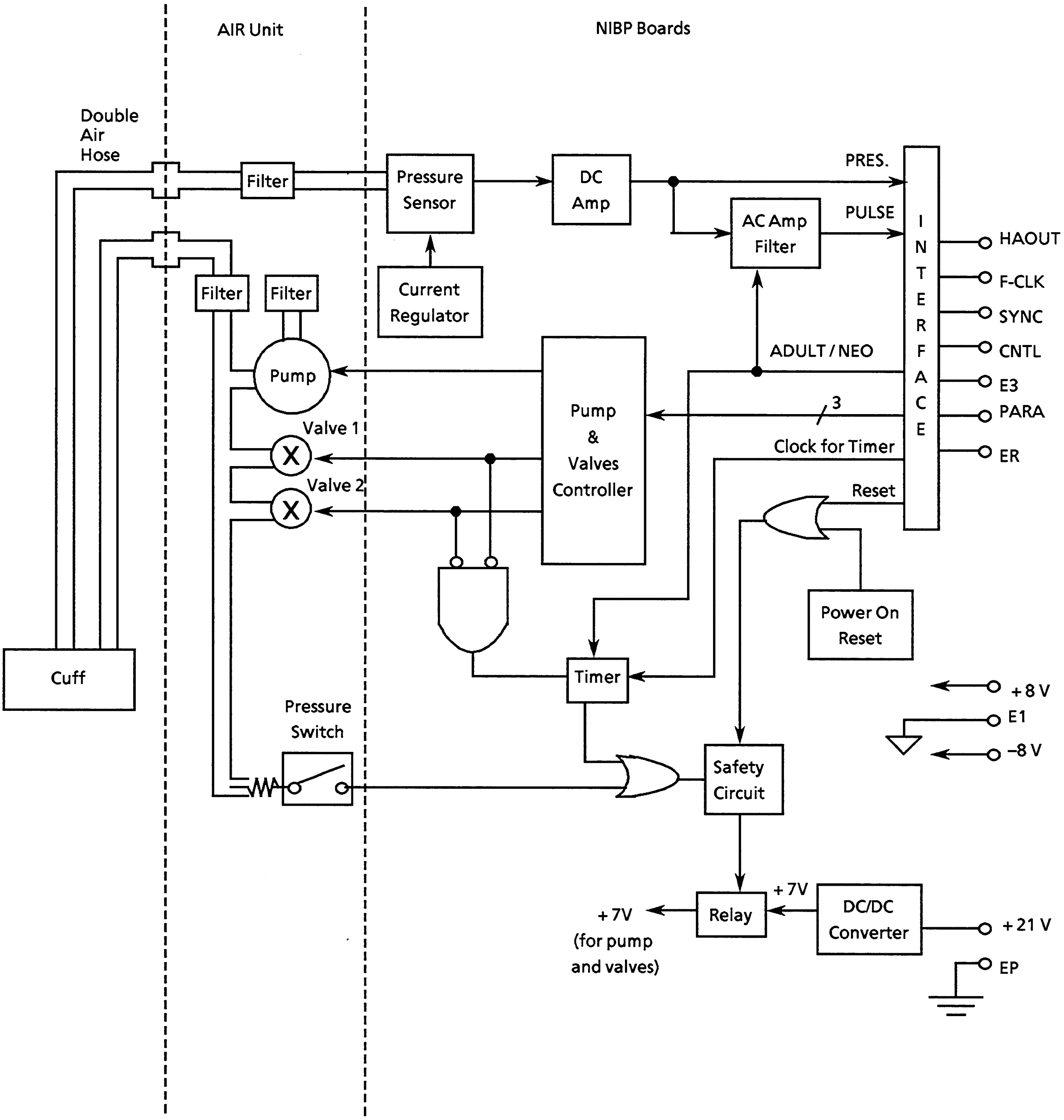
The other type of NIBP head amplifier is the AP-851PA head amplifier. The AP-851PA head amplifier uses the single air hose method.

◆ System Connection

NIBP head amplifier is inserted into the input box of the bedside monitor and the dual air hose is connected to the two NIBP sockets.



◆ Block Description


AIR Unit
NIBP Boards
Double Air Hose
Filter
Pressure Sensor
DC Amp
PRES.
AC Amp Filter
PULSE
INTERFACE
HAOUT
F-CLK
SYNC
CNTL
E3
PARA
ER
Filter
Filter
Current Regulator
Pump
ADULT / NEO
3
Pump & Valves Controller
Valve 1
Valve 2
Clock for Timer
Reset
Power On Reset
Cuff
Timer
+8 V
E1
-8 V
Pressure Switch
Safety Circuit
+7V
Relay
DC/DC Converter
+7V (for pump and valves)
+21 V
EP

• AIR Unit, SG-001P

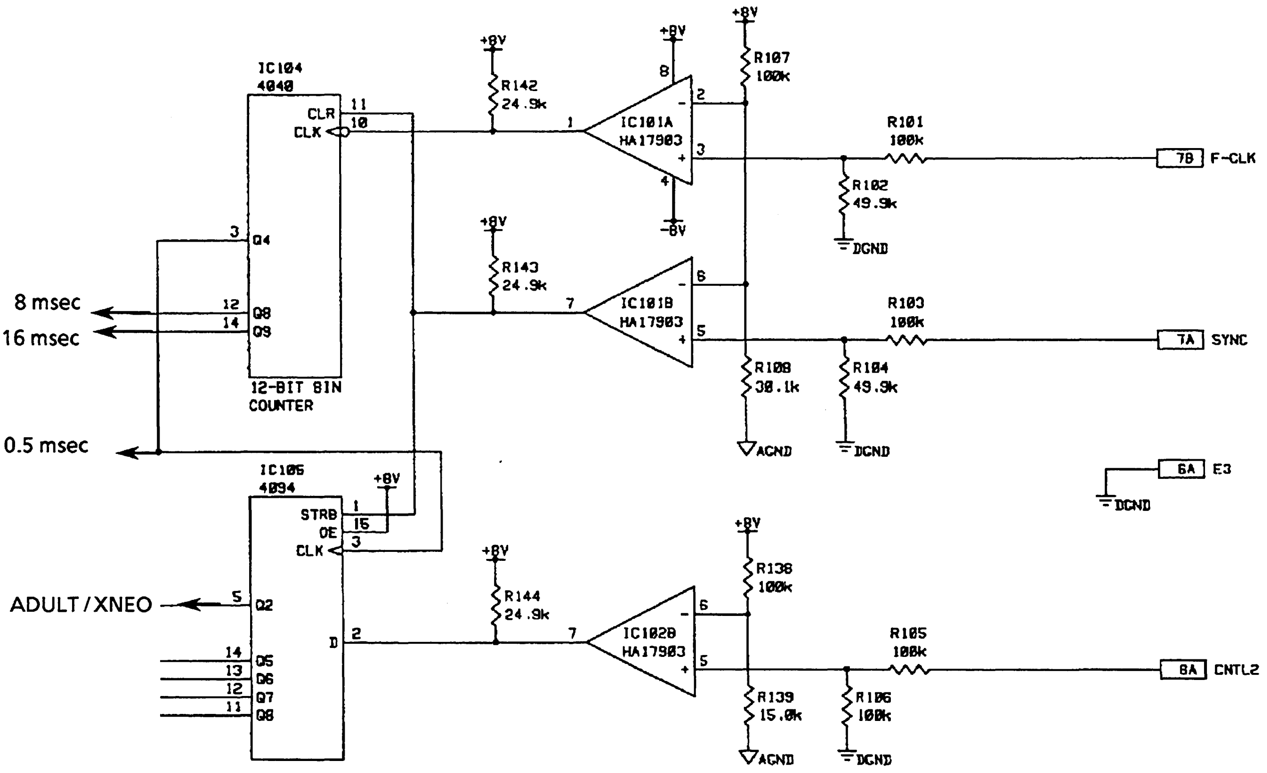
This unit consists of the pump, solenoid valves, and over pressure control switch.

• NIBP boards

There are two boards in the NIBP head amplifier unit, NIBP Main board, UP-0629, and NIBP Sub board, UP-0630. The main unit of the bedside monitor controls the NIBP Main board. The main function of the NIBP Main board is to control the pump and solenoid valves through the time limiter circuit, pressure circuit, and safety circuit. The main function of the NIBP Sub board is to regulate the current supply to the pressure sensor, process the pressure and pulse signals, and finally multiplex all the signals from both the boards before sending it to the bedside monitor.

The DC/DC converter supplies the power to the NIBP Main and Sub boards and the AIR unit.

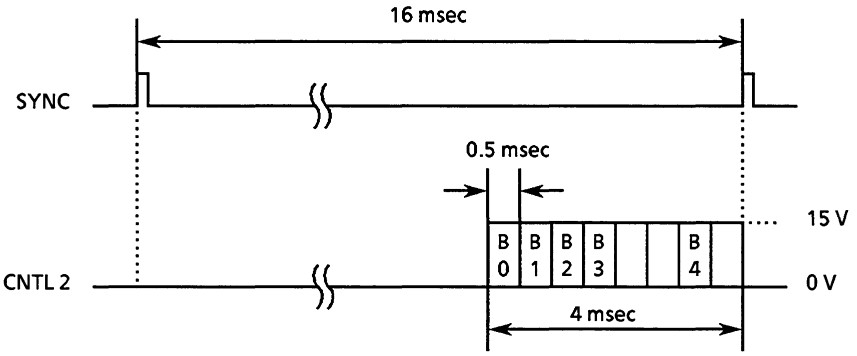
◆ Control Circuit (NIBP Main Board, UP-0629)


IC104
4040
CLR 11
CLK 10
3 Q4
12 Q8
14 Q9
12-BIT BIN COUNTER
8 msec
16 msec
0.5 msec
IC106
4094
+8V
STRB 1
OE 15
CLK 3
ADULT / XNEO
5 Q2
D 2
14 Q5
13 Q6
12 Q7
11 Q8
+8V
R142 24.9k
R143 24.9k
R144 24.9k
IC101A HA17903
IC101B HA17903
IC102B HA17903
-8V
R107 100k
R101 100k
R102 49.9k
DGND
R103 100k
R108 30.1k
R104 49.9k
AGND
R138 100k
R105 100k
R139 15.0k
R106 100k
7B F-CLK
7A SYNC
6A E3
8A CNTL2

The signal level of the input signals, F-CLK, SYNC, and CNTL2, from the input box is within the range of 0 ~ 15 V. The comparators IC101 and 102 change the signal level of these input signals to ±8 V.

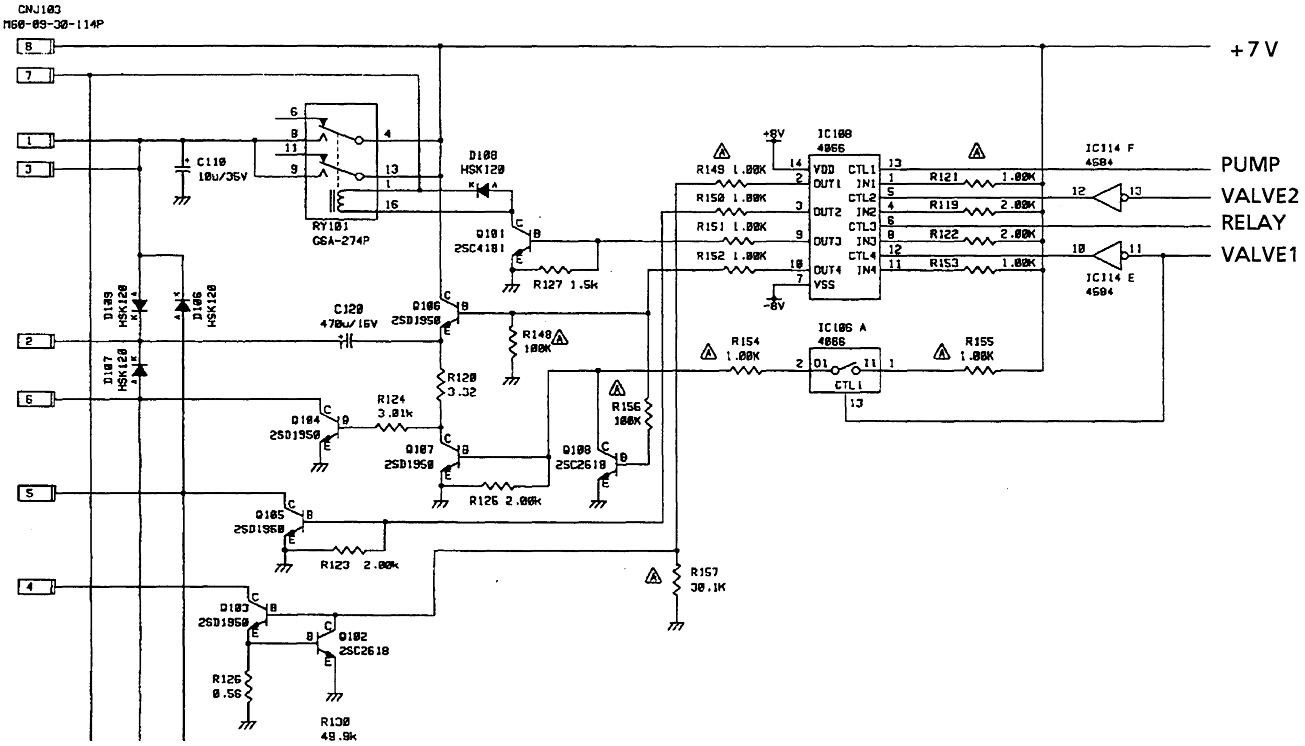
The 64 kHz F-CLK signal is then counted by counter IC104 to give 0.5 msec, 8 msec, and 16 msec timing signals. The analog switch IC106 shunt the 8 msec or 16 msec timing signal to the timer IC109 of the safety circuit. The status signal, ADULT/XNEONATUS, controls the analog switch IC106. In the adult mode, the analog switch shunt the 16 msec timing signal to the safety circuit, and in the neonatal mode, the switch shunt the 8 msec timing signal. The 8 msec and 16 msec timing signals are also output to the multiplexer IC208 of the NIBP Sub board.

The 0.5 msec timing signal in the serial to parallel converter IC105 chops the serial CNTL2 signal into parallel output. The SYNC signal provides the synchronizing signal for the serial to parallel converter. The serial to parallel conversion of the CNTL2 signal is shown below.



Bit	Description	1 (High)	0 (Low)
B0	Pump	On	Off
B1	Valve 1	Close	Open
B2	Valve 2	Close	Open
B3	Inst	On	Off
B4	Adult/Neonatal	Adult	Neonatal

◆ Relay, Pump, and Solenoid Valves Controller Circuit (NIBP Main Board, UP-0629)


CNJ103
M60-09-30-114P
+7V
PUMP
VALVE2
RELAY
VALVE1
RY101
G6A-274P
C110
10u/35V
D108
HSK120
Q101
2SC4181
R127 1.5k
D109
HSK120
D106
HSK120
D107
HSK120
C120
470u/16V
Q106
2SD1950
R148
100K
R120
3.32
R124
3.01k
Q104
2SD1950
Q107
2SD1950
Q108
2SC2618
R156
100K
R126 2.00k
Q105
2SD1950
R123 2.00k
R157
30.1K
Q103
2SD1950
Q102
2SC2618
R126
0.56
R130
49.9k
IC108
4066
R149 1.00K
R150 1.00K
R151 1.00K
R152 1.00K
+8V
-8V
VDD
VSS
OUT1
OUT2
OUT3
OUT4
IN1
IN2
IN3
IN4
CTL1
CTL2
CTL3
CTL4
R121 1.00K
R119 2.00K
R122 2.00K
R153 1.00K
IC114 F
4584
IC114 E
4584
IC105 A
4066
R154
1.00K
R155
1.00K
CTL1

The safety circuit controls the relay RY101. The relay RY101 switches on or off the +7 V power supply from the DC/DC converter to the pump and solenoid valves in the AIR unit through connector CNJ103.

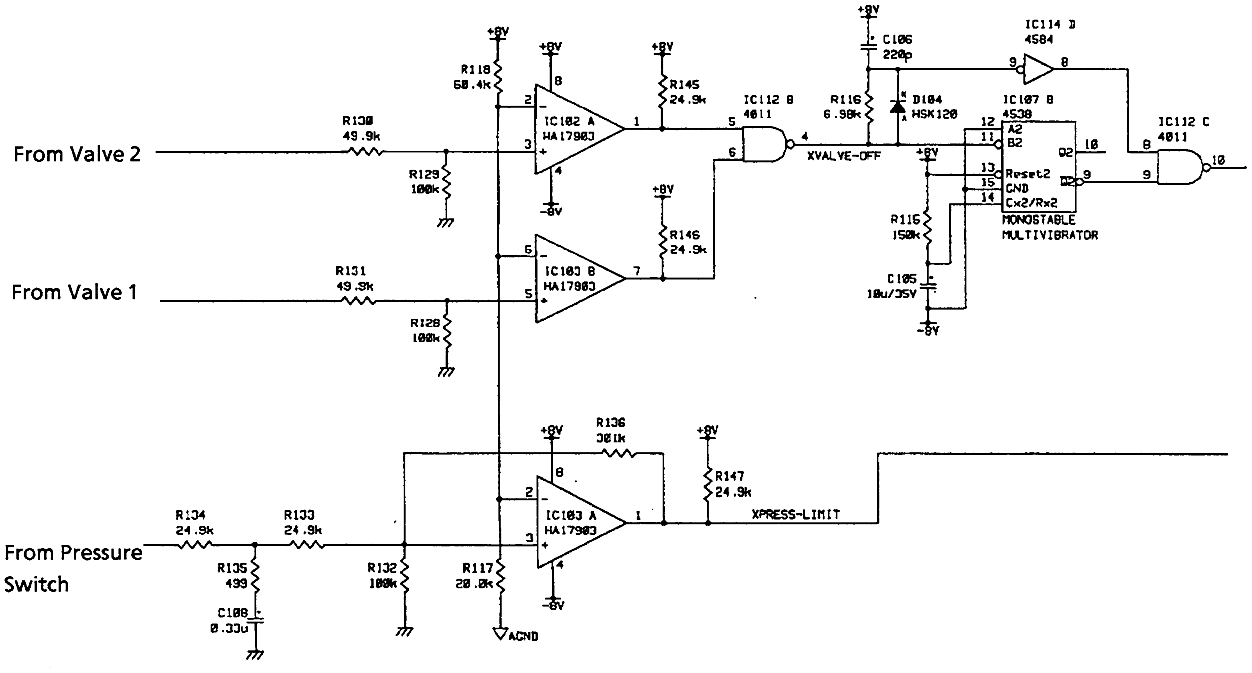
The parallel output signals from the IC105 control the pump, solenoid valves by switching on and off the transistor Q101 ~ 108.

◆ Safety Circuit (NIBP Main board, UP-0629)

The Main unit controls this circuit, but, this circuit can also operate independently under the following conditions:
1) When the cuff pressure exceeds 300 mmHg.
2) When the measuring time exceeds 120 seconds for adult and 60 seconds for neonatal.

The safety circuit has two major blocks, namely the comparator block and the timer, latch, and reset block.

a) Comparator Block

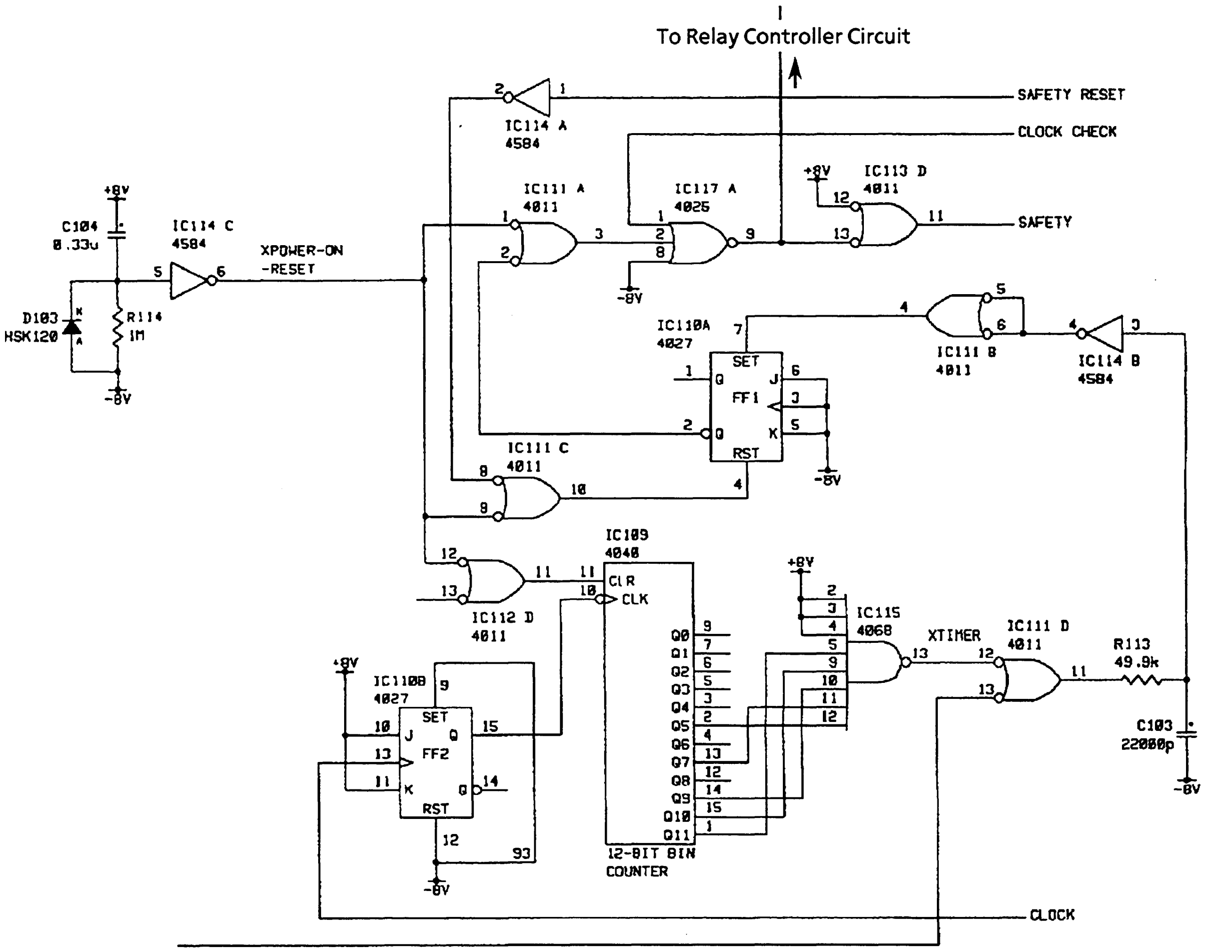

From Valve 2
From Valve 1
From Pressure Switch
R118 60.4k
R130 49.9k
R129 100k
R131 49.9k
R128 100k
IC102 A HA17903
IC103 B HA17903
IC103 A HA17903
R145 24.9k
R146 24.9k
IC112 B 4011
XVALVE-OFF
C106 220p
R116 6.98k
D104 HSK120
IC114 D 4584
IC107 B 4538
A2
B2
Q2
Reset2
GND
Cx2/Rx2
MONOSTABLE MULTIVIBRATOR
R115 150k
C105 10u/35V
IC112 C 4011
R136 301k
R147 24.9k
XPRESS-LIMIT
R134 24.9k
R133 24.9k
R135 499
C108 0.33u
R132 100k
R117 20.0k
AGND
+8V
-8V

The comparators IC102 and 103 change the signal level of the input signals from the solenoid valves and pressure switch. When both of the solenoid valves are opened, the output of IC112 is set to low (−8 V). This low signal is used to reset the counter of timer circuit.

This NIBP head amplifier uses the step deflation method and this caused the solenoid valves to open and close repeatedly. This opening and closing of the solenoid valves can clear the timer circuit. To prevent this from happening, the monostable multivibrator IC107 treats the approximately 1.5 seconds of the period when the valve is opened as the period as if the valve is closed.

The pressure switch set the output of IC103 to low (−8 V) when the cuff pressure exceeds 300 mmHg.

b) Timer, Latch, and Reset Block

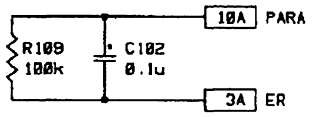

To Relay Controller Circuit
SAFETY RESET
CLOCK CHECK
SAFETY
CLOCK
IC114 A
4584
IC111 A
4011
IC117 A
4025
IC113 D
4011
+8V
-8V
C104
0.33u
IC114 C
4584
XPOWER-ON
-RESET
D103
HSK120
R114
1M
IC110A
4027
SET
FF1
RST
IC111 B
4011
IC114 B
4584
IC111 C
4011
IC109
4040
CLR
CLK
IC112 D
4011
IC110B
4027
FF2
12-BIT BIN
COUNTER
IC115
4068
XTIMER
IC111 D
4011
R113
49.9k
C103
22000p

When the solenoid valves are closed during the NIBP measurement, the comparators output a high signal to the timer circuit (IC109 and IC115). A low input signal causes the timer circuit to start counting. Depending on the type of clock signal (adult mode, 16 msec; neonatal mode, 8 msec), the timer output a high signal at the pin-11 of IC111 if the solenoid valves are closed for more than 120 seconds in the adult mode or 60 seconds in the neonatal mode. A high output signal from the timer circuit causes the latch IC110 to output a low signal that finally causes the output of pin-9 of IC117 to go low. A low signal at pin-9 of IC117 switches off the relay RY101, which in turn stops the +7 V power supply to the pump and solenoid valves in the AIR unit.

The reset signal from the main unit and the power on reset signal from the power on reset detector circuit can also set the pin-9 of IC117 low through latch IC110.

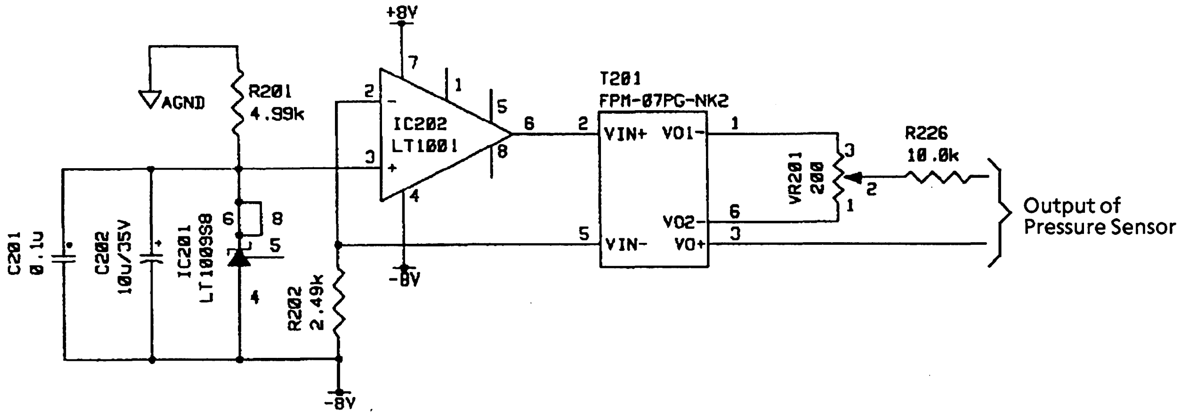
The status of this safety circuit is output to pin No. 6 of connector CN104 to the NIBP Sub board through analog switch IC106. A low output from the pin No. 6 of connector CN104 shows that the safety circuit is in operation.

◆ PARA Signal (NIBP Main board, UP-0629)


10A
PARA
R109
100k
C102
0.1u
3A
ER

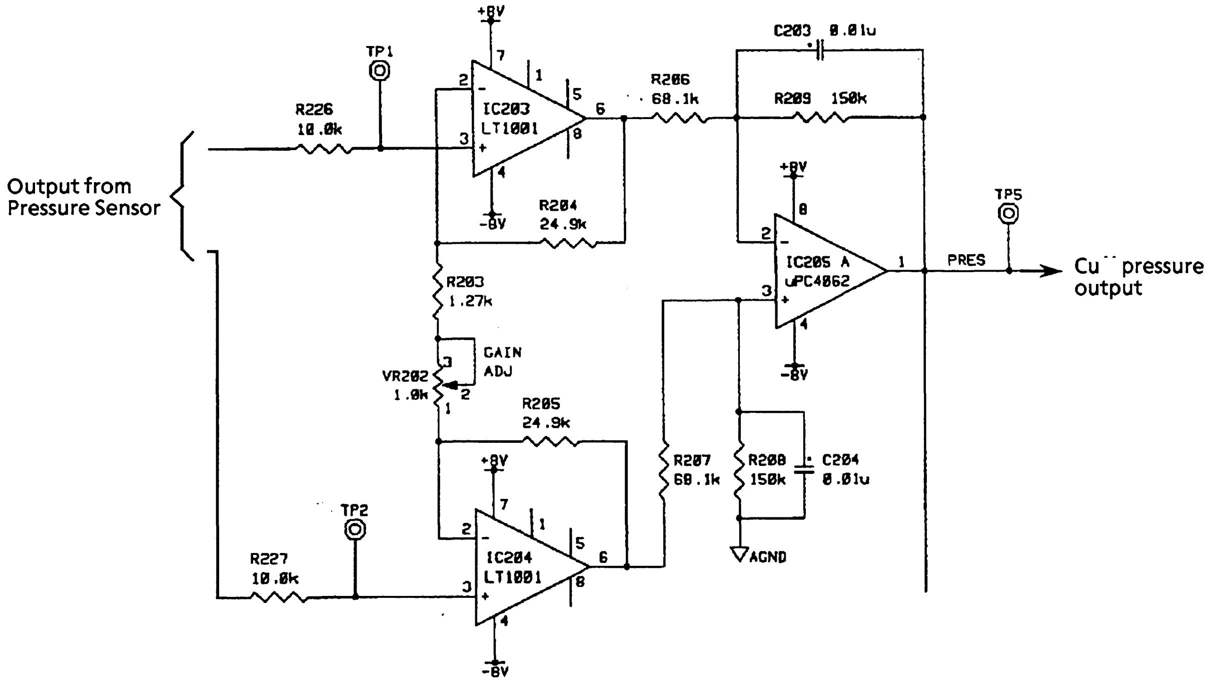
The PARA signal for the NIBP head amplifier has a fixed voltage of 4.55 V. This PARA signal is the NIBP head amplifier AP-860PA's identification signal for the main unit of the bedside monitor.

◆ Cuff Pressure Sensor Circuit (NIBP Sub Board, UP-0630)


+8V
AGND
R201
4.99k
IC202
LT1001
T201
FPM-07PG-NK2
VIN+
VO1
VO2
VIN-
VO+
VR201
200
R226
10.0k
Output of Pressure Sensor
C201
0.1u
C202
10u/35V
IC201
LT1009S8
R202
2.49k
-8V
-8V

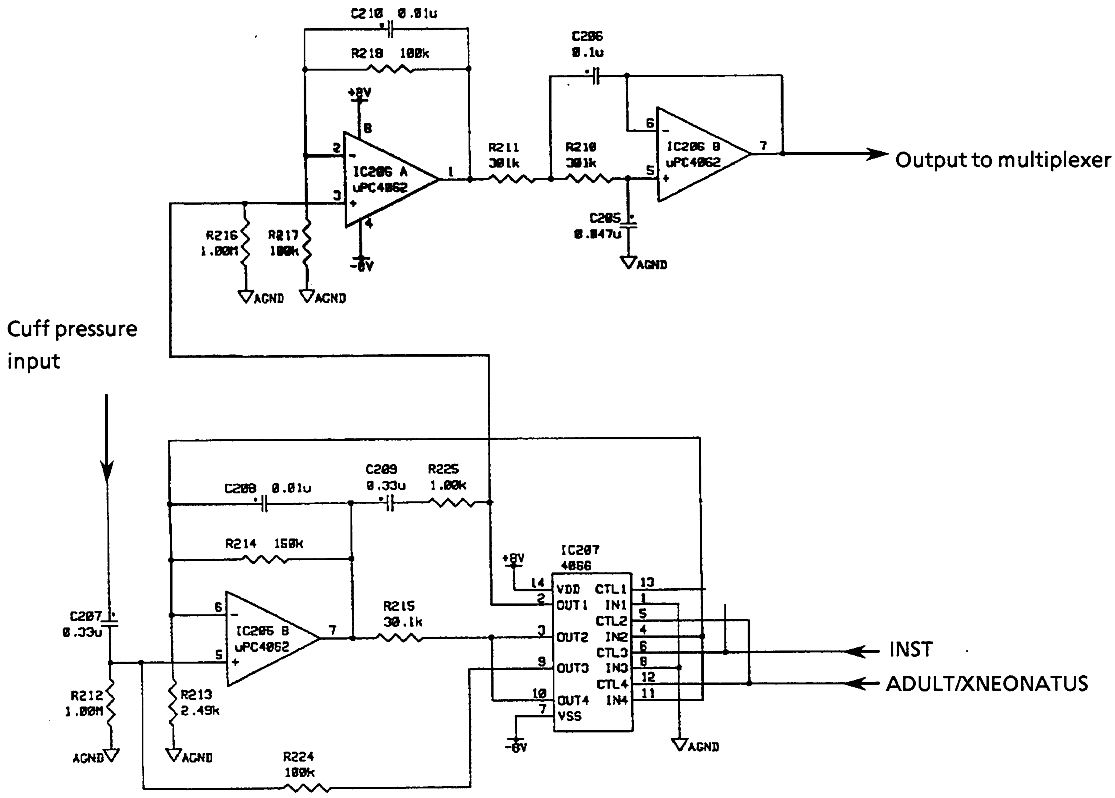
This circuit is based around the cuff pressure sensor T201. A 2.5 V Zener diode IC201, OP amplifier IC202, and resistor R202 supply a constant regulated current to the cuff pressure sensor T201. The cuff pressure sensor T201 varies the output voltage according to the pressure in the cuff. The variable resistor VR201 is used to zero adjust the cuff pressure sensor T201.

◆ Cuff Pressure Voltage Amplification Circuit (NIBP Sub Board, UP-0630)


+8V
C203 0.01u
TP1
R206 68.1k
R209 150k
R226 10.0k
IC203 LT1001
Output from Pressure Sensor
+8V
TP5
R204 24.9k
-8V
IC205 A uPC4062
PRES
Cuff pressure output
R203 1.27k
GAIN ADJ
VR202 1.0k
-8V
R205 24.9k
+8V
R207 68.1k
R208 150k
C204 0.01u
TP2
AGND
R227 10.0k
IC204 LT1001
-8V

This circuit, consisting of IC203 ~ 205, amplifies the cuff sensor output voltage about 60 times and outputs the amplified signal to the oscillating cuff sensor output voltage amplification and filtering circuit. It adjusts the sensitivity of the cuff sensor output voltage to 100 mmHg/1 V through sensitivity volume of the variable resistor VR202.

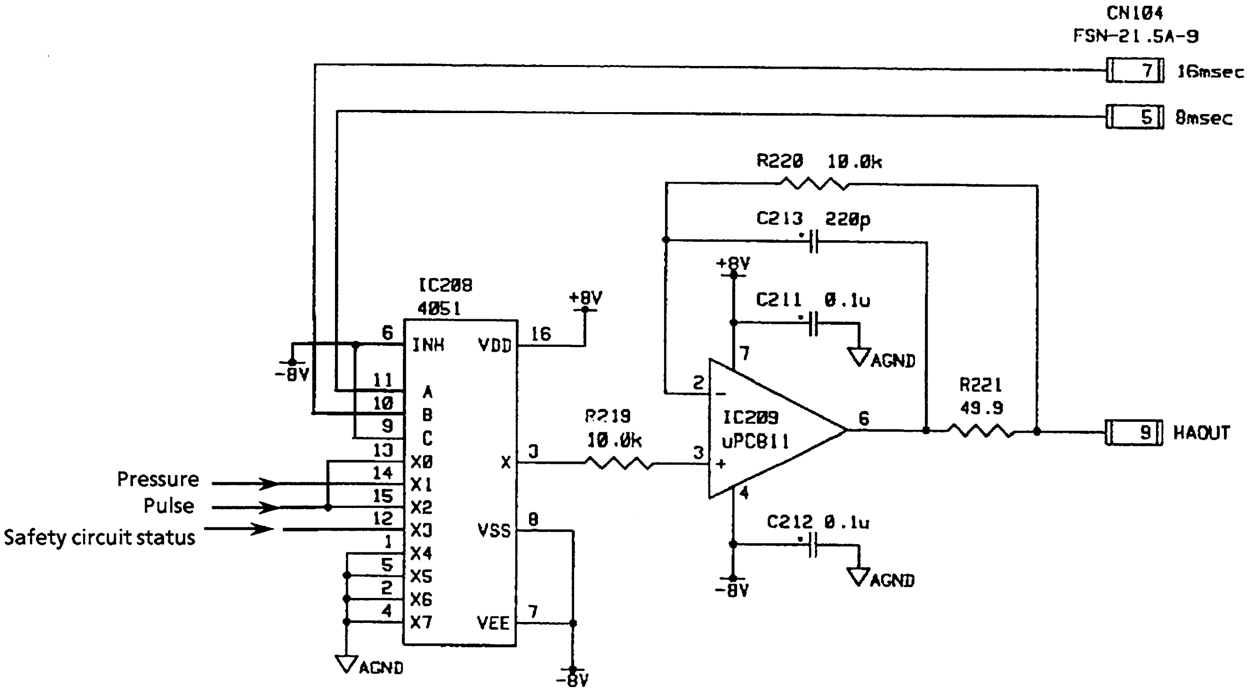
◆ Oscillating Cuff Sensor Output Voltage Amplification and Filtering Circuit (NIBP Sub Board, UP-0630)


C210 0.01u
R219 100k
C206 0.1u
+8V
IC206 A
uPC4062
-8V
R211 301k
R210 301k
IC206 B
uPC4062
Output to multiplexer
C205 0.047u
AGND
R216 1.00M
R217 100k
AGND
AGND
Cuff pressure input
C209 0.33u
R225 1.00k
C208 0.01u
R214 150k
+8V
IC207 4066
VDD
CTL1
OUT1
IN1
CTL2
OUT2
IN2
CTL3
OUT3
IN3
CTL4
OUT4
IN4
VSS
R215 30.1k
IC205 B
uPC4062
C207 0.33u
R212 1.00M
R213 2.49k
AGND
AGND
R224 100k
-8V
AGND
INST
ADULT/XNEONATUS

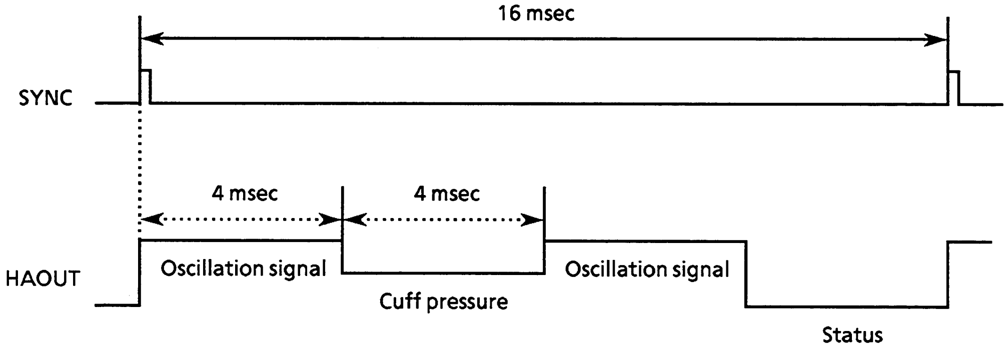
NIBP measurement using the occlusive-oscillometric method gives an oscillating pressure reading during the measurement. This circuit amplify and filter this oscillating cuff sensor output voltage signal and output the final signal to the multiplexer IC208.

This circuit consists of two level low cut filter with 0.3 second time constant block (C207, R212, C209, and R216) and a 7.5 Hz high cut filter block (R210, R211, C205, C206, and IC206). In the adult mode, IC205 and 206 amplify the signal about 22 times, and in the neonatal mode, IC205 and 206 amplify the signal about 122 times.

◆ Multiplexer Circuit (NIBP Sub Board, UP-0630)


CN104
FSN-21.5A-9
7
16msec
5
8msec
R220 10.0k
C213 220p
+8V
C211 0.1u
AGND
IC208
4051
INH
VDD
16
-8V
A
B
C
X0
X1
X2
X3
X4
X5
X6
X7
X
VSS
VEE
Pressure
Pulse
Safety circuit status
R219
10.0k
IC209
uPC811
R221
49.9
9
HAOUT
C212 0.1u
-8V
AGND

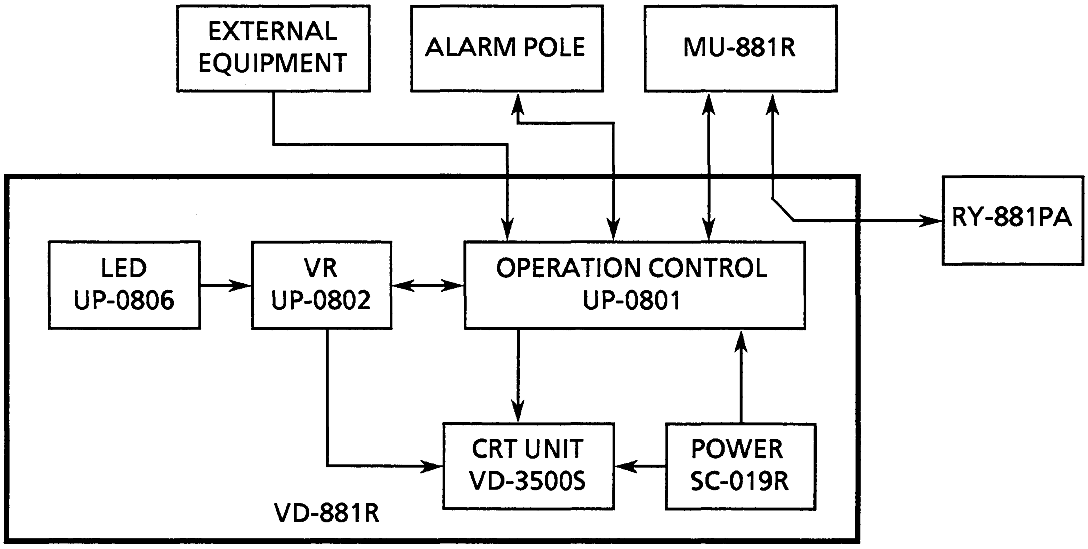
This multiplexer circuit IC208 uses the timing signals (8 msec and 16 msec) from the NIBP Main board to time-share the cuff pressure output voltage signal, oscillation signal, safety circuit status signal into the HAOUT signal. The timing of the final output signal is shown below.


16 msec
SYNC
4 msec
4 msec
HAOUT
Oscillation signal
Cuff pressure
Oscillation signal
Status

3-5 Display Unit, VD-881R

3-5-1 General

◆ **Block Diagram**


EXTERNAL EQUIPMENT
ALARM POLE
MU-881R
RY-881PA
LED UP-0806
VR UP-0802
OPERATION CONTROL UP-0801
CRT UNIT VD-3500S
POWER SC-019R
VD-881R

The Display unit consists of the following sub-unit:

• OPERATION CONTROL Board, UP-0801
The two 1 chip CPUs (IC201, 204) on this board control the display unit. They communicate with the bedside monitor main unit via the RS-232C interface. This board also controls the sound, video, power supply, and alarm pole. The signal from the remote control is processed on this board too.

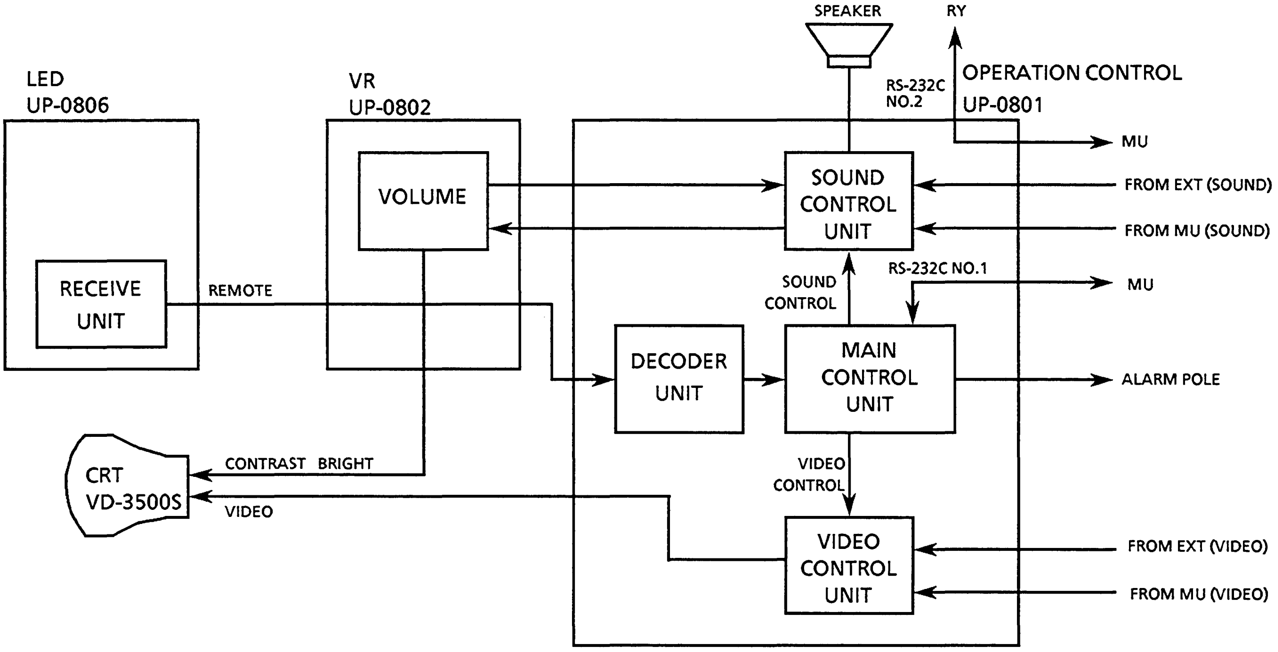
• OPERATION (VR) Board, UP-0802
This controls the sound volume, brightness, and contrast.

• LED Board, UP-0806
This board receives the remote control signal and relay it to the OPERATION CONTROL board via the OPERATION (VR) board.

• CRT Unit, VD-3500S
This is a 14 inches three mode scanning color monitor.

• Power Supply Unit, SC-019R
This supplies the power for the video display unit.

◆ Signal Flow


SPEAKER
RY
LED
UP-0806
VR
UP-0802
RS-232C NO.2
OPERATION CONTROL
UP-0801
MU
VOLUME
SOUND CONTROL UNIT
FROM EXT (SOUND)
FROM MU (SOUND)
RECEIVE UNIT
REMOTE
SOUND CONTROL
RS-232C NO.1
MU
DECODER UNIT
MAIN CONTROL UNIT
ALARM POLE
CRT
VD-3500S
CONTRAST BRIGHT
VIDEO
VIDEO CONTROL
VIDEO CONTROL UNIT
FROM EXT (VIDEO)
FROM MU (VIDEO)

• Remote Control Signal

The light sensor on the LED board receives the light signal from the remote control. The sensor sends the signal to the OPERATION CONTROL board via the OPERATION (VR) board. The OPERATION CONTROL board decodes the signal and then sends it to the bedside monitor main unit via the RS-232S.

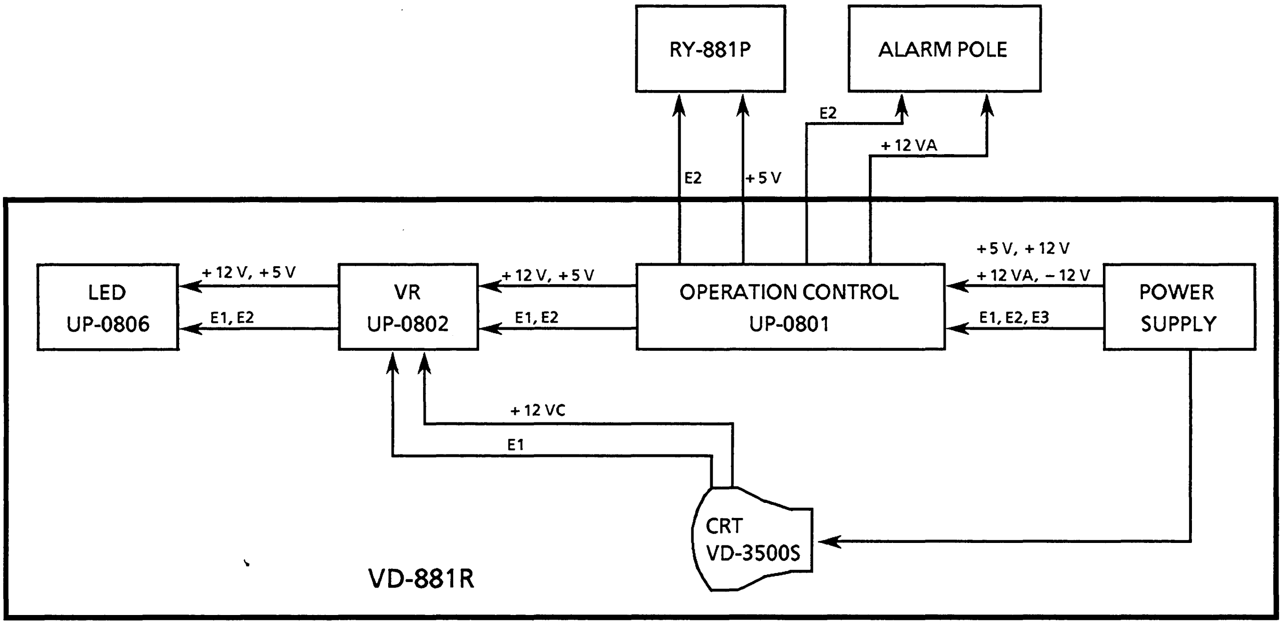
• SOUND Signal

The OPERATION CONTROL board receives and selects the sound signal from the bedside monitor main unit or the external unit. The OPERATION CONTROL board then sends the SOUND signal to the VR board for processing before returning it to the OPERATION CONTROL board. The processed SOUND signal is inputted into the speaker unit via the power amplifier.

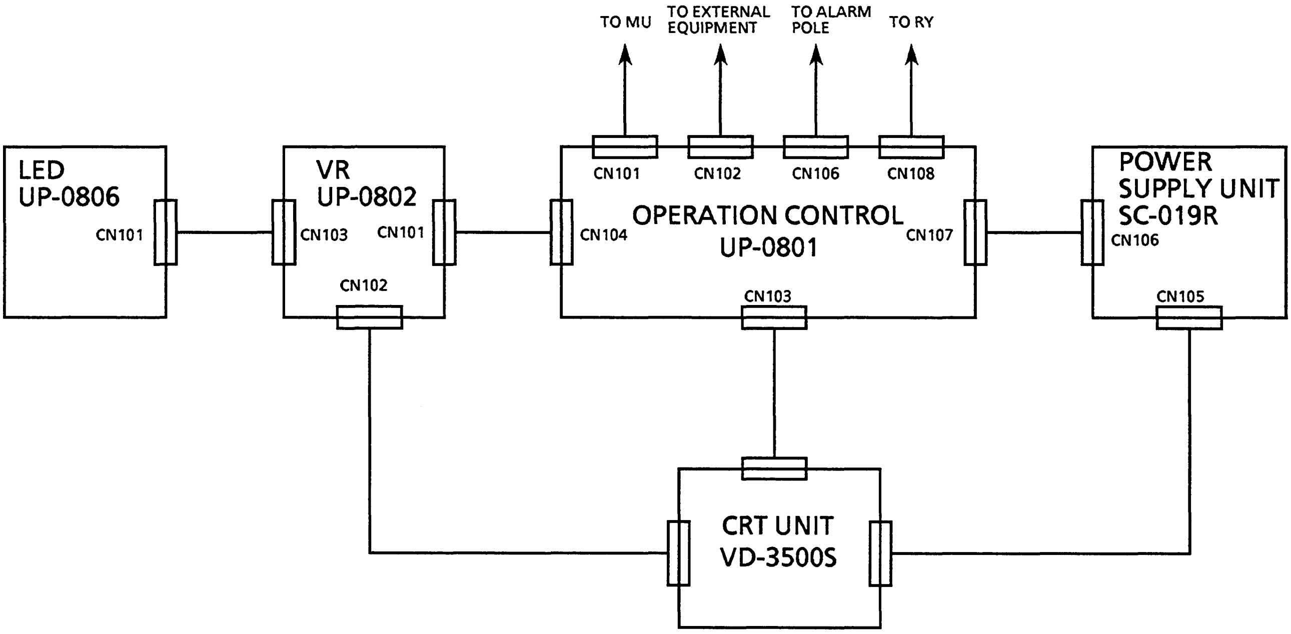
• VIDEO Signal

The OPERATION CONTROL board receives and selects the VIDEO signal from the bedside monitor main unit or the external unit.

Display Unit Power Supply Block Diagram

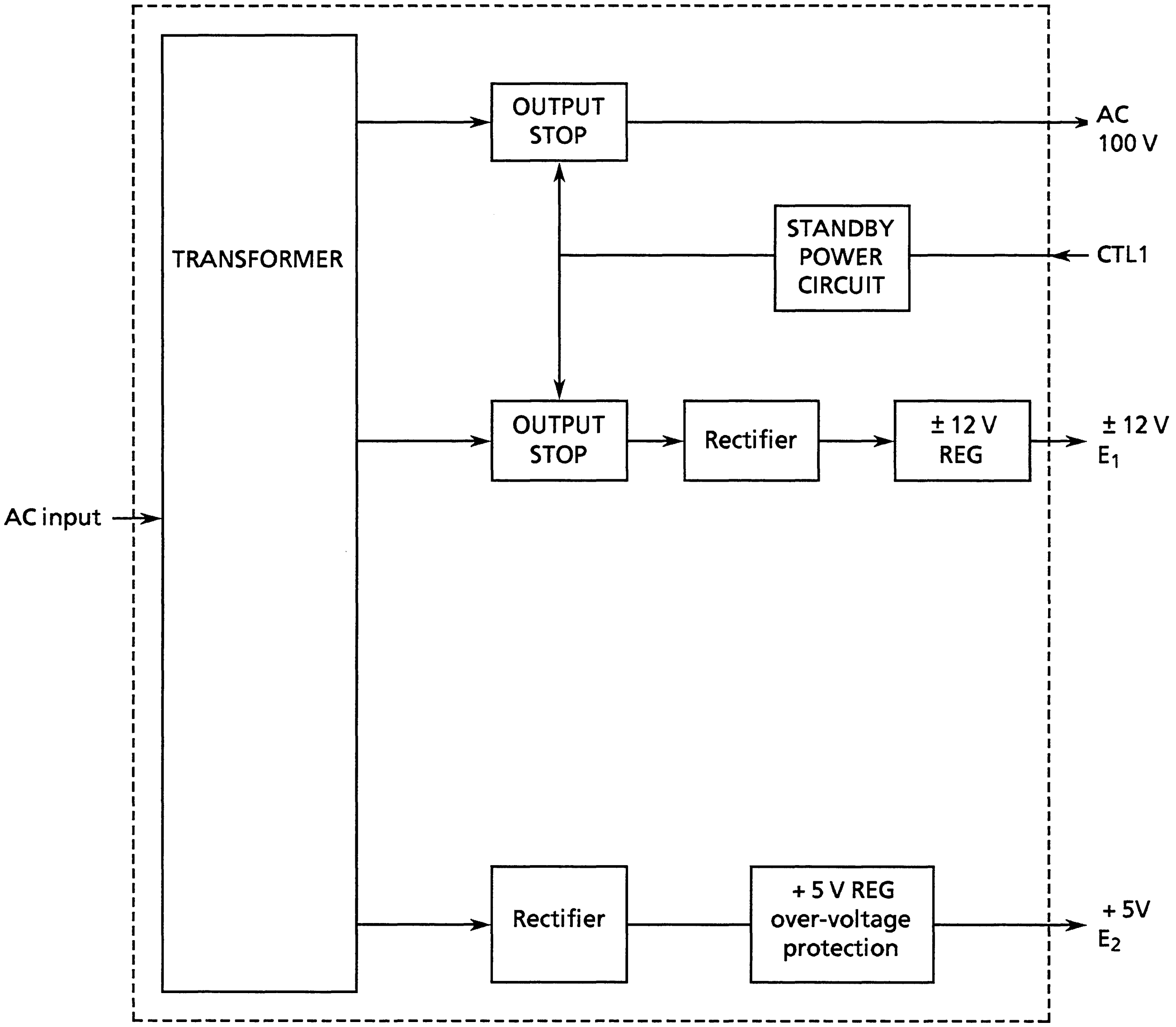

RY-881P
ALARM POLE
E2
+5 V
E2
+12 VA
LED
UP-0806
+12 V, +5 V
E1, E2
VR
UP-0802
+12 V, +5 V
E1, E2
OPERATION CONTROL
UP-0801
+5 V, +12 V
+12 VA, −12 V
E1, E2, E3
POWER
SUPPLY
+12 VC
E1
CRT
VD-3500S
VD-881R

Display Unit Connection Diagram


TO MU
TO EXTERNAL EQUIPMENT
TO ALARM POLE
TO RY
LED
UP-0806
CN101
VR
UP-0802
CN103
CN101
CN102
CN101
CN102
CN106
CN108
OPERATION CONTROL
UP-0801
CN104
CN107
CN103
POWER
SUPPLY UNIT
SC-019R
CN106
CN105
CRT UNIT
VD-3500S

3-5-2 Power Supply Unit, SC-019R

Block Diagram


TRANSFORMER
OUTPUT STOP
AC 100 V
STANDBY POWER CIRCUIT
CTL1
OUTPUT STOP
Rectifier
± 12 V REG
± 12 V
E1
AC input
Rectifier
+ 5 V REG over-voltage protection
+ 5V
E2

◆ General

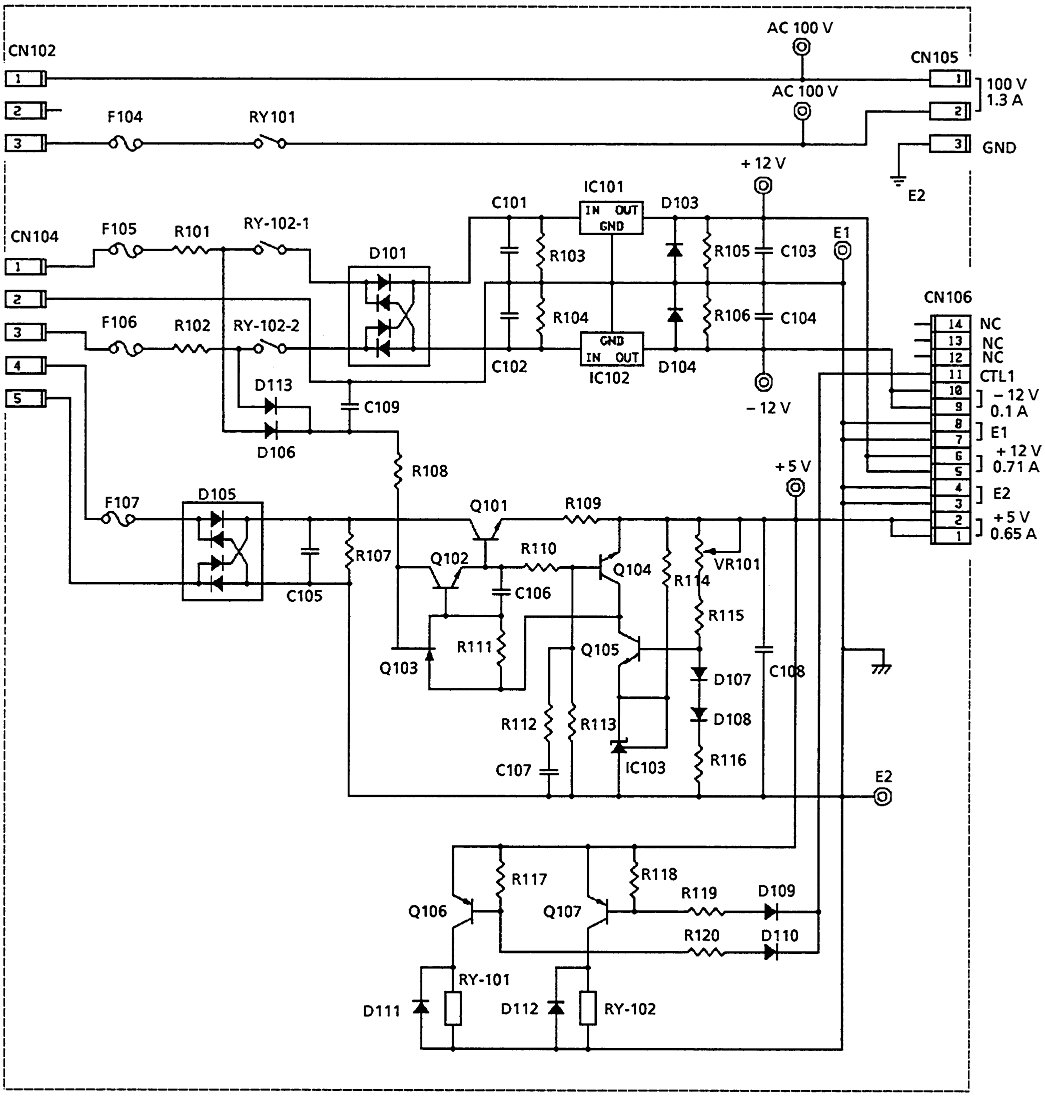
This unit consists of the transformer sub-unit and the regulator sub-unit. The regulator sub-unit also performs as a rectifier as well as an overvoltage protector.

This regulator sub-unit consists of the following circuit:
* +5 V Regulating Circuit
* CTL1 Signal Circuit
* ±12 V Regulating Circuit
* AC 100 V Output

The various power voltage are used and processed as follow:

Voltage	Processing Method	Use
+5 V	Dropper	Digital circuit
±12 V	3 point regulator output	Analog circuit
AC 100 V		CRT unit

◆ Circuit Description


CN102
1
2
3
F104
RY101
AC 100 V
AC 100 V
CN105
1
2
3
100 V
1.3 A
GND
E2
+12 V
IC101
IN OUT
GND
C101
D103
CN104
1
2
3
4
5
F105
R101
RY-102-1
D101
R103
R105
C103
E1
R104
R106
C104
CN106
F106
R102
RY-102-2
GND
IN OUT
IC102
C102
D104
D113
C109
-12 V
D106
R108
+5 V
F107
D105
Q101
R109
R107
Q102
R110
Q104
R114
VR101
C105
C106
R115
R111
Q105
Q103
D107
C108
R112
R113
D108
C107
IC103
R116
E2
R117
R118
R119
D109
Q106
Q107
R120
D110
RY-101
D111
D112
RY-102
14
13
12
11
10
9
8
7
6
5
4
3
2
1
NC
NC
NC
CTL1
-12 V
0.1 A
E1
+12 V
0.71 A
E2
+5 V
0.65 A

◆ + 5V Regulating Circuit

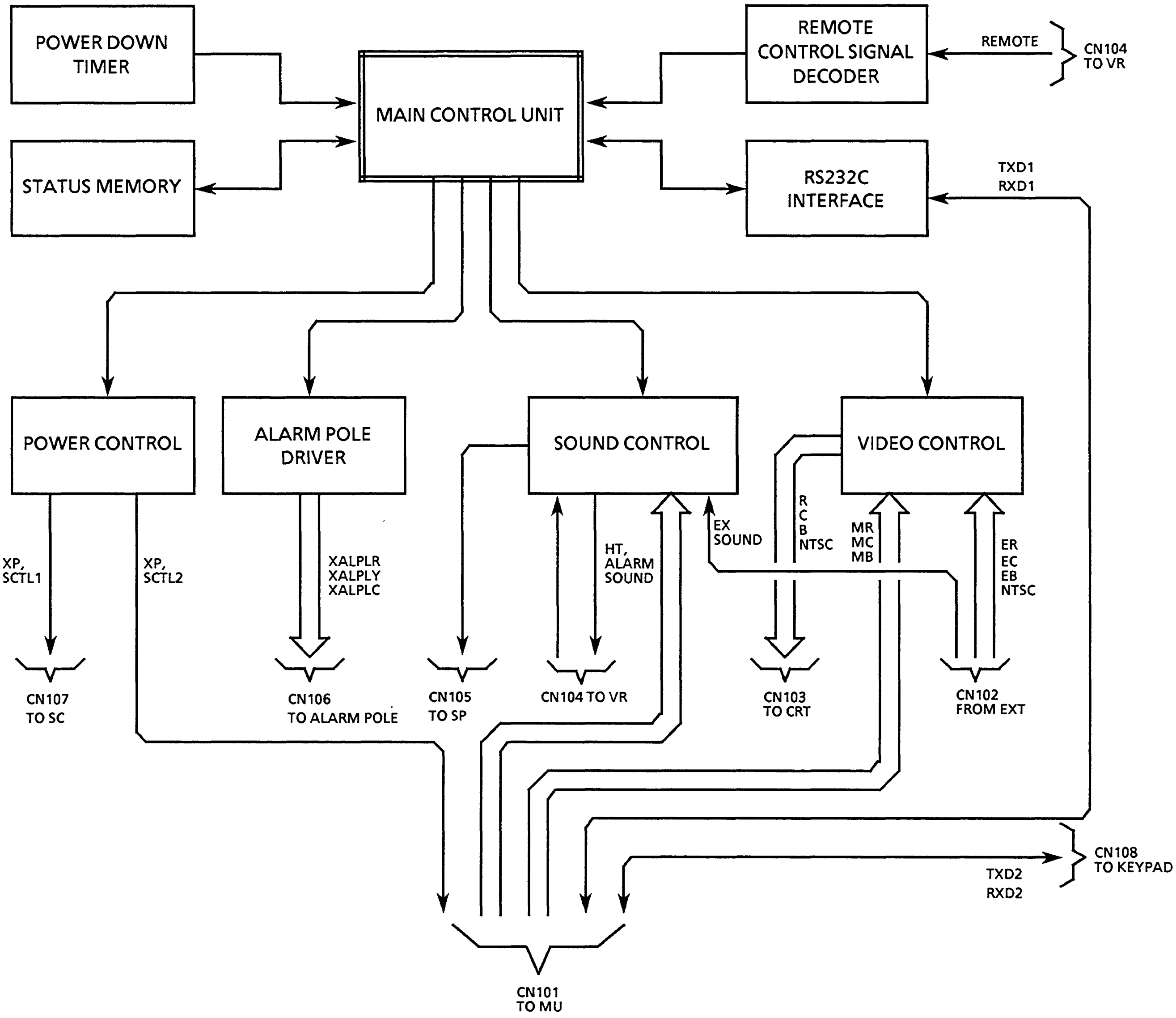
The transistor Q104 is the overvoltage protector. When the output voltage exceeds +5V, Q104 starts to operate since there is a voltage drop across the resistor R109. This decreases the bias of transistor Q101, which in turn decreases the output volatage.

◆ CTL1 Signal Circuit

When the voltage of terminal CTL1 reaches +5V, it switches off the relay RY101 and RY102. This stops the output of the AC 100V and ±12V.

3-5-3 OPERATION CONTROL Board, UP-0801

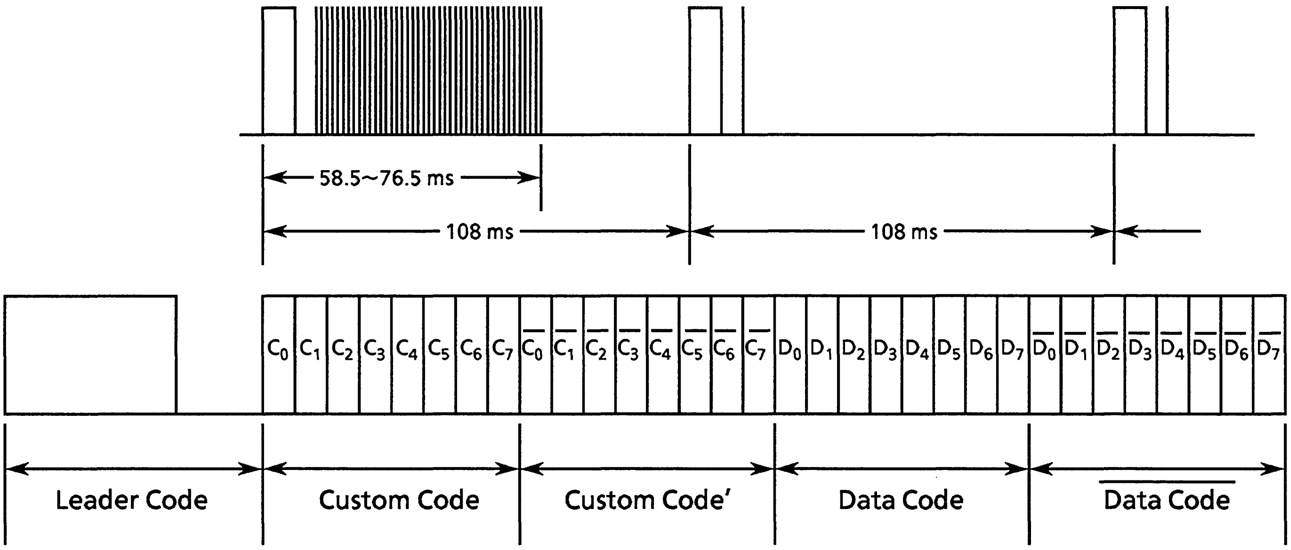
Block Diagram


POWER DOWN TIMER
STATUS MEMORY
MAIN CONTROL UNIT
REMOTE CONTROL SIGNAL DECODER
REMOTE
CN104 TO VR
RS232C INTERFACE
TXD1
RXD1
POWER CONTROL
ALARM POLE DRIVER
SOUND CONTROL
VIDEO CONTROL
XP, SCTL1
XP, SCTL2
XALPLR
XALPLY
XALPLC
HT, ALARM SOUND
EX SOUND
R
C
B
NTSC
MR
MC
MB
ER
EC
EB
NTSC
CN107 TO SC
CN106 TO ALARM POLE
CN105 TO SP
CN104 TO VR
CN103 TO CRT
CN102 FROM EXT
CN108 TO KEYPAD
TXD2
RXD2
CN101 TO MU

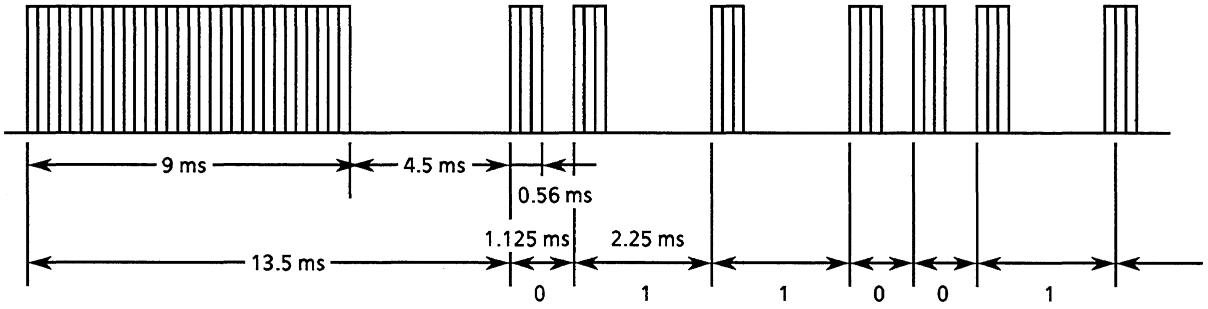
◆ Infra-red Remote Control Receiver Unit

• Format of Remote Control Signal

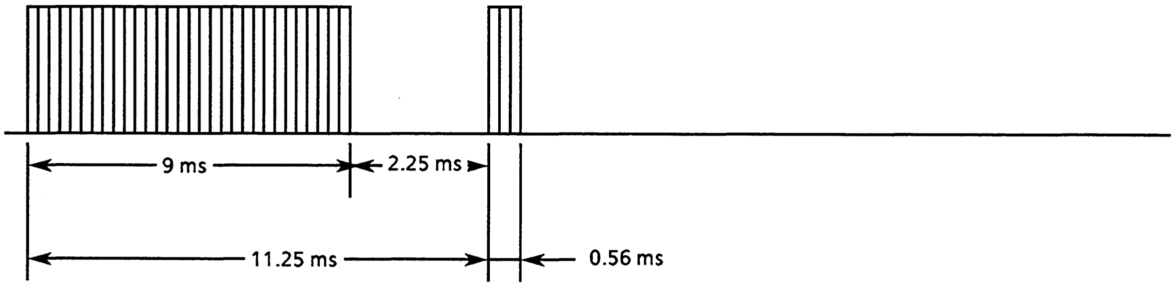
The remote control signal consists of the leader code, 16 bits custom code, 8 bits data code and 8 bits complement data code. The 16 bits custom code contains the code for the type of the remote control sending the signal. The data code contains the information of the pressed key on the remote control.
The infra-red remote control signal is transmitted by PPM modulation.


58.5~76.5 ms
108 ms
108 ms
C_0 C_1 C_2 C_3 C_4 C_5 C_6 C_7 $\overline{C_0}$ $\overline{C_1}$ $\overline{C_2}$ $\overline{C_3}$ $\overline{C_4}$ $\overline{C_5}$ $\overline{C_6}$ $\overline{C_7}$ D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 $\overline{D_0}$ $\overline{D_1}$ $\overline{D_2}$ $\overline{D_3}$ $\overline{D_4}$ $\overline{D_5}$ $\overline{D_6}$ $\overline{D_7}$
Leader Code
Custom Code
Custom Code'
Data Code
$\overline{\text{Data Code}}$

1st time


9 ms
4.5 ms
0.56 ms
1.125 ms
2.25 ms
13.5 ms
0
1
1
0
0
1

2nd time (When the key is continuously pressed)


9 ms
2.25 ms
11.25 ms
0.56 ms

• Remote Control Signal Demodulating Circuit

The 4 bit slave CPU (IC204) demodulates the received signal. If the custom code is correct, the accompanying data of the pressed key is sent, via the serial bus, to the display unit 8 bit master CPU (IC201) for processing.

• Serial Bus Interface

The serial bus interface consists of one serial bus line (SB0) and one serial clock (XSCK) line. The clock frequency is 187.5 kHz.

◆ Power Supply Control Circuit

The function of this circuit is to switch on/off the display unit. This switch is based on the status of the XP.S CTL1 output signal of IC201. The table below shows the logic of the switch.

Selection	XP.S CTL1
Display Power Source OFF	0
Display Power Source ON	1

The XP.S CTL1 exits the OPERATION CONTROL board via Pin No.11 of connector CN107 to the power supply unit. When the terminal becomes LOW, the voltages ±12 V/ +12 V AC, and +5 V are turned on. When the terminal becomes HIGH, only +5 V is turned on.

• Display Unit Power Supply Control

The power supply in the display unit can be controlled by the bedside monitor main unit and the display unit itself. Hence, instructions received from the keypad on the control of the power supply can either be processed in the main unit or the display unit. The operating status of IC201 determines the unit that control the power supply.

The bedside monitor decides the status of the IC201 of the display unit by asserting/negating IC201's status port via its M/S SEL signal. The table below shows the switching process of this decision.

Status port (P23, 30PIN) Input	OperatinG mode
1 (HIGH)	MASTER
0 (LOW)	SLAVE

–Display Unit as the Controller

The display unit functions as the controller when its IC201 is in the master operating mode. The keypad outputs the power supply control output signal, XP.S CTLIN. IC201 receives the XP.S CTLIN, via its port P21 (pin No. 29) and outputs the power supply control output 1 signal, XP.S CTL1, to the power supply unit via the OPERATION CONTROL board connector CN107.

–Bedside Monitor Main Unit as Controller

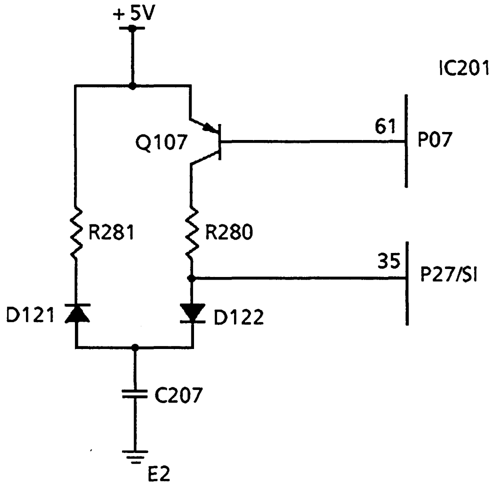
When the IC201 of the display unit is in the slave operating mode, it relays the signal to the bedside monitor main unit for further processing. The IC201 receives the XP.S CTLIN via its port P21, but now it outputs the power supply control output 2 signal, XP.S CTL2, to the bedside monitor main unit via the OPERATION CONTROL board connector CN101.

◆ Status Memory

The status memory is based on a Serial In/Serial Out EEPROM (IC206). The function of this status memory is to set the CPU setting back to its last setting prior to any unintentional resetting or power down, software malfunction, and others.

The status memory contains the following information.
* Video input and output switching (INTERNAL/EXTERNAL)
* Video output switching (Separate Sink/Composite Sink)
* Display power supply output control (ON/OFF)

◆ Low Voltage Monitor Timer



This timer monitors the instantaneous loss of power supply in the display unit. During power down condition, the capacitor C207 supplies the back-up power when there is a drop in the +5 V voltage. If the voltage drops to +0 V, the capacitor will discharge its stored electricity for a period determined by resistor R281 and capacitor C207.

When the system is reset after a power down condition, the CPU reads the value of voltage at port P35. If the value is "1", the CPU interprets that the power was on prior to reset, and therefore switches the display power on.

After the power is restored, the CPU writes the instruction to recharge the capacitor. The transistor Q107 redirect the current to the capacitor.

◆ Serial Communication

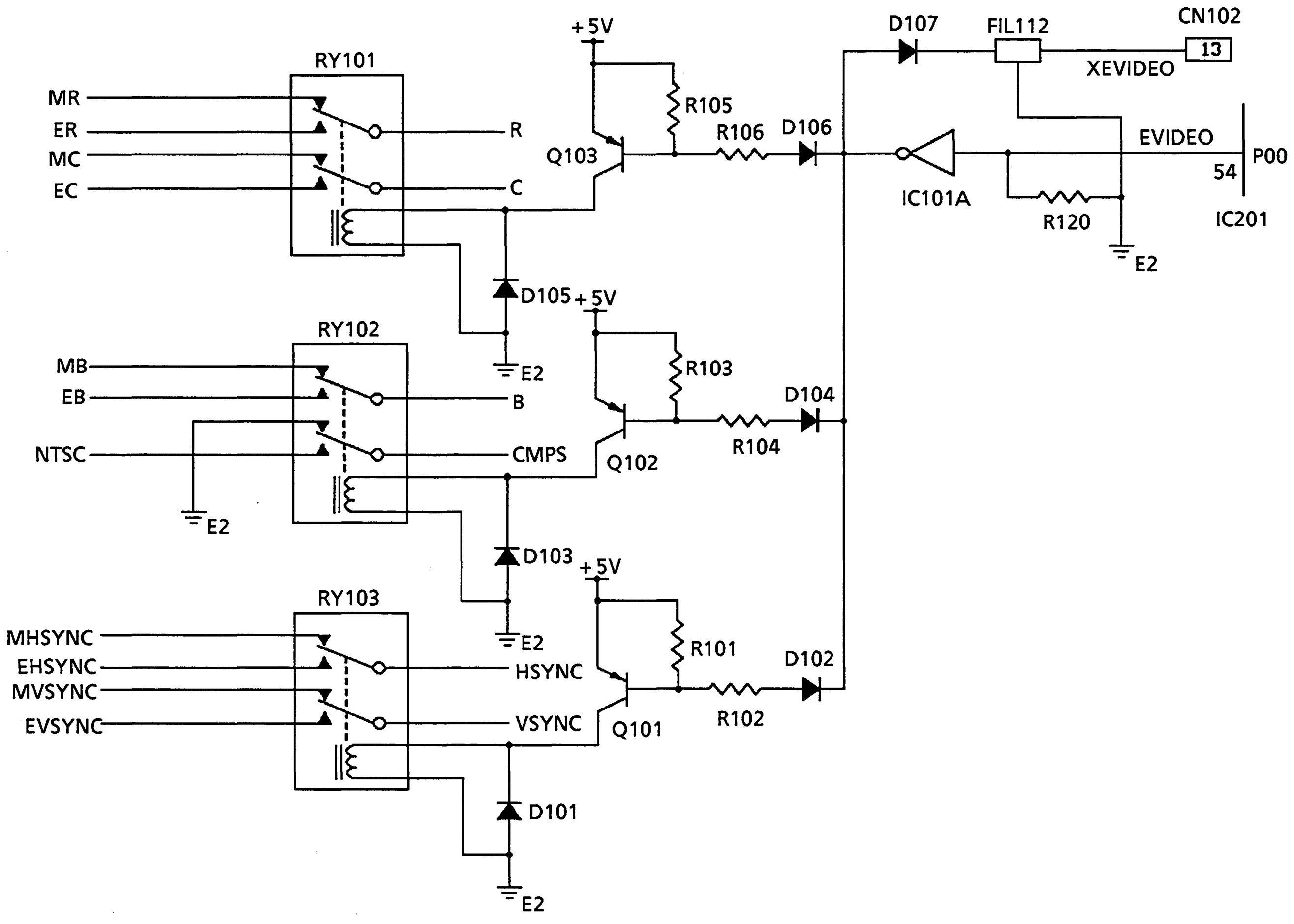
The communication format is as follow:
* RS-232C Communication
* Baud Rate : 4800/9600 BPS (hardware switch)
* Character Length : 8 bits
* Stop Bit Value : 1 bit
* Operation Mode : ASYNC
* Parity : None

The baud rate depends on the value of the CPU input port (P25). When the value is "1", the baud rate is 4800 BPS; when the value is "0", the baud rate is 9600 BPS.

The CPU will begin sending its data when the READY signal is asserted (HIGH).

◆ Video Signal Control

Video Signal Control Circuit


+5V
RY101
MR
ER
MC
EC
R
C
Q103
R105
R106
D106
D105
+5V
E2
RY102
MB
EB
NTSC
B
CMPS
Q102
R103
R104
D104
E2
D103
+5V
RY103
MHSYNC
EHSYNC
MVSYNC
EVSYNC
HSYNC
VSYNC
Q101
R101
R102
D102
D101
E2
D107
FIL112
CN102
13
XEVIDEO
EVIDEO
IC101A
R120
E2
P00
54
IC201

• Main Unit/External Unit RGB Signal Selection

- Software Control

The IC201 on this OPERATION CONTROL board can select the source of the RGB signals. The source can be from the main unit or an external unit. The status of the IC201's EVIDEO signal output determines the selection. The switching process is based on transistors Q101 - 103 and relays RY101 - 103.

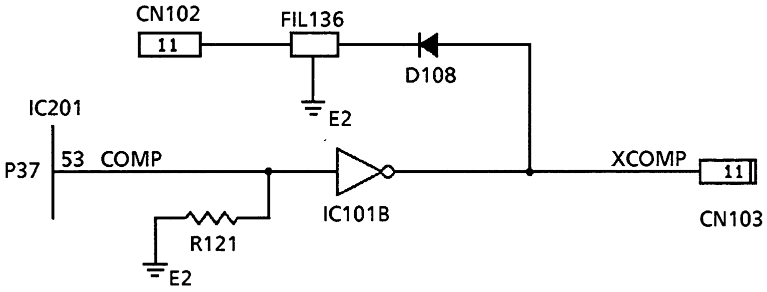
The table below shows the statuses of the EVIDEO signal output and their selections.

Selection	EVIDEO
RGB signal from the main unit	0
RGB signal from external units	1

- Hardware Control

Switching to received the RGB signals from the external unit can also be done through the connection between the OPERATION CONTROL board and the external unit. If the pin No. 13 of connector CN102 is LOW, the same transistor Q101 - 103 and relays RY101 - 103 select the RGB signals from the external unit.

• CRT Unit Operation Mode Selection Circuit



The CRT unit can operate in the RGB mode as well as the NTSC mode. The selection is again by software or hardware control. The status of the XCOMP signal sets the operating mode of the CRT unit. The table below shows the status of the XCOMP and its operating mode settings.

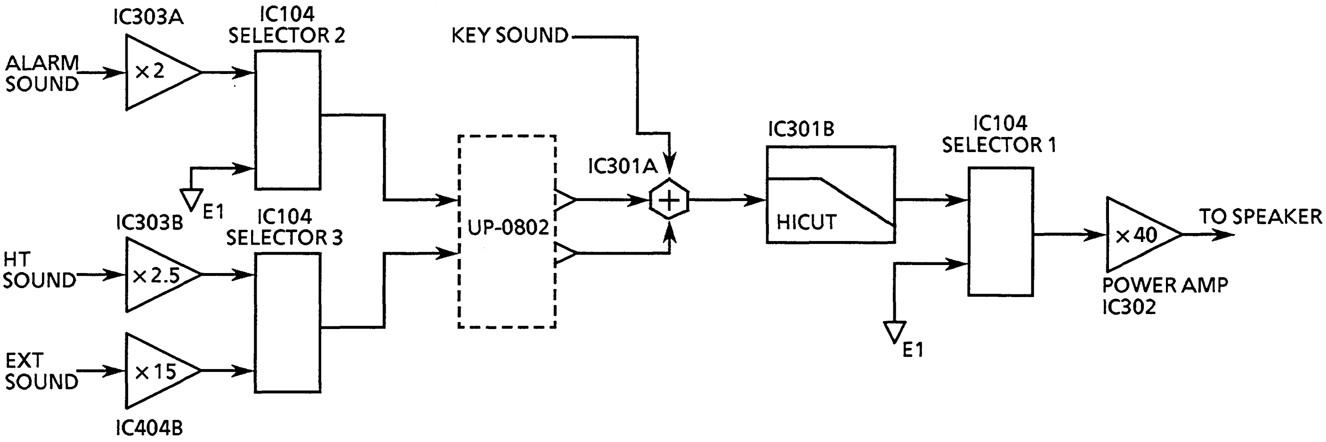
Operation mode	XCOMP
RGB IN	1
NTSC IN	0

- Software Control
The IC201 outputs the COMP signal through its port P37. The COMP signal is inverted by IC101B, and the resulting signal XCOMP is outputted to the CRT unit via the OPERATION CONTROL Board connector CN103.

- Hardware Control
The status on pin No. 11 of the external unit connector CN102 informs the CRT unit whether to display under the RGB mode or the NTSC mode. When the pin No. 11 is LOW, the CRT is to operate on the NTSC mode, and when it is HIGH, the RGB mode.

◆ Sound Signal

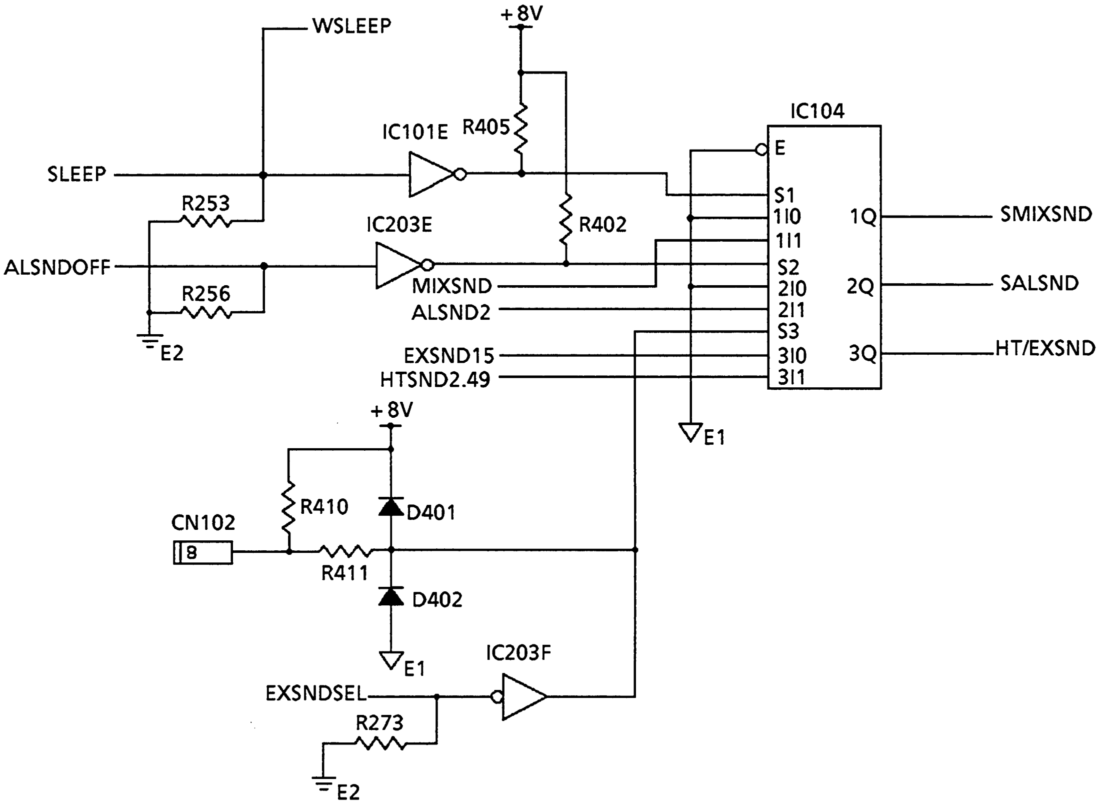
• Sound Signal Flow


IC303A
IC104
SELECTOR 2
KEY SOUND
ALARM SOUND
×2
E1
IC303B
IC104
SELECTOR 3
HT SOUND
×2.5
EXT SOUND
×15
IC404B
UP-0802
IC301A
IC301B
HICUT
IC104
SELECTOR 1
E1
×40
TO SPEAKER
POWER AMP
IC302

There are three kinds of sounds, alarm sound, QRS sound, and external sound. The alarm sound and the QRS sound originate from the bedside monitor main unit. The external sound originates from the external unit. These sound signals undergo amplification, selection, volume adjustment, key sound addition, noise filtering, final selection, power amplification before outputted to the speaker.

• Sound Signal Control

Sound Signal Control Circuit


WSLEEP
+8V
IC104
IC101E
R405
SLEEP
R253
R402
IC203E
ALSNDOFF
R256
E2
MIXSND
ALSND2
EXSND15
HTSND2.49
E
S1
1I0
1I1
S2
2I0
2I1
S3
3I0
3I1
1Q
2Q
3Q
SMIXSND
SALSND
HT/EXSND
E1
+8V
CN102
8
R410
D401
R411
D402
E1
IC203F
EXSNDSEL
R273
E2

- Software Control

The IC201 outputs the sound control signals (SLEEP, ALSNDOFF, EXSNDSEL). The IC104 reads the statuses of these signals and determines the selection. The status of EXSNDSEL signal determines the selection between the QRS sound mode or external sound mode. The status of ALSNDOFF signal determines the ON/OFF mode of the alarm. The status of SLEEP signal determines the ON/OFF of the whole sound unit.

The tables below show the statuses of the signal outputs and their selections.

Selection	EXSNDSEL
QRS sound output mode	0
External sound mode	1

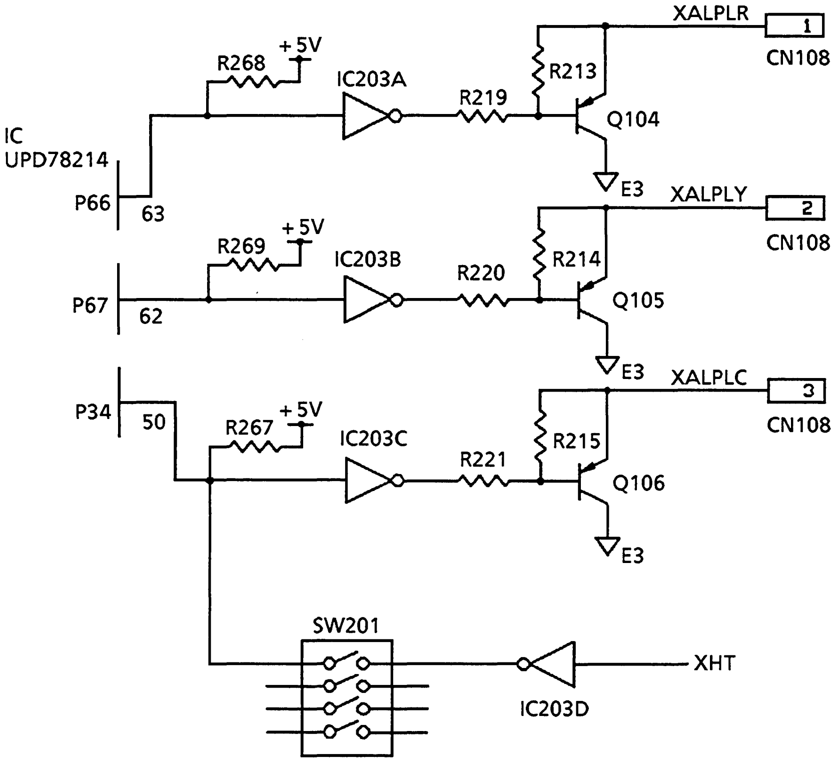
Selection	ALSNDOFF
Alarm ON	0
Alarm OFF	1

Selection	SLEEP
Whole sound unit ON	0
Whole sound unit OFF	1

- Hardware Control

The external unit can only control the selection between the QRS sound output mode or external sound mode. When the pin No. 8 of the external unit connector CN102 is LOW, the sound unit outputs the external sound; when OPEN, the sound units outputs the QRS sound.

◆ Alarm Pole Control


XALPLR
1
CN108
+5V
R268
IC203A
R213
R219
Q104
IC
UPD78214
P66
63
E3
XALPLY
2
CN108
+5V
R269
IC203B
R220
R214
Q105
P67
62
E3
XALPLC
3
CN108
P34
50
+5V
R267
IC203C
R215
R221
Q106
E3
SW201
XHT
IC203D

• Software Control

The IC201's PIN63 switches the alarm pole's red light on/off. The IC201's PIN62 switches the alarm pole's yellow light on/off. The IC201's PIN50 switches the alarm pole's green light on/off.

• XHT Signal

The XHT signal only controls the alarm's pole green light. When the active-low XHT signal is asserted, the alarm pole's green continues to light up. When the active-low XHT signal is negated, it switches off the alarm pole's green light.

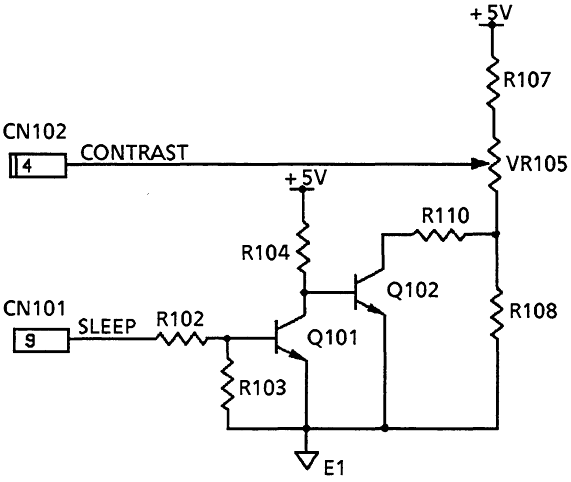
3-5-4 OPERATION (VR) Board, UP-0802

◆ Brightness and Contrast Adjustment

For brightness adjustment, adjust the variable resistor VR103 until the voltage on pin No. 1 of the OPERATION (VR) board's connector CN102 reach a certain value. For contrast adjustment, adjust the variable resistor VR105 until the voltage on pin No. 4 of the OPERATION (VD) board's connector CN102 reach a certain value.

◆ Sleep Control

Sleep Control Circuit



The active ("0") SLEEP signal on pin No. 9 of the OPERATION (VR) board's bedside monitor main unit connector CN101 causes the impedance between the variable resistor VR103 and pin E1 to drop. This in turn causes the voltage of the CONTRAST signal output of pin No. 4 of the OPERATION (VR) board's CRT unit connector CN102 to drop.

◆ Sound Adjustment

Adjustment on the variable resistors VR101 and VR102 attenuate the sound signal on pin Nos. 1 and 3 respectively of the OPERATION (VR) board's OPERATION CONTROL board connector CN101.

3-5-5 LED Board, UP-0806

The LED board has one LED that goes off during the standby mode, one LED that lights up when power is switched on, and an infra-red sensor for the remote control. The infra-red sensor circuit has a noise filter. This circuit outputs the TTL level signal.

Section 4 SELFCHECK

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- 4-2-2 DPU (Data Processing Unit) Board 4.4
- 4-2-3 COM3 (Communication) Board 4.4

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- 4-3-3 Patient Monitor Mode 4.9
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        - ● Global Memory Check 4.14
        - ● Key Check 4.15
        - ● Sound Check 4.16
        - ● RS232C Check 4.17
        - ● RY/VD COM Check 4.18
        - ● Memory Card Check 4.21
        - ● Alarm Pole Check 4.22
        - ● DIP SW/LED/STATUS Check 4.23
        - ● Other Check 4.24
    - ◆ CRTC (CRT Control board) Check 4.25
        - ● WAVE RAM Check 4.26
        - ● CHARACTER RAM Check 4.27
        - ● GRAPHIC RAM Check 4.28
        - ● PALETTE RAM Check 4.29
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        - ● GRAPHIC Display Check 4.37

◆ DPU (Data Processing Unit board) check 4.39
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- Global Memory Check 4.42
- A/D RAM Check 4.43
- D/A - A/D Loop Check 4.44
- JA Check (Input Box Check) 4.45
- NIBP AMP Check (AP-851P) 4.46
- NIBP AMP Check (AP-860P) 4.47
- CO2 AMP Check (AG0830P) 4.49
- D/A WAVE RAM Check 4.50
- A/D - D/A Check 4.51
- HEAD AMP Control 4.53
- DIP SW/LED Check 4.54
- OUTPUT Check 4.55
- Other Check 4.56
- FIELD STRENGTH Check 4.57

◆ COM check (Communication board check) 4.58
- ROM Check 4.59
- RAM Check 4.60
- GLOBAL MEMORY Check (from COM) 4.61
- GLOBAL MEMORY Check (from CPU) 4.62
- CNS COMMUNICATION Check 4.63
- WS RECORD Check (Recorder Check) 4.64
- DIP SW/LED Check 4.66
- INTERBED SELECT Check 4.67
- D/A WAVE Check 4.68

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4-1 General

The following SELF CHECK programs are provided.

1. POWER-ON INITIAL SELF CHECK
2. MANUAL SELF CHECK

Each SELF CHECK PROGRAM consists of the following check items.

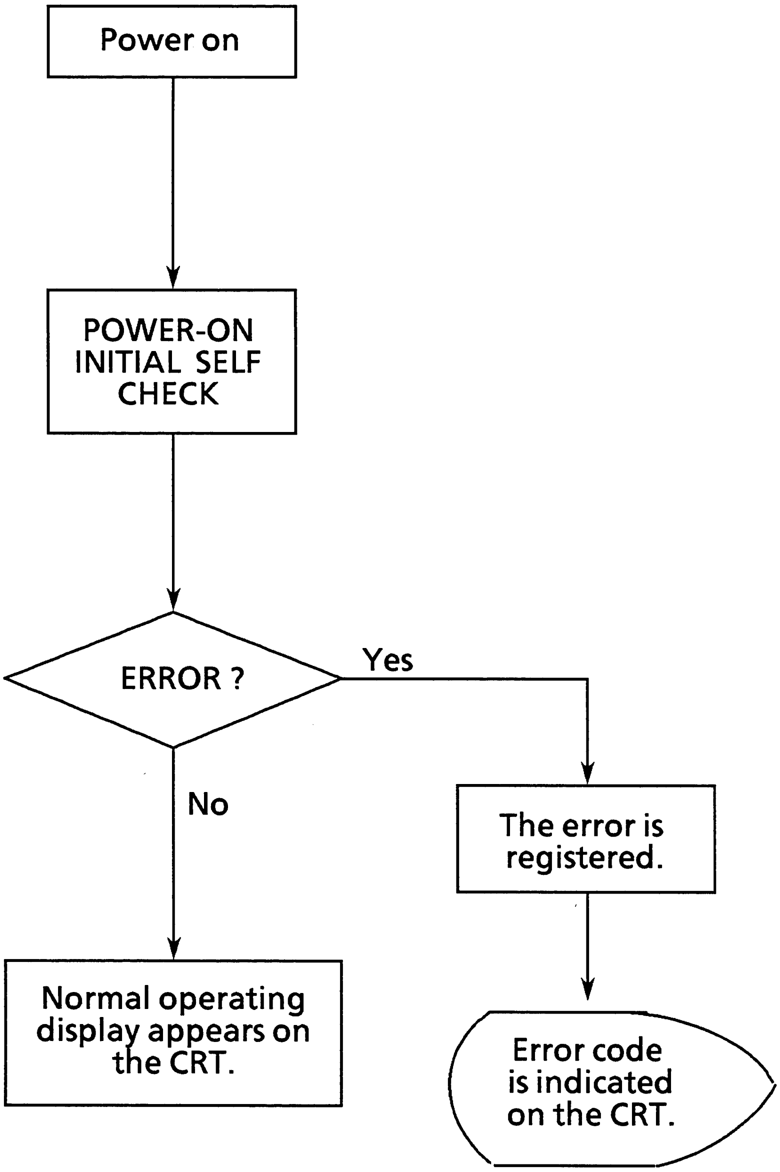
	POWER-ON INITIAL SELF CHECK	MANUAL (SELF) CHECK
CPU	ROM RAM 8279 (I/O) 71051 (I/O) 72001 (I/O) E^{2}PROM Global Memory (GLB.RAM) DPU Communication COM Communication [on DPU & COM board]	ROM RAM Global Memory (DPU) KEY (8279) SOUND (8279) RS232C (71051) RY/VD COM MEMORY CARD ALARM POLE DIP SW/LED/STATUS OTHER
CRTC		WAVE RAM CHARACTER RAM GRAPH RAM PALLET RAM Wave Display Character Display Graph Display
DPU	ROM RAM Global Memory (GLB.RAM) A/D-D/A Loop (A/D) Timing Port (RTC)	ROM RAM Global Memory (DPU) A/D RAM D/A-A/D Loop JA NIBP AMP (AP-851P) NIBP AMP (AP-860P) tcPO$_2$/tcPCO$_2$ AMP (AG-810P) CO$_2$ AMP (AG-830P) D/A WAVE D/A-A/D HEAD AMP CONTROL DIP SW/LED OUTPUT OTHER FIELD STRENGTH
COM3	ROM (from 8085) RAM (from 8085) 8251 (I/O) RTC	ROM RAM Global Memory (from COM3) Global Memory (from CPU) Communication WS RECORD DIP SW/LED INTERBED SELECT D/A Wave

NOTE

Global Memory: **The memory that can be accessed not only by the specific device but also by the other device.**

4-2 Power-On Initial Self Check

This check program is automatically executed whenever the power switch is turned on. If there is a problem, the display changes to DIAGNOSTIC CHECK AND SYSTEM SETUP display with the error indication while the error code is registered on ERROR HISTORY.


Power on
POWER-ON INITIAL SELF CHECK
ERROR ?
Yes
No
The error is registered.
Normal operating display appears on the CRT.
Error code is indicated on the CRT.

4-2-1 CPU Board

(1) ROM check
The ROM check is executed by comparing the value of the acquired sum of data except the value at the last address with the prestored checksum at the last address. If the values do not coincide, the error code is indicated on the CRT. Refer to ERROR CODE explanation (Section 5-3-2 & 3 at the page 5-6).

(2) RAM check (including Global Memory check on DPU, COM board)
The RAM check is executed by comparing each word after being written into the memory area of the RAM with "5555"H to be written as a test pattern. If a word is not "5555"H, the error code is indicated on the CRT.

(3) 8279 (Programmable keyboard/display controller) check
The check is executed by comparing each byte after being written into the memory area of the internal RAM (LED DISPLAY RAM) with "FF"H or "55"H to be written as a test pattern.

(4) 71051 (Programmable communication controller interface) check
Two bits of the status register of 71051, "Tx" and "Rx", are checked.

(5) 72001 (Advanced multi protocol controller)
Read and write return loop check.

(6) EEPROM, 58C65 check
The check is executed by means of Cyclic Redundancy Check (C.R.C.).

(7) Communication check between CPU board and DPU board
The MPU on the DPU board inverts all the words after the MPU on the CPU board writes a test pattern "5555"H into the memory area of the Global Memory on the DPU board. The check is executed by comparing each word with "AAAA"H.

(8) Communication check between CPU board and COM board
The MPU on the COM board inverts all the words after the MPU on the CPU board writes a test pattern "5555"H into the memory area of the Global Memory on the COM board. The check is executed by comparing each word with "AAAA"H.

4-2-2 DPU (Data Processing Unit) Board

(1) ROM check
The check is the same as the ROM check on the CPU board.

(2) RAM check (including Global Memory check on DPU board)
The check is the same as the RAM on the CPU board.

(3) A/D - D/A Loop check
The check is the same as "A/D - D/A Loop check" in MANUAL (SELF) CHECK.

(4) Timing Port check
The check is executed by verifying that the data acquires a increment after reading a stored data of the TIMING PORT every 1 millisecond.

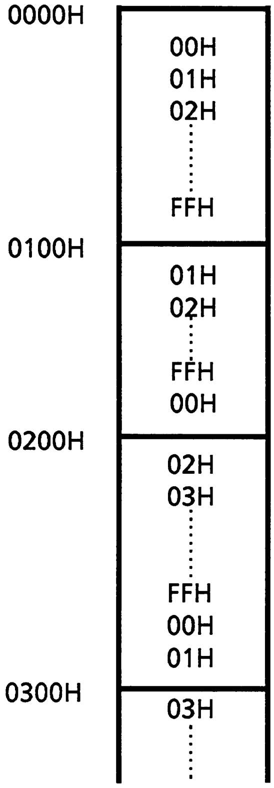
4-2-3 COM3 (Communication) Board

(1) RTC (Real Time Clock) check
The check is executed by comparing the interval time of the periodic interrupt with the value counted by the software counter.

(2) 8251 (for Central Monitor Interface) check
Two bits of the Input /Output (I/O) Port, "Tx" and "Rx", are checked.

(3) RAM check (from COM3)

The following test pattern is used to be written into the RAM. The check is executed every 256 byte by comparing the data after being written into the RAM with each data of the test pattern.


0000H
00H
01H
02H
FFH
0100H
01H
02H
FFH
00H
0200H
02H
03H
FFH
00H
01H
0300H
03H

(4) Global Memory check (from CPU)

Same procedure as RAM Check.

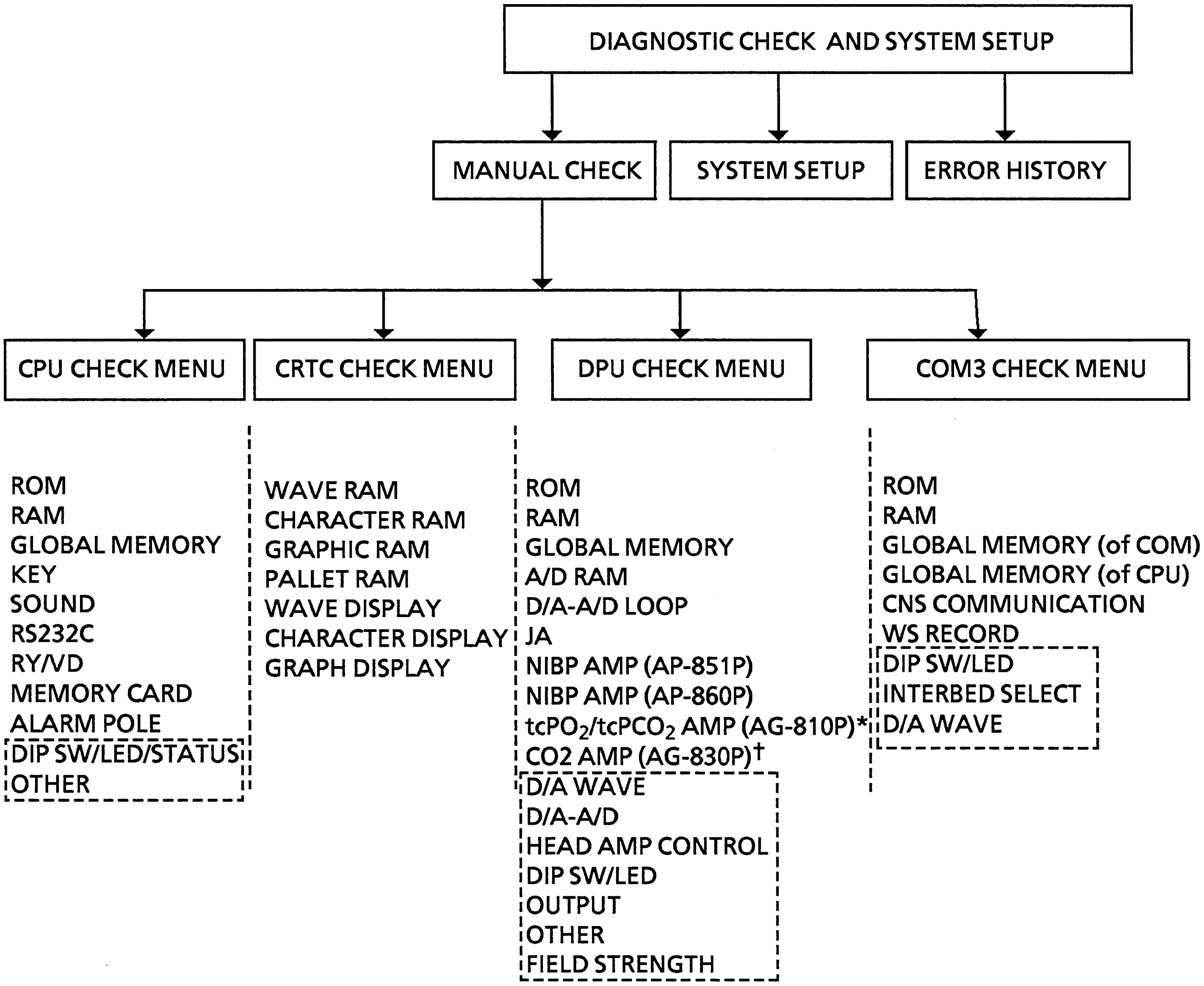
(5) ROM check (from CPU)

The check is the same as the ROM on the CPU board.

4-3 Manual (Self) Check

The Manual (Self) check program [CHECK MENU] is included in ”Diagnostic Check and System Setup” display as follows:

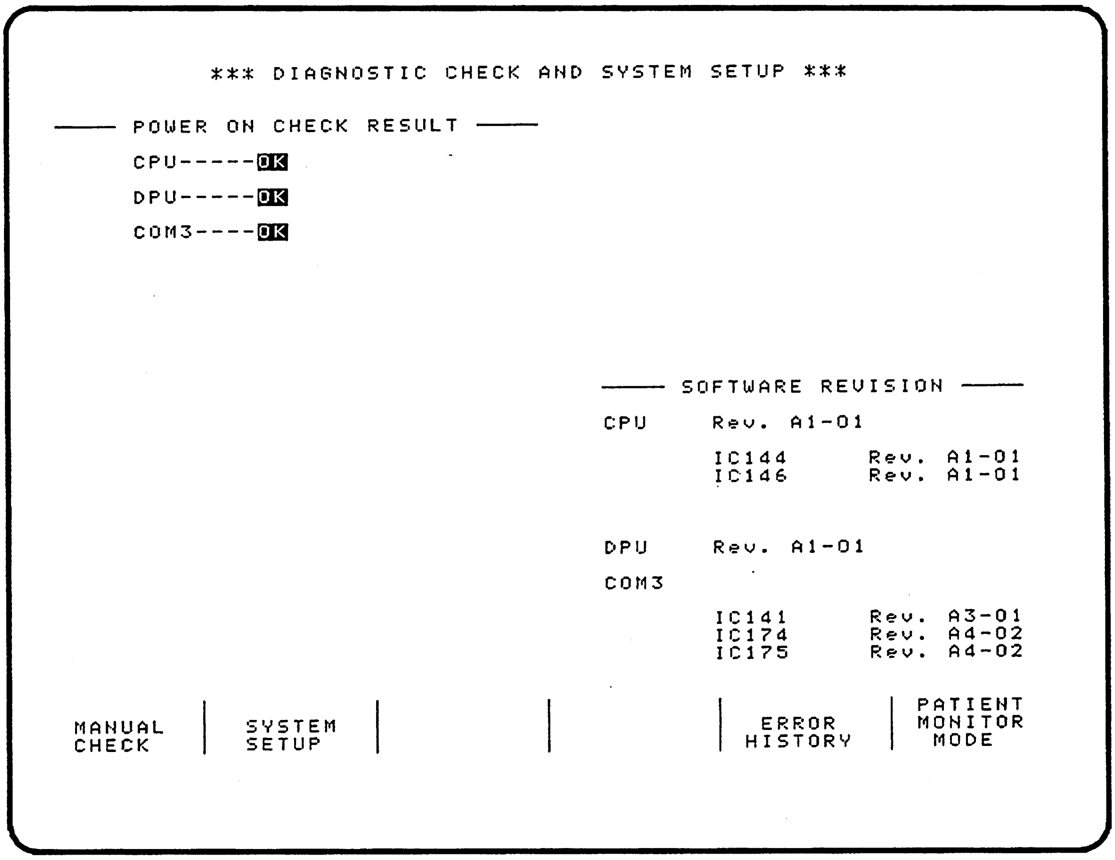
[PROGRAM HIERARCHY STRUCTURE]


DIAGNOSTIC CHECK AND SYSTEM SETUP
MANUAL CHECK
SYSTEM SETUP
ERROR HISTORY
CPU CHECK MENU
CRTC CHECK MENU
DPU CHECK MENU
COM3 CHECK MENU
ROM
RAM
GLOBAL MEMORY
KEY
SOUND
RS232C
RY/VD
MEMORY CARD
ALARM POLE
DIP SW/LED/STATUS
OTHER
WAVE RAM
CHARACTER RAM
GRAPHIC RAM
PALLET RAM
WAVE DISPLAY
CHARACTER DISPLAY
GRAPH DISPLAY
ROM
RAM
GLOBAL MEMORY
A/D RAM
D/A-A/D LOOP
JA
NIBP AMP (AP-851P)
NIBP AMP (AP-860P)
tcPO2/tcPCO2 AMP (AG-810P)*
CO2 AMP (AG-830P)†
D/A WAVE
D/A-A/D
HEAD AMP CONTROL
DIP SW/LED
OUTPUT
OTHER
FIELD STRENGTH
ROM
RAM
GLOBAL MEMORY (of COM)
GLOBAL MEMORY (of CPU)
CNS COMMUNICATION
WS RECORD
DIP SW/LED
INTERBED SELECT
D/A WAVE

⬚ : Press the REVIEW key first before pressing the “MANUAL CHECK” multifunction key to display the check items in the dotted rectangle.

*** Available in Japan only.**
† Not available in the U.S.

The following “Diagnostic Check and System Setup”display appears on the CRT by pressing the SELF CHECK key on the operation panel for three seconds, or switching on the main power switch while pressing the SUSPEND key.

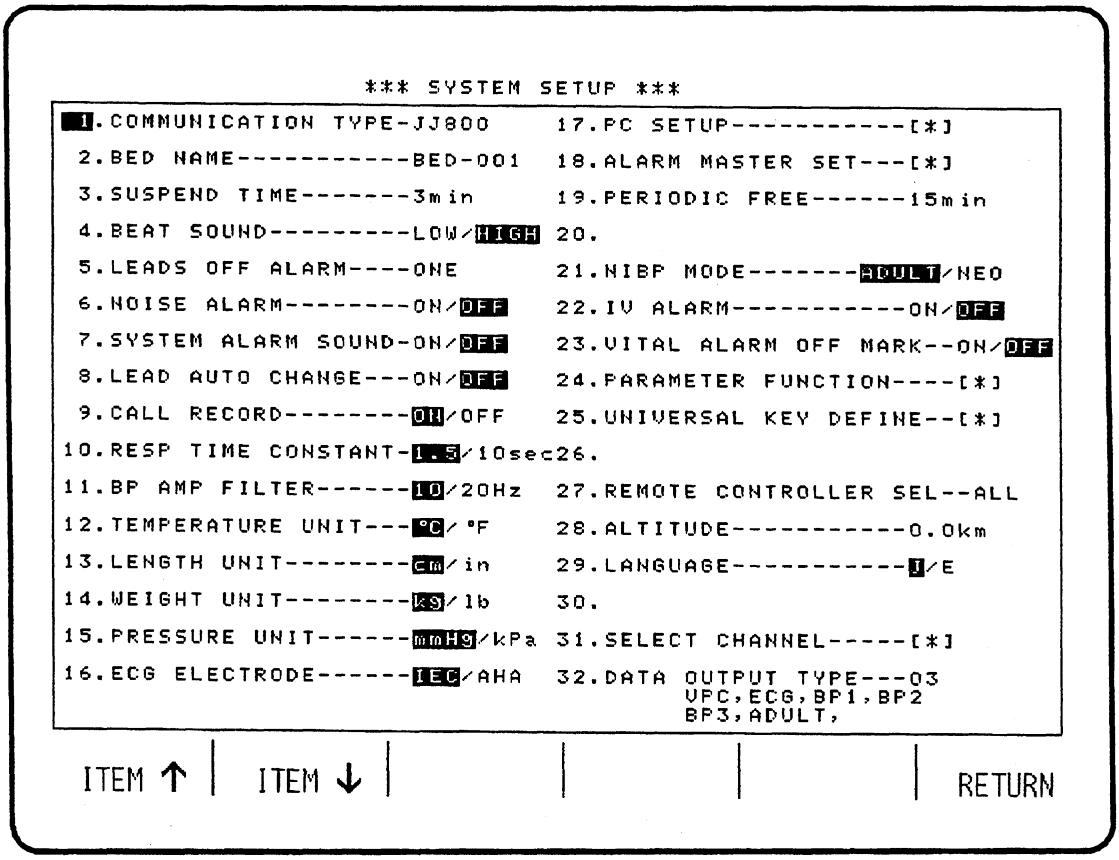


```
          *** DIAGNOSTIC CHECK AND SYSTEM SETUP ***

 ------ POWER ON CHECK RESULT ------
        CPU-----OK
        DPU-----OK
        COM3----OK




                                          ------ SOFTWARE REVISION ------
                                          CPU     Rev. A1-01
                                                  IC144       Rev. A1-01
                                                  IC146       Rev. A1-01

                                          DPU     Rev. A1-01
                                          COM3
                                                  IC141       Rev. A3-01
                                                  IC174       Rev. A4-02
                                                  IC175       Rev. A4-02

                                                                  PATIENT
 MANUAL   |  SYSTEM   |            |            |   ERROR     |   MONITOR
 CHECK    |  SETUP    |            |            |  HISTORY    |    MODE
```

On the above display, MANUAL CHECK, SYSTEM SETUP, ERROR HISTORY or PATIENT MONITOR MODE (Normal Operating mode) can be selected by pressing a multifunction key related to each mode.

4-3-1 System Setup

When SYSTEM SETUP is selected by pressing the SYSTEM SETUP key, the display changes to the following display.

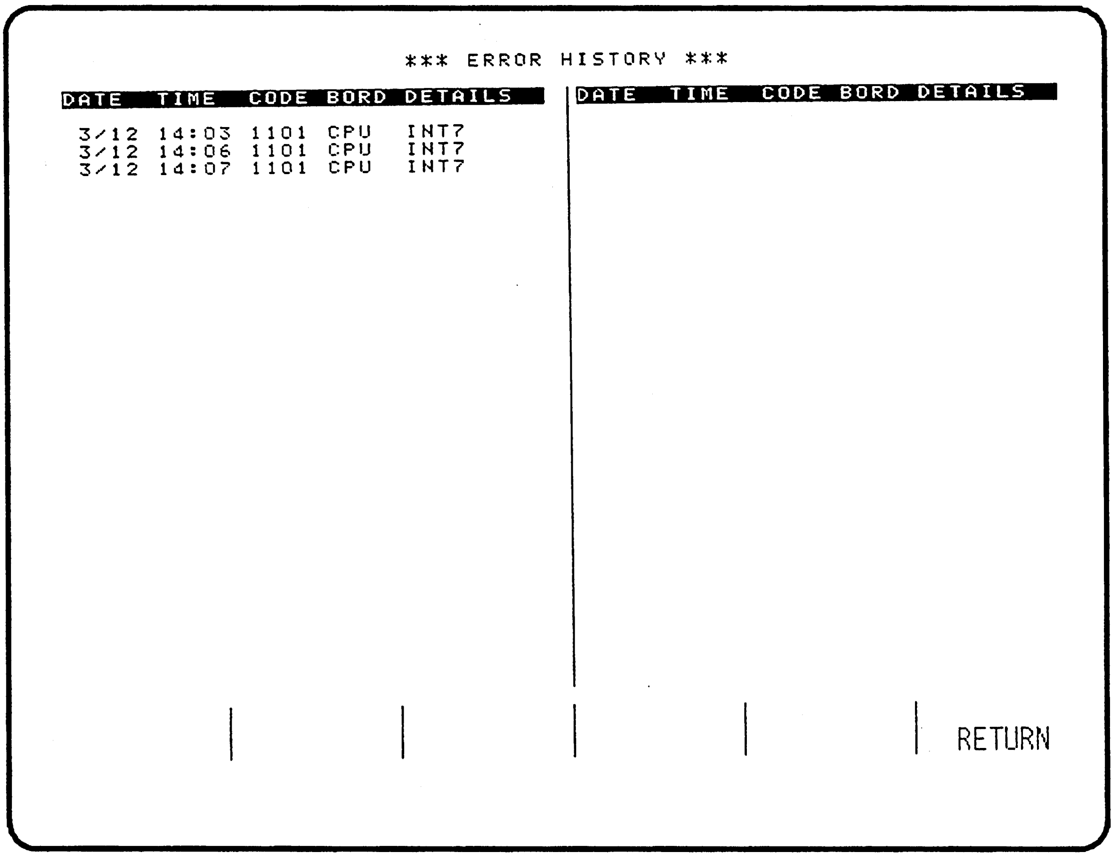


```
                    *** SYSTEM SETUP ***
 1.COMMUNICATION TYPE-JJ800    17.PC SETUP-----------[*]
 2.BED NAME-----------BED-001  18.ALARM MASTER SET---[*]
 3.SUSPEND TIME-------3min     19.PERIODIC FREE------15min
 4.BEAT SOUND---------LOW/HIGH 20.
 5.LEADS OFF ALARM----ONE      21.NIBP MODE-------ADULT/NEO
 6.NOISE ALARM--------ON/OFF   22.IV ALARM-----------ON/OFF
 7.SYSTEM ALARM SOUND-ON/OFF   23.VITAL ALARM OFF MARK--ON/OFF
 8.LEAD AUTO CHANGE---ON/OFF   24.PARAMETER FUNCTION----[*]
 9.CALL RECORD--------ON/OFF   25.UNIVERSAL KEY DEFINE--[*]
10.RESP TIME CONSTANT-1.5/10sec26.
11.BP AMP FILTER------10/20Hz  27.REMOTE CONTROLLER SEL--ALL
12.TEMPERATURE UNIT---°C/ °F   28.ALTITUDE-----------0.0km
13.LENGTH UNIT--------cm/ in   29.LANGUAGE-----------J/E
14.WEIGHT UNIT--------kg/ lb   30.
15.PRESSURE UNIT------mmHg/kPa 31.SELECT CHANNEL-----[*]
16.ECG ELECTRODE------IEC/AHA  32.DATA OUTPUT TYPE---03
                                       VPC,ECG,BP1,BP2
                                       BP3,ADULT,
```

All the above conditions can be modified by pressing multifunction keys related to the up/downward key or right/leftward key after selecting a item by pressing the "ITEM ↑" or "ITEM ↓" multifunction key.

4-3-2 Error History

When ERROR HISTORY is selected by pressing the ERROR HISTORY key, the display changes to the following display.



```
                    *** ERROR HISTORY ***
DATE  TIME   CODE BORD DETAILS     DATE  TIME   CODE BORD DETAILS

 3/12 14:03 1101 CPU   INT7
 3/12 14:06 1101 CPU   INT7
 3/12 14:07 1101 CPU   INT7

                                                         RETURN
```

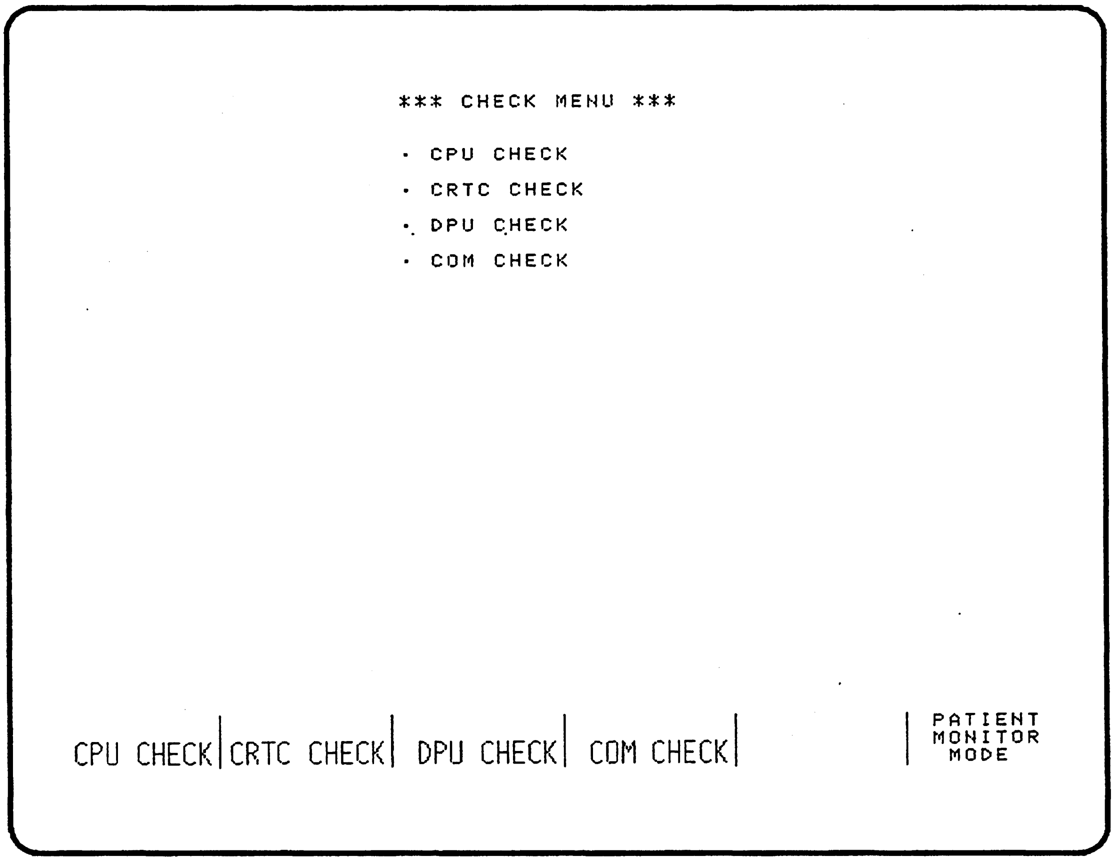
If an error is found, the date, time, code, board concerned and details are shown. Concerning the error code, refer to ERROR CODE (Section 5-3-2 & 3).

4-3-3 Patient Monitor Mode

When PATIENT MONITOR MODE is selected by pressing the “PATIENT MONITOR MODE” multifunction key, a normal operating display appears on the CRT.

4-3-4 Check Menu

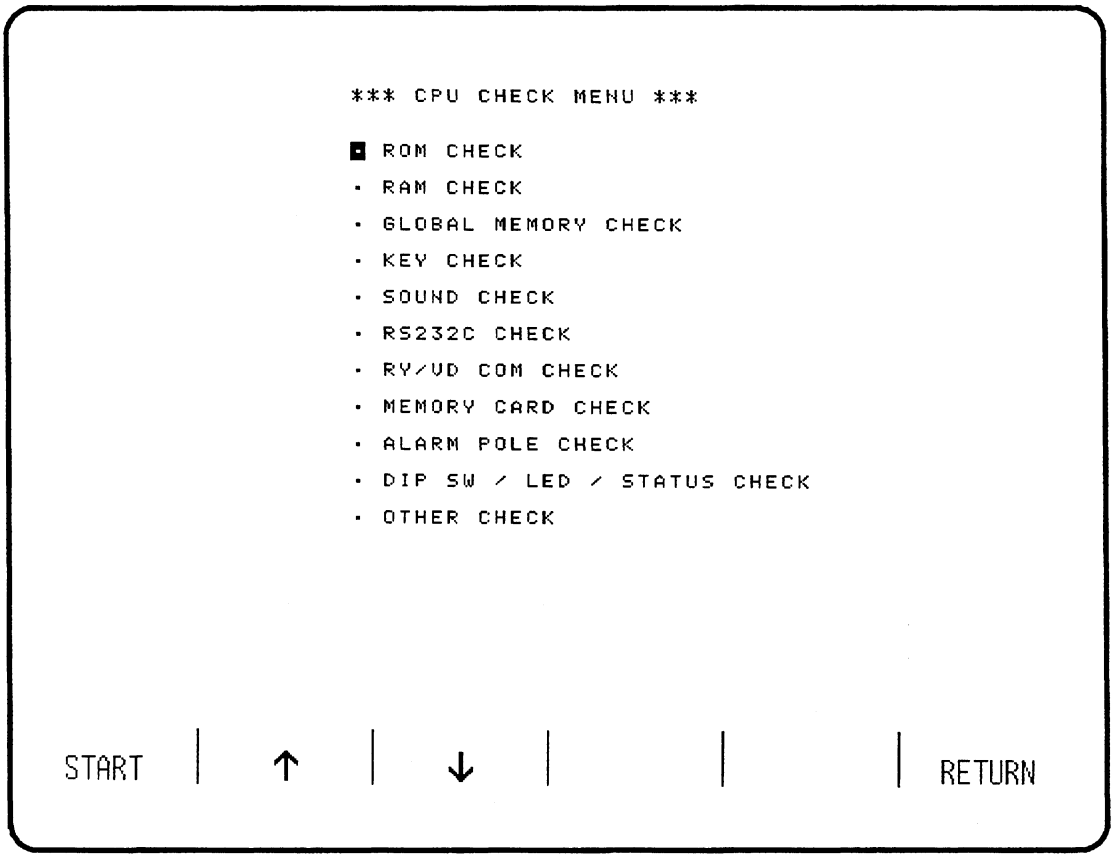
When MANUAL CHECK is selected by pressing the MANUAL CHECK key on the DIAGNOSTIC CHECK AND SYSTEM SETUP display, the display changes to the following display.


*** CHECK MENU ***
· CPU CHECK
· CRTC CHECK
· DPU CHECK
· COM CHECK
CPU CHECK
CRTC CHECK
DPU CHECK
COM CHECK
PATIENT MONITOR MODE

On the above display, the CPU, CRTC, DPU or COM board check can be selected by pressing the "CPU CHECK", "CRTC CHECK", "DPU CHECK" or "COM CHECK" multifunction key respectively.

◆ CPU (Central Processing Unit board) check

The following display appears on the CRT by first pressing the REVIEW key and then pressing the "CPU CHECK" multifunction key in the CHECK MENU display.



```
*** CPU CHECK MENU ***

■ ROM CHECK
· RAM CHECK
· GLOBAL MEMORY CHECK
· KEY CHECK
· SOUND CHECK
· RS232C CHECK
· RY/VD COM CHECK
· MEMORY CARD CHECK
· ALARM POLE CHECK
· DIP SW / LED / STATUS CHECK
· OTHER CHECK
```

On the above display,

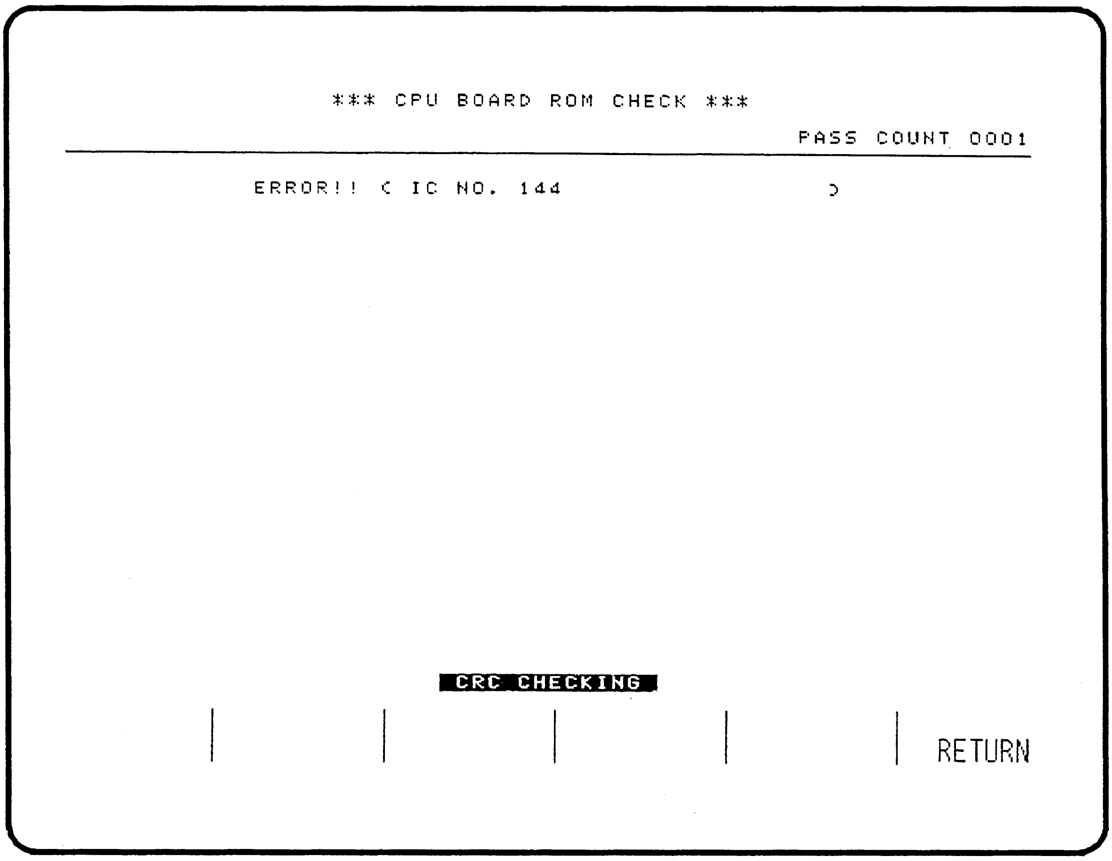
↑ ↓: to select a check item from the check items on the CRT

START: to execute the program for a selected check item while changing to the display for the check item

RETURN: to return to CHECK MENU display

- **ROM check**

  When ROM CHECK is selected, the display changes to the following display.



```
              *** CPU BOARD ROM CHECK ***
                                          PASS COUNT 0001
---------------------------------------------------------
        ERROR!! ( IC NO. 144                 )

                      CRC CHECKING
```

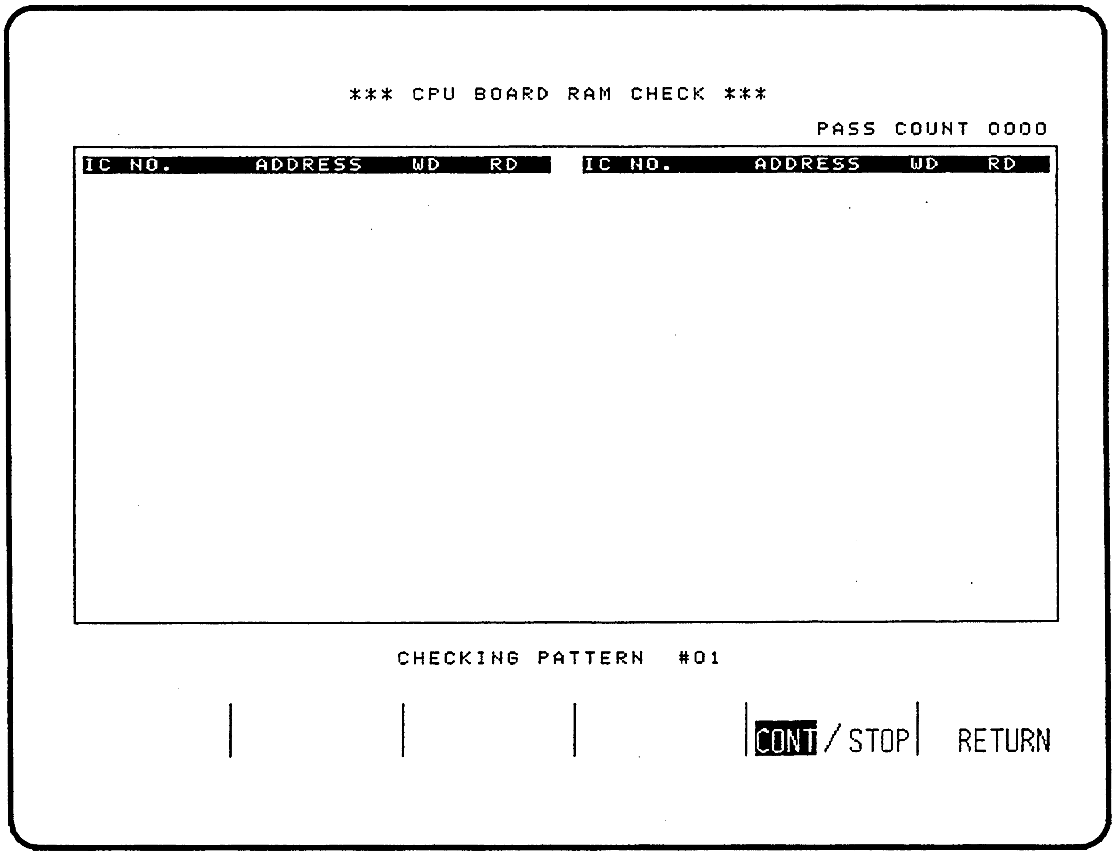
"CRC CHECKING" message is blinking while the check is executed with Cyclic Redundancy Check (C.R.C.). Whenever one cycle of the check is completed without an error, "PASS COUNT" increases by one. If there is an error, the error message appears on the display, as in the following example.

ERROR !! (IC No. 144, 146)

The check is stopped by pressing the "RETURN" multifunction key and the display returns to the CPU CHECK MENU.

- **RAM check**

  When RAM CHECK is selected, the display changes to the following display.



```
                 *** CPU BOARD RAM CHECK ***
                                              PASS COUNT 0000
IC NO.        ADDRESS    WD    RD    IC NO.        ADDRESS    WD    RD

                  CHECKING PATTERN  #01
```

“CHECKING PATTERN #XX” message blinks during the checking.
The check is executed by comparing each data after writing one of the following check patterns (No.1 to 15) into the memory area with the check pattern.

[TABLE - 1]

No.	PATTERN	No.	PATTERN
1	Decrement (BYTE)	9	Upper BYTE: FF, Lower BYTE: 00
2	55 (BYTE)	10	00 (BYTE)
3	0F (BYTE)	11	BIT SHIFT (WORD)
4	Alternating “00”H and “FF”	12	5555 (WORD)
5	Upper BYTE: 00, Lower BYTE: FF	13	AAAA (WORD)
6	AA (BYTE)	14	FFFF (WORD)
7	F0 (BYTE)	15	0000 (WORD)
8	Alternating “FF” and “00”		

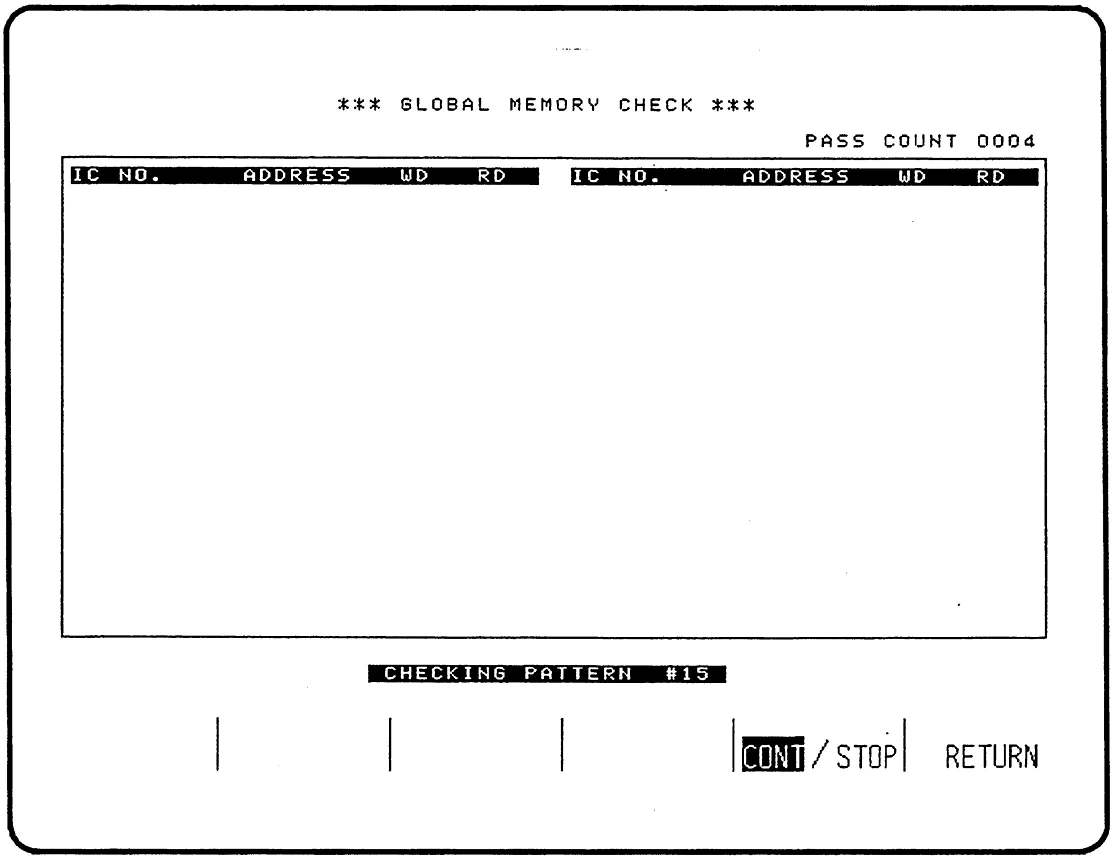
Whenever one cycle of the check patterns (No.1 to 15) is completed without an error, "PASS COUNT" increases by one. If there is an error, the error message appears on the display as in the following example.

IC Number	Address	WD	RD	
IC 152, 153	08A000	5555	FFFF	(WD: Data to be written) (RD: Data to be read)

The check is continued until the CONT/STOP mode on the display is set to STOP by pressing the "CONT/STOP" multifunction key.

The display returns to the CPU CHECK MENU by pressing the "RETURN" multifunction key.

- **Global Memory check**



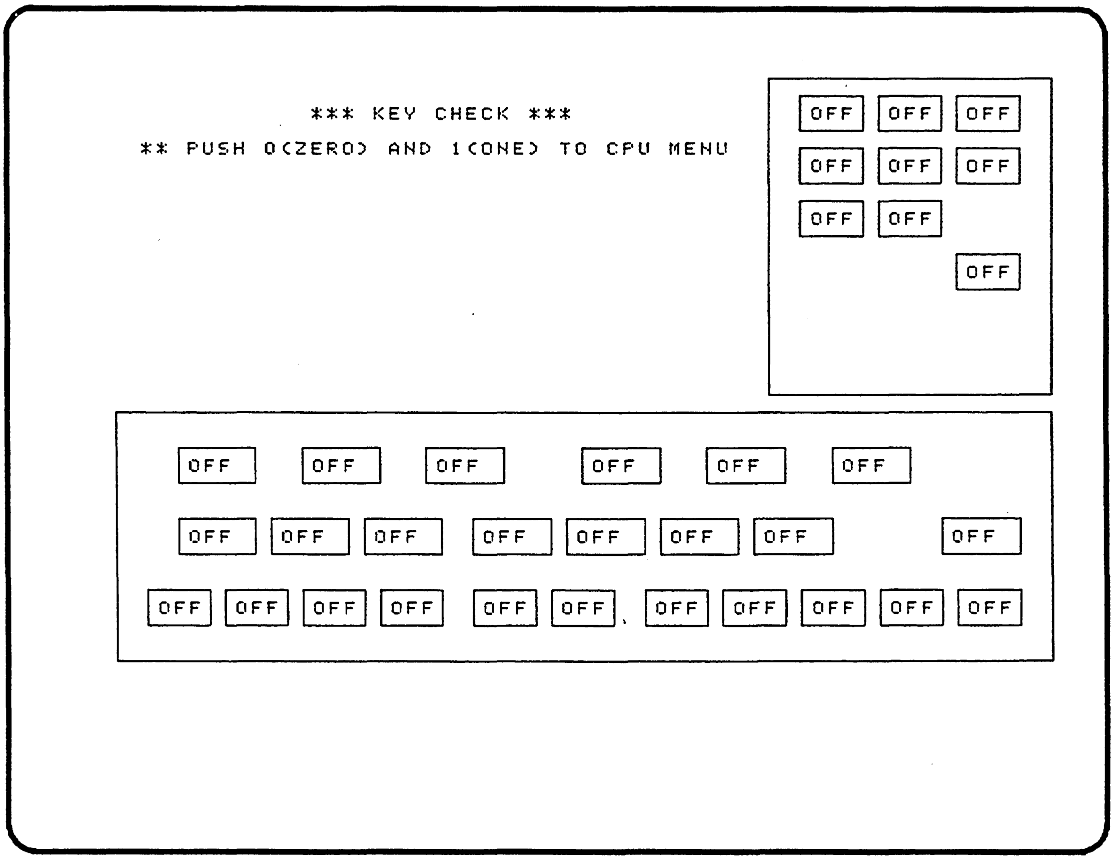
```
*** GLOBAL MEMORY CHECK ***
                                        PASS COUNT 0004
IC NO.      ADDRESS   WD    RD    IC NO.      ADDRESS   WD    RD

CHECKING PATTERN #15
```

The check contents are the same as the TABLE-1 of the RAM CHECK. The checking area is the global memory on the DPU board. When the global memory can not be accessed, the following message appears on the CRT.

"DPU BOARD NOT INSTALLED"

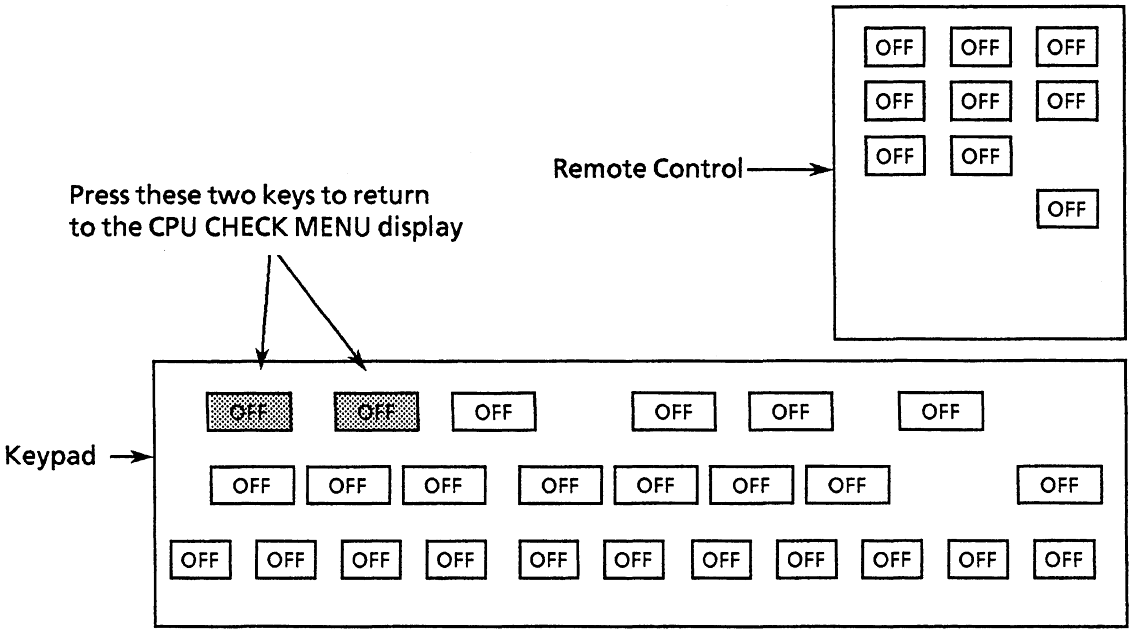
The check is continued until the CONT/STOP mode on the display is set to STOP by pressing the "CONT/STOP" multifunction key.

- **Key check**



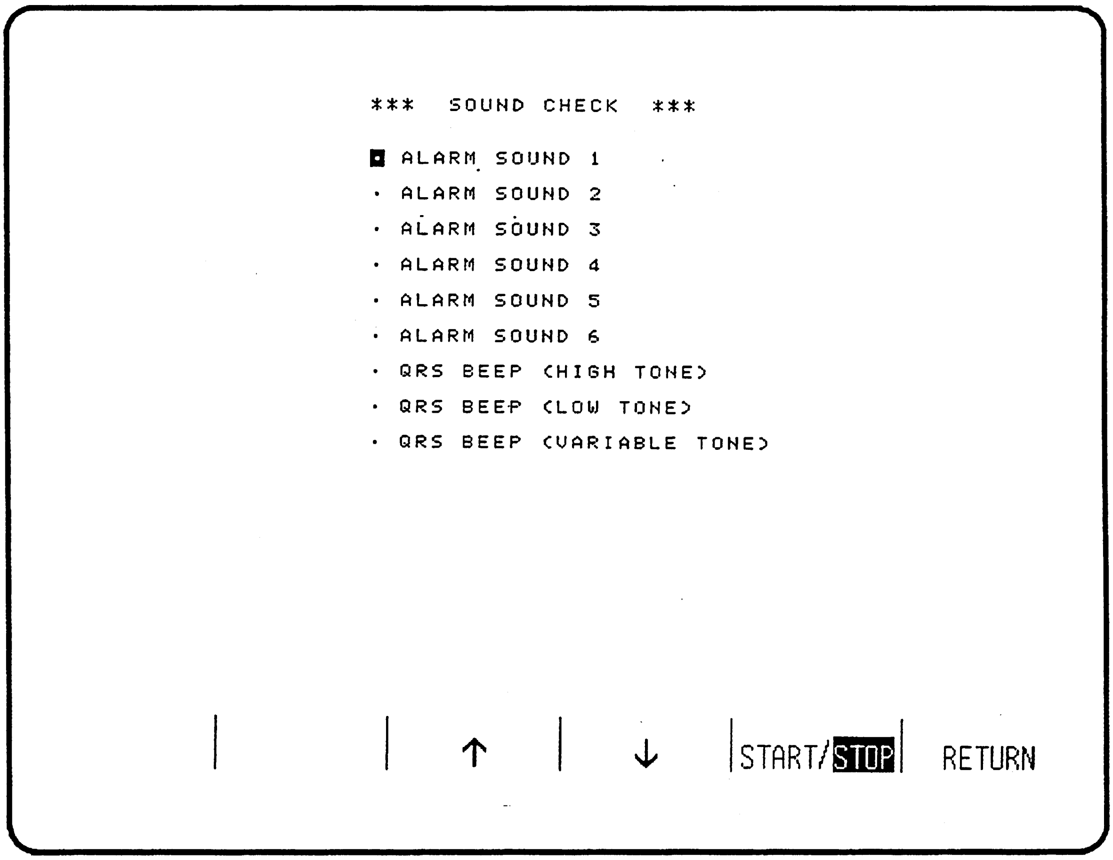
```
*** KEY CHECK ***
** PUSH 0(ZERO) AND 1(ONE) TO CPU MENU
```

"OFF" marks located according to keys on the keypad and the remote control appear on the screen. When a key switch is normal, the "OFF" mark concerned changes to a reverse lit "ON" while the key switch is pressed.
To return to the CPU CHECK MENU, press the shaded keys as shown below.



Remote Control
Press these two keys to return to the CPU CHECK MENU display
Keypad
OFF

- **Sound check**

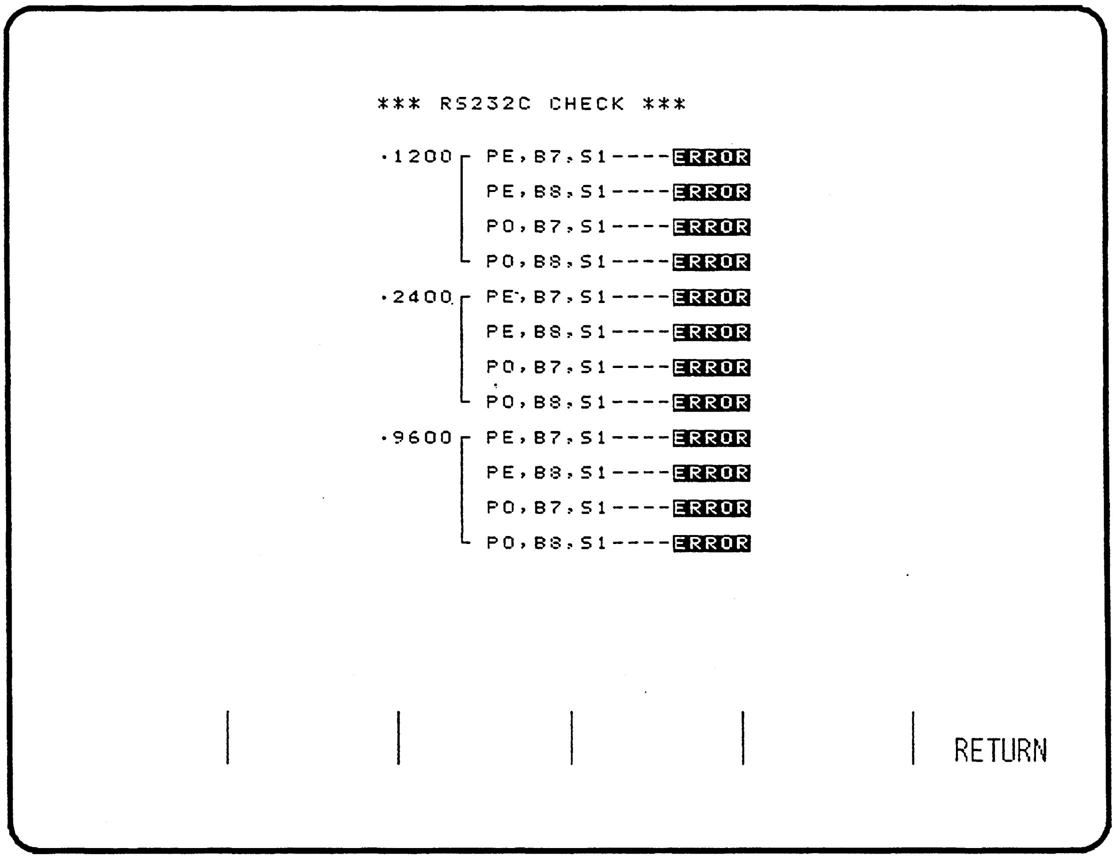


```
*** SOUND CHECK ***

■ ALARM SOUND 1
· ALARM SOUND 2
· ALARM SOUND 3
· ALARM SOUND 4
· ALARM SOUND 5
· ALARM SOUND 6
· QRS BEEP (HIGH TONE)
· QRS BEEP (LOW TONE)
· QRS BEEP (VARIABLE TONE)

|        |  ↑  |  ↓  |START/STOP|  RETURN
```

Each sound is generated by setting the START/STOP mode to START after selecting one of five check sounds on the display by pressing the " ↑ "or " ↓ " key.

SOUND MENU	TONE
ALARM SOUND 1	"Piro Piro"
ALARM SOUND 2	"Ping Pong"
ALARM SOUND 3	"Pon"
ALARM SOUND 4	"Pii Pii"
ALARM SOUND 5	"Pipi Pipi"
ALARM SOUND 6	"Pii"
QRS BEEP (High Tone)	"Pi" (High Beep)
QRS BEEP (Low Tone)	"Pock" (Low Beep), (Clack)
QRS BEEP (Variable Tone)	

- **RS232 check**



```
*** RS232C CHECK ***

·1200┌ PE,B7,S1----ERROR
     │ PE,B8,S1----ERROR
     │ PO,B7,S1----ERROR
     └ PO,B8,S1----ERROR
·2400┌ PE,B7,S1----ERROR
     │ PE,B8,S1----ERROR
     │ PO,B7,S1----ERROR
     └ PO,B8,S1----ERROR
·9600┌ PE,B7,S1----ERROR
     │ PE,B8,S1----ERROR
     │ PO,B7,S1----ERROR
     └ PO,B8,S1----ERROR
```

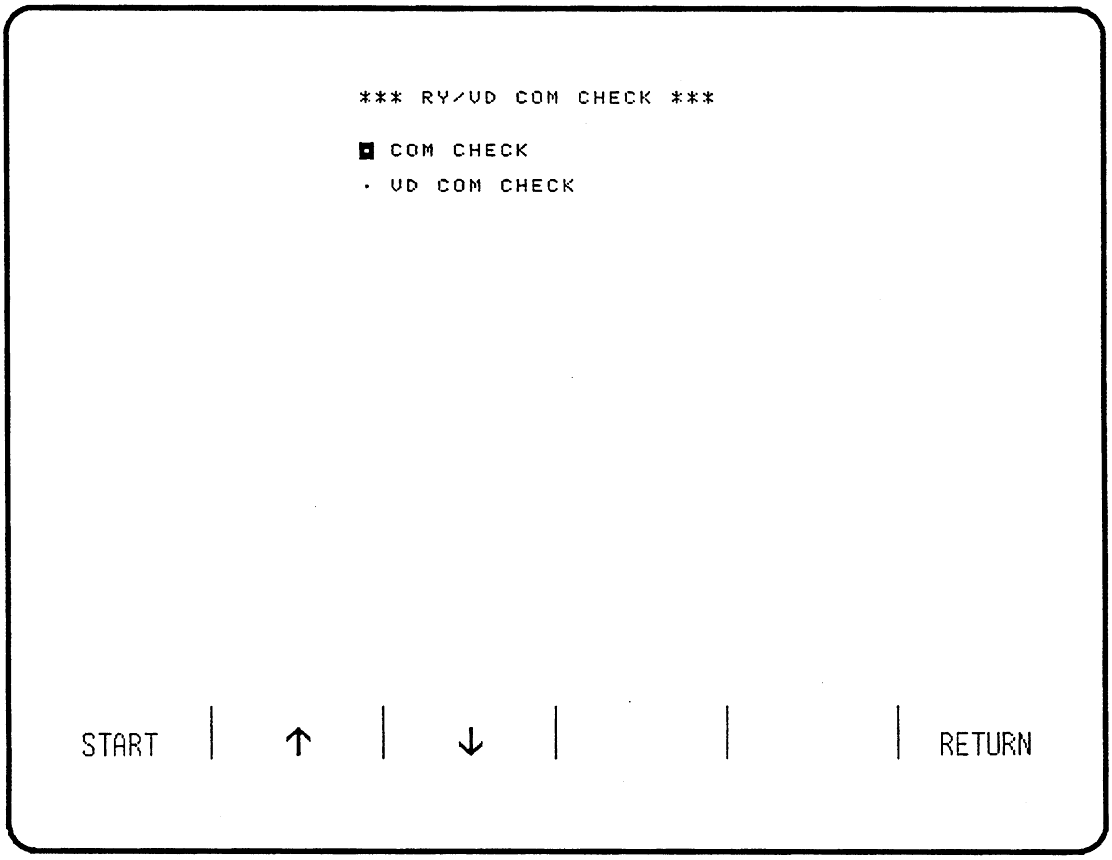
When the bedside monitor is not connected with external equipment which provides RS232C communication or when the following modification is not done to the receptacle for RS232C, the RS232C CHECK display appears with all the error indications on the CRT as in the above display.

[Modification]
pin 2 & 3: Short
Pin 4 & 5: Short
Pin 6 & 20: Short

1200, 2400, 9600: Baud rate (bits/sec.)

PE:	Even Parity
PO:	Odd Parity
B7:	7 Bits Data
B8:	8 Bits Data
S1:	1 Stop bit

- **RY/VD COM check**

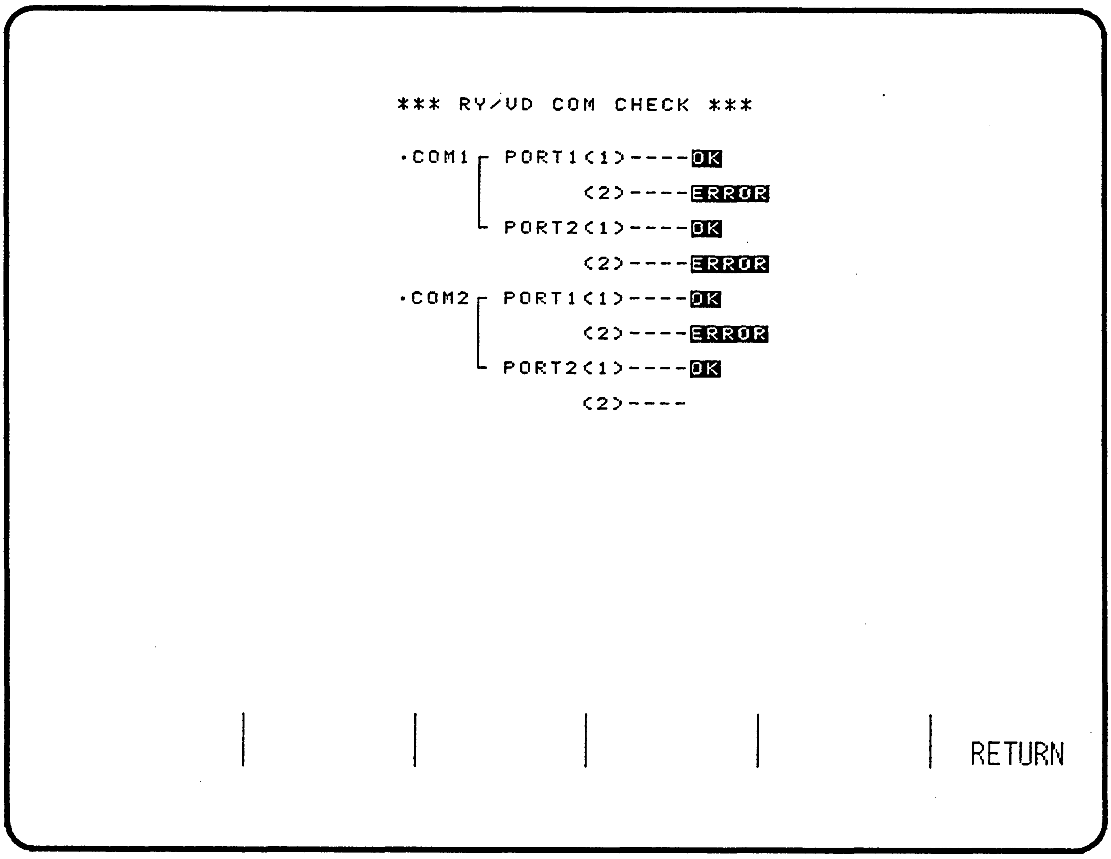


```
*** RY/VD COM CHECK ***

■ COM CHECK
· VD COM CHECK
```

This checks the communication between the bedside monitor main unit and the keypad (COM CHECK) or the video display unit (VD COM CHECK).

↑/↓: To selects the check items.
START: To starts the check.
RETURN: To return to CHECK MENU display.

COM Check



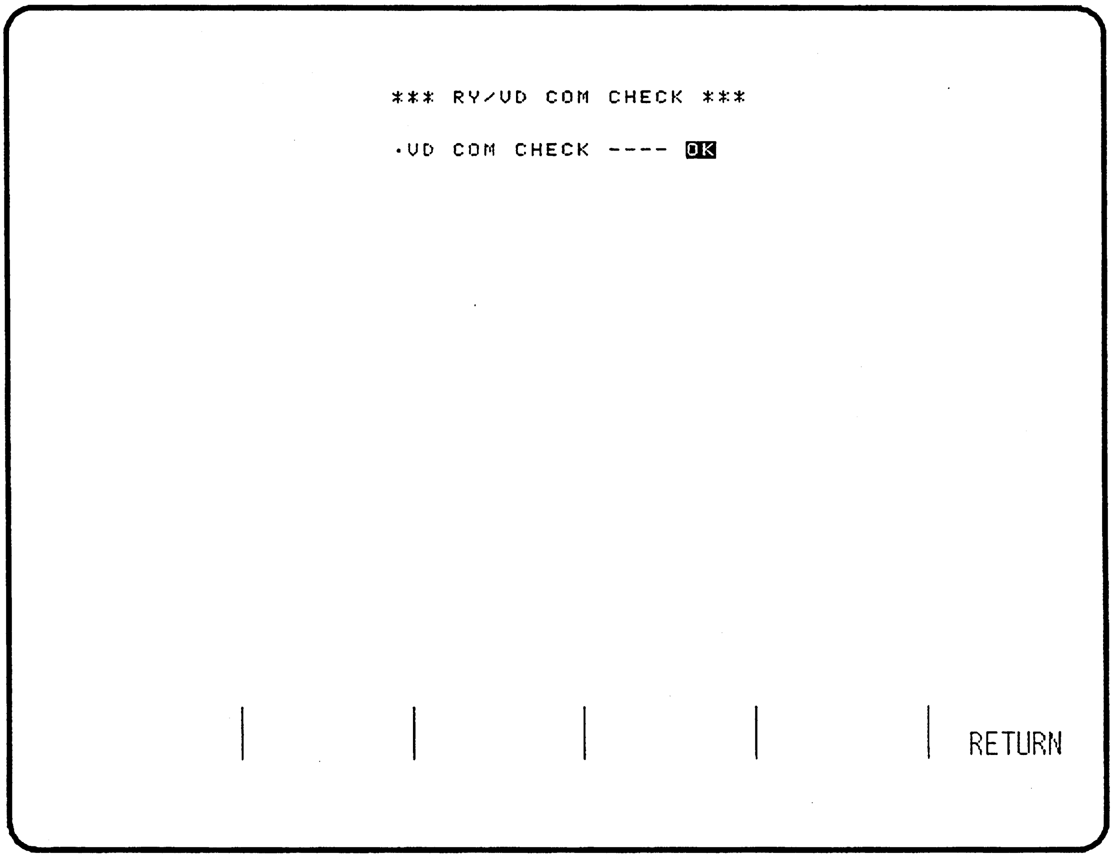
```
*** RY/UD COM CHECK ***

·COM1┌ PORT1<1>----OK
     │      <2>----ERROR
     └ PORT2<1>----OK
            <2>----ERROR
·COM2┌ PORT1<1>----OK
     │      <2>----ERROR
     └ PORT2<1>----OK
            <2>----
```

RETURN: To return to CHECK MENU display.

The table belowshows the communicating units and their pre–check run procedures (if, required)of the COM Check mode.

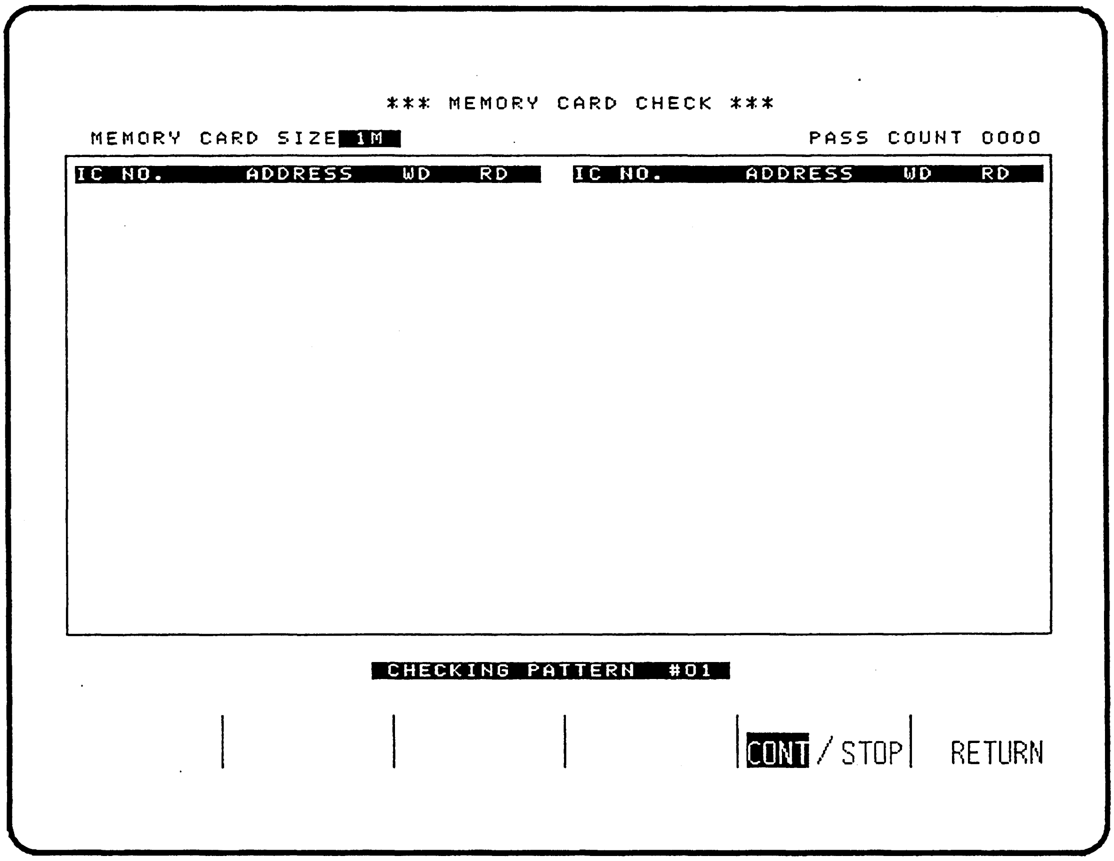
	PORT	COMMUNICATING UNIT	Pre–Check Run Procedures
COM1	PORT 1	Full-key board (Not used)	1) Not used 2) Not used
	PORT 2	Display unit	1) Not needed, IC's internal return loop check 2) Shot Pin No. 16 with Pin No. 17, and Pin No. 20 with Pin No21 of connector CN102 (UP-0795 Board)
COM2	PORT 1	Keypad (connected to display unit)	1) Not needed, IC's internal return loop check 2) Shot Pin No. 3 with Pin No. 4 of connector CN106 (UP-0801 Board)
	PORT 2	Keypad (connected to main unit)	1) Not needed, IC's internal return loop check 2) Shot Pin No. 3 with Pin No. 4 of connector CN104 (UP-0807 Board)

VD check



```
*** RY/VD COM CHECK ***

·VD COM CHECK ---- OK
```

- **MEMORY CARD Check**



```
                 *** MEMORY CARD CHECK ***
MEMORY CARD SIZE 1M                           PASS COUNT 0000
IC NO.      ADDRESS   WD   RD    IC NO.      ADDRESS   WD   RD

                  CHECKING PATTERN  #01

          |        |        |      |CONT/STOP|  RETURN
```

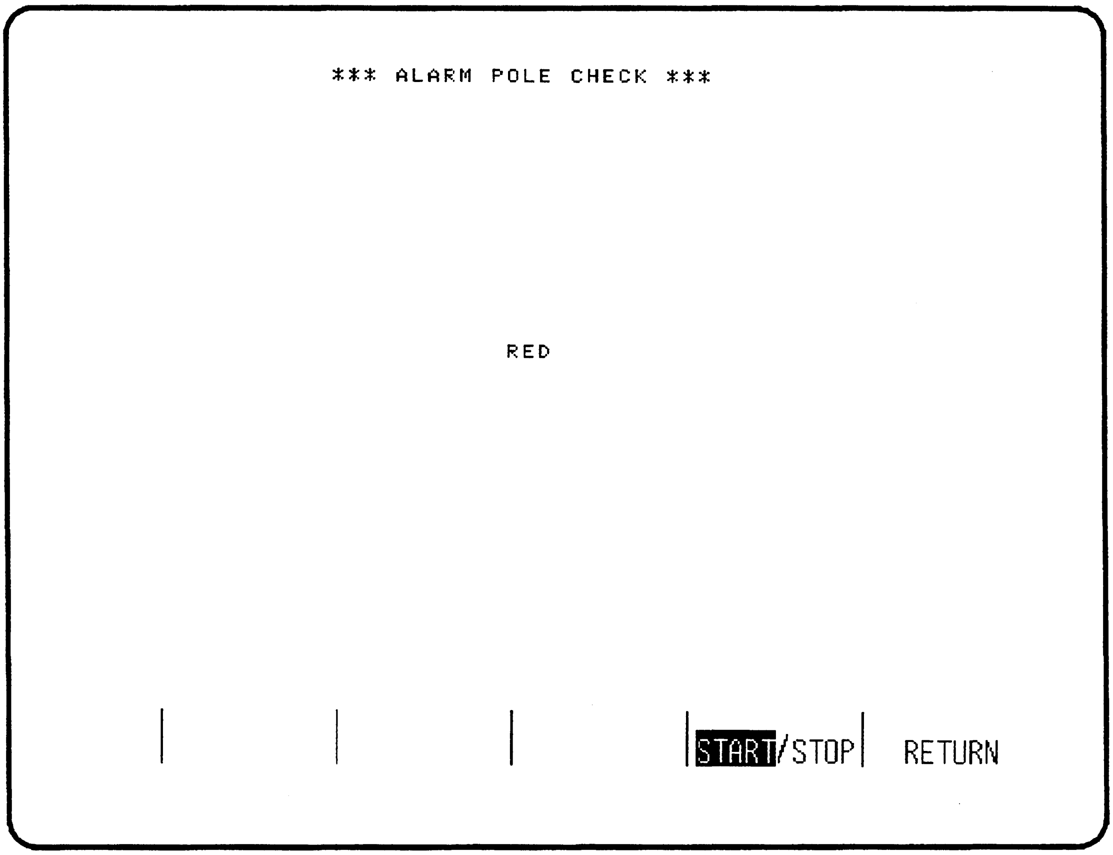
When the check mode is running "CHECKING PATTERN #01 " message blinks. If the MEMORY CARD is not inserted, the "MEMORY CARD NOT INSERTED" message is displayed. The "LOW BATTERY" message appears when the battery power of the memory card is low. The "WRITE PROTECT ERROR" message appears when data are written into a write protected memory card.

Checking pattern
The table below shows the 4 checking patterns.

No.	PATTERN	
1	Decrement	(BYTE)
2	5555	(WORD)
3	AAAA	(WORD)
4	FFFF	(WORD)

In the MEMORY CARD check, the checking pattern #1 to 4 are continuously written and read. To stop this, press the "STOP" multifunction key.

- **ALARM POLE Check**



*** ALARM POLE CHECK ***

RED

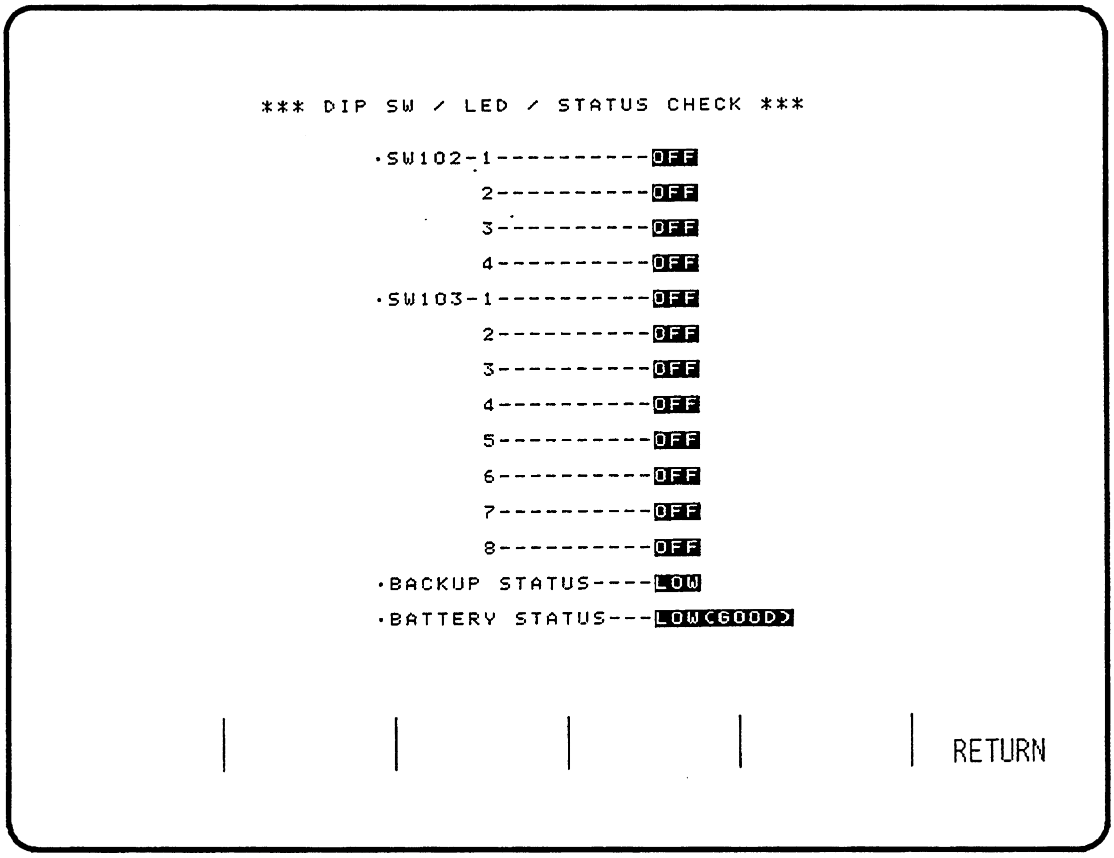
When the check mode is running the following messages appear repeatively.
RED → YELLOW → GREEN → RED → ...
At the same time the alarm pole flashes the above corresponding colors.

On the above display,
START/STOP: to start or stop this check program.

RETURN: to return to the CHECK MENU display.

The following sections are displayed by first pressing the REVIEW key and then "CPU CHECK" multifunction key on the DIAGNOSTIC CHECK AND SYSTEM SETUP display. These sections are for your reference since these check programs are for product inspection at the factory.

- **DIP SW / LED / STATUS check**

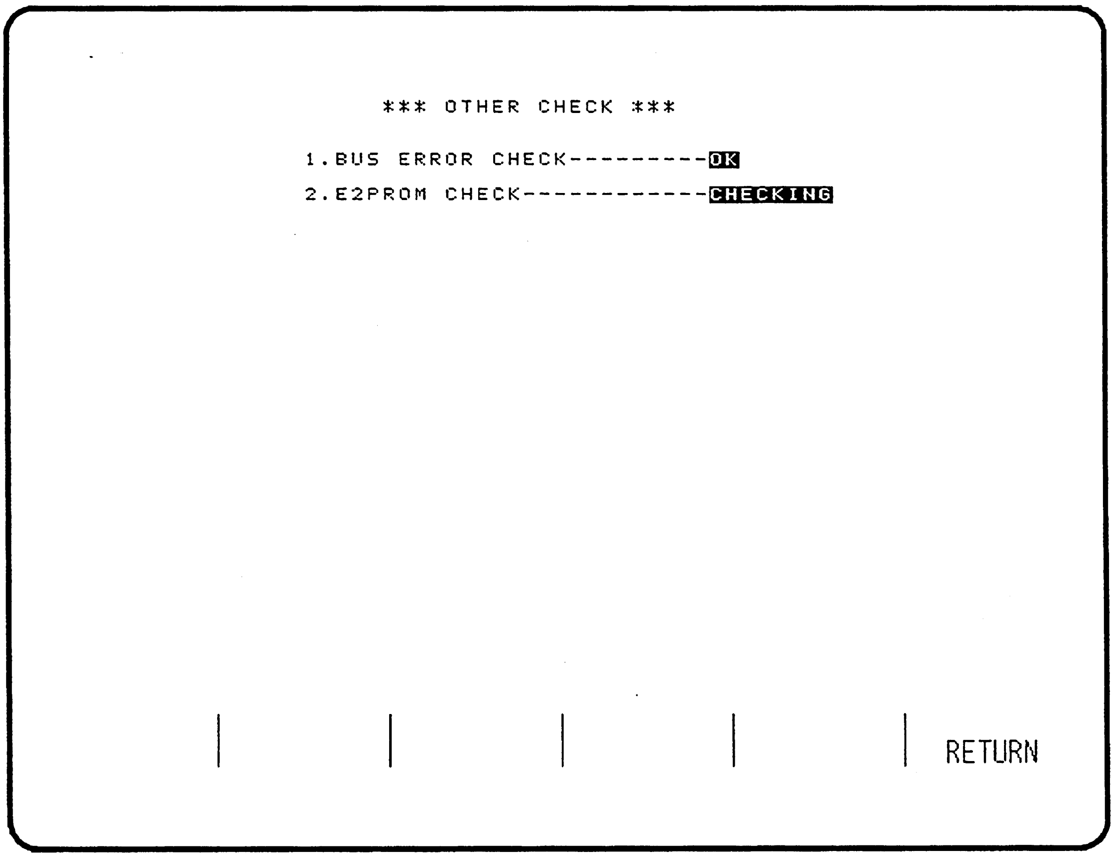


```
*** DIP SW / LED / STATUS CHECK ***

        •SW102-1----------OFF
               2----------OFF
               3----------OFF
               4----------OFF
        •SW103-1----------OFF
               2----------OFF
               3----------OFF
               4----------OFF
               5----------OFF
               6----------OFF
               7----------OFF
               8----------OFF
        •BACKUP STATUS----LOW
        •BATTERY STATUS---LOW(GOOD)
```

1) DIP SWITCH check
   The set condition of the dip switch on the CPU board, SW102 and SW103, appears on the CRT.
2) LED check
   Each LED (8 bits) on the CPU board sequentially lights and goes out one after another.
3) STATUS check
   "Backup Status" and "Battery Status" appear on the CRT as follows:

[Backup Status]		[Battery Status]	
Low:	Normal condition	Low:	Normal condition
High:	Super-capacitor must be charged	High:	Lithium battery must be replaced

- **Other Check**



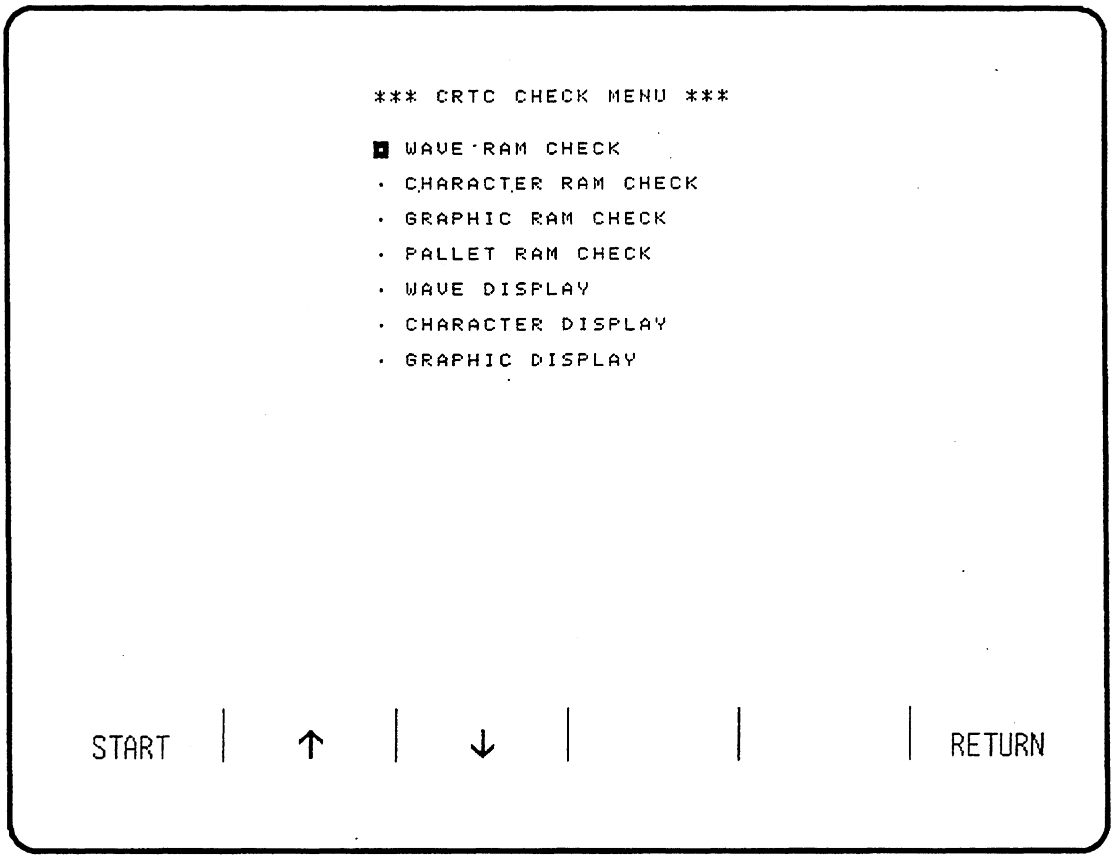
```
*** OTHER CHECK ***

1.BUS ERROR CHECK---------OK
2.E2PROM CHECK------------CHECKING
```

"CHECKING " message blinks during the checking.

1) BUS ERROR check
   The check is executed by accessing an address at which memory area does not exist. A detection of a bus error signal is confirmed by indicating "OK."
2) EEPROM check
   The check is executed by comparing each byte after being written into the EEPROM with check byte "55"H to be written. All data of EEPROM are stacked before "55" is written.

◆CRTC (CRT Control board) Check

When CRTC CHECK is selected by pressing the CRTC CHECK key on the CHECK MENU display, the following CRTC CHECK MENU appears on the display unit.

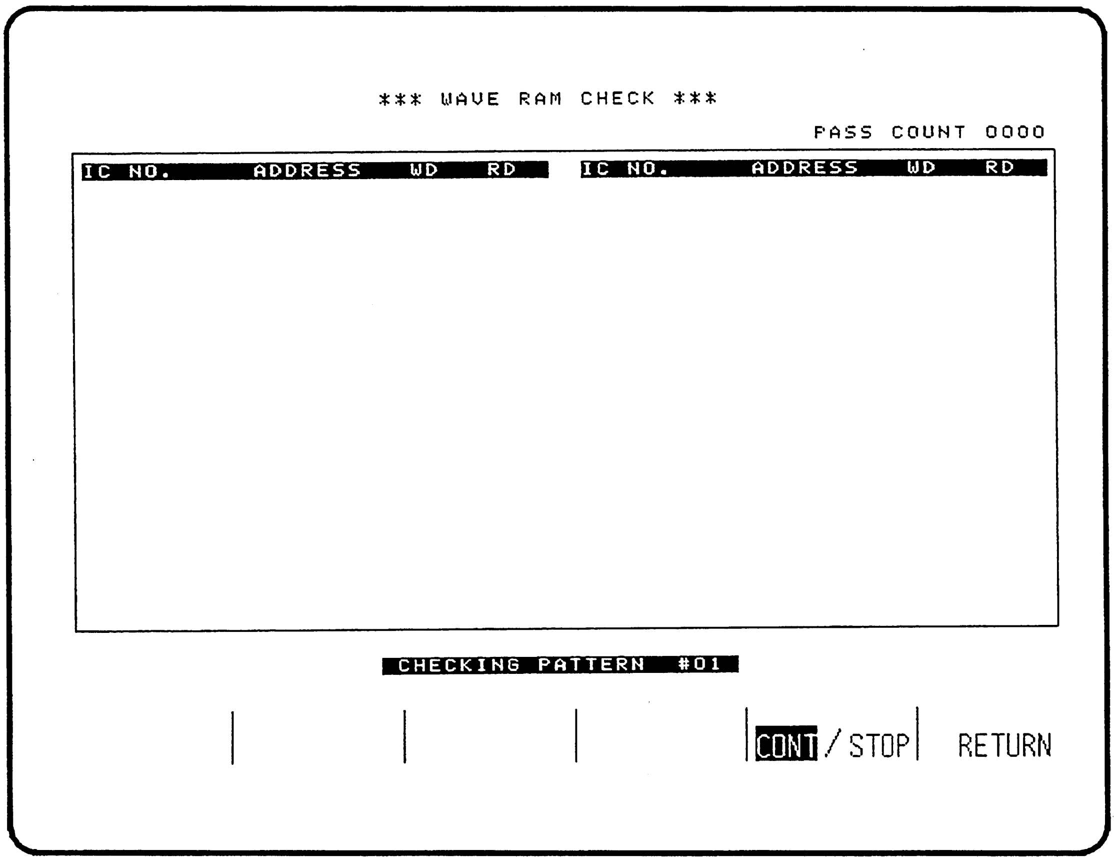

*** CRTC CHECK MENU ***
■ WAVE RAM CHECK
· CHARACTER RAM CHECK
· GRAPHIC RAM CHECK
· PALLET RAM CHECK
· WAVE DISPLAY
· CHARACTER DISPLAY
· GRAPHIC DISPLAY
START
↑
↓
RETURN

On the above display,

↑ ↓:	to select a check item from the check items on the CRT
START:	to execute the program for a selected check item while changing to the display for the check item
RETURN:	to return to the CHECK MENU display

- **WAVE RAM check**

  When RAM CHECK is selected, the display changes to the following display.



```
*** WAVE RAM CHECK ***
                                                  PASS COUNT 0000
IC NO.    ADDRESS    WD    RD      IC NO.    ADDRESS    WD    RD



                       CHECKING PATTERN #01
```

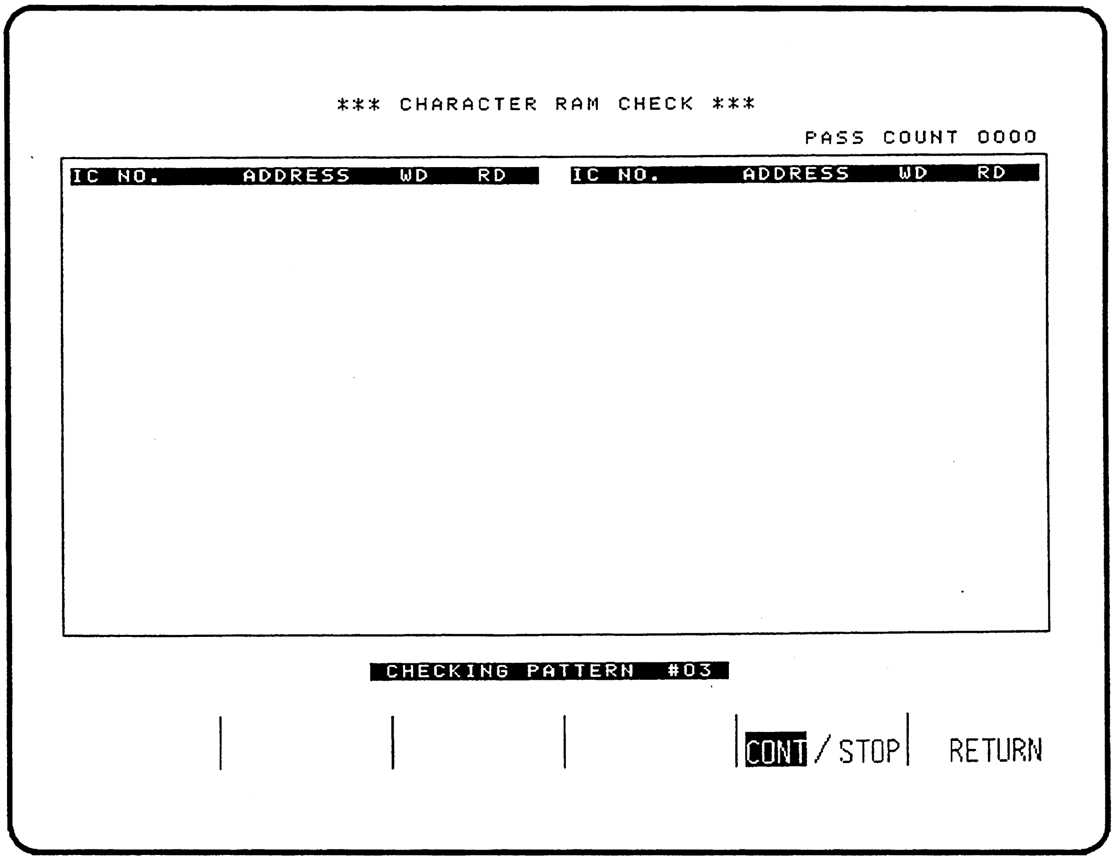
"CHECKING PATTERN #XX" message blinks during the checking.
The check is executed by comparing each data after writing one of the following check patterns (No.1 to 4) into the memory area with the check pattern.

[TABLE - 2]

No.	PATTERN	
1	AAAA	(WORD)
2	5555	(WORD)
3	FFFF	(WORD)
4	0000	(WORD)

- **CHARACTER RAM check**

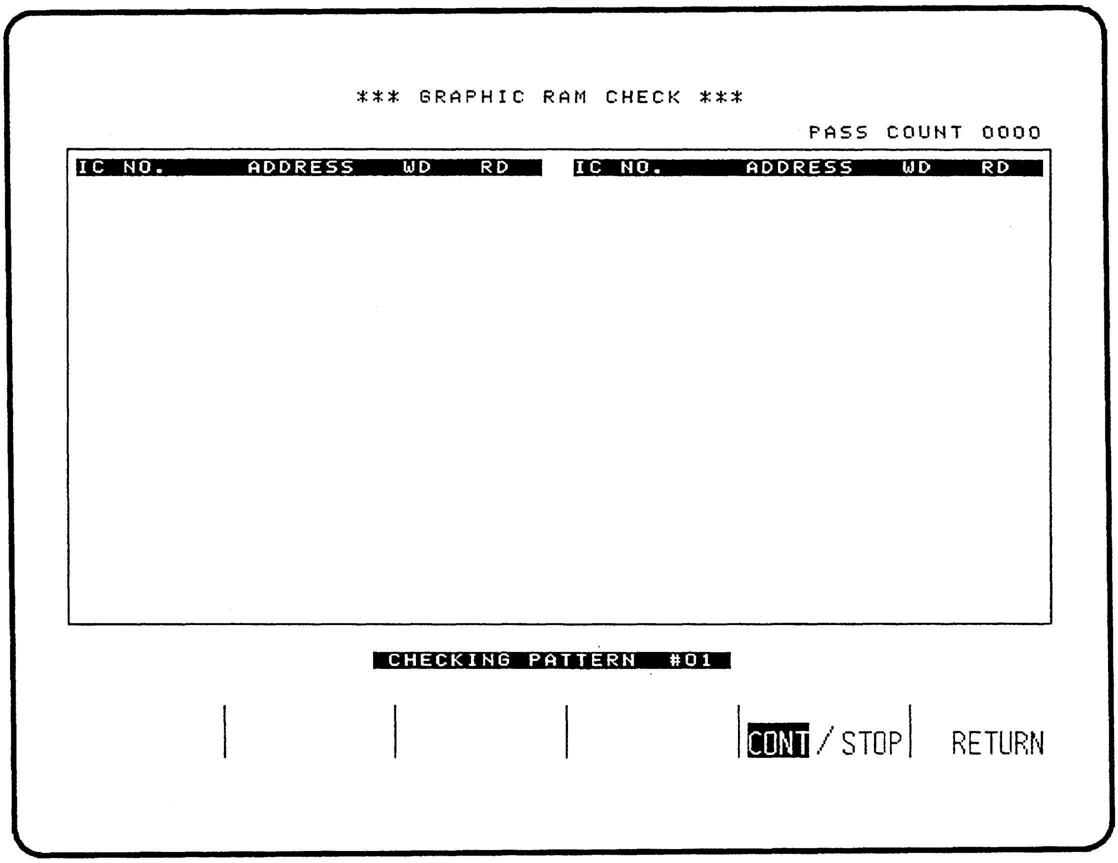
  Pattern No. 1 to 4 of Table-2 are used as the check pattern. The check is the same as the WAVE RAM CHECK on the CRTC board.



```
                    *** CHARACTER RAM CHECK ***
                                              PASS COUNT 0000
IC NO.       ADDRESS    WD    RD     IC NO.       ADDRESS    WD    RD









                     CHECKING PATTERN  #03
```

- **GRAPHIC RAM check**

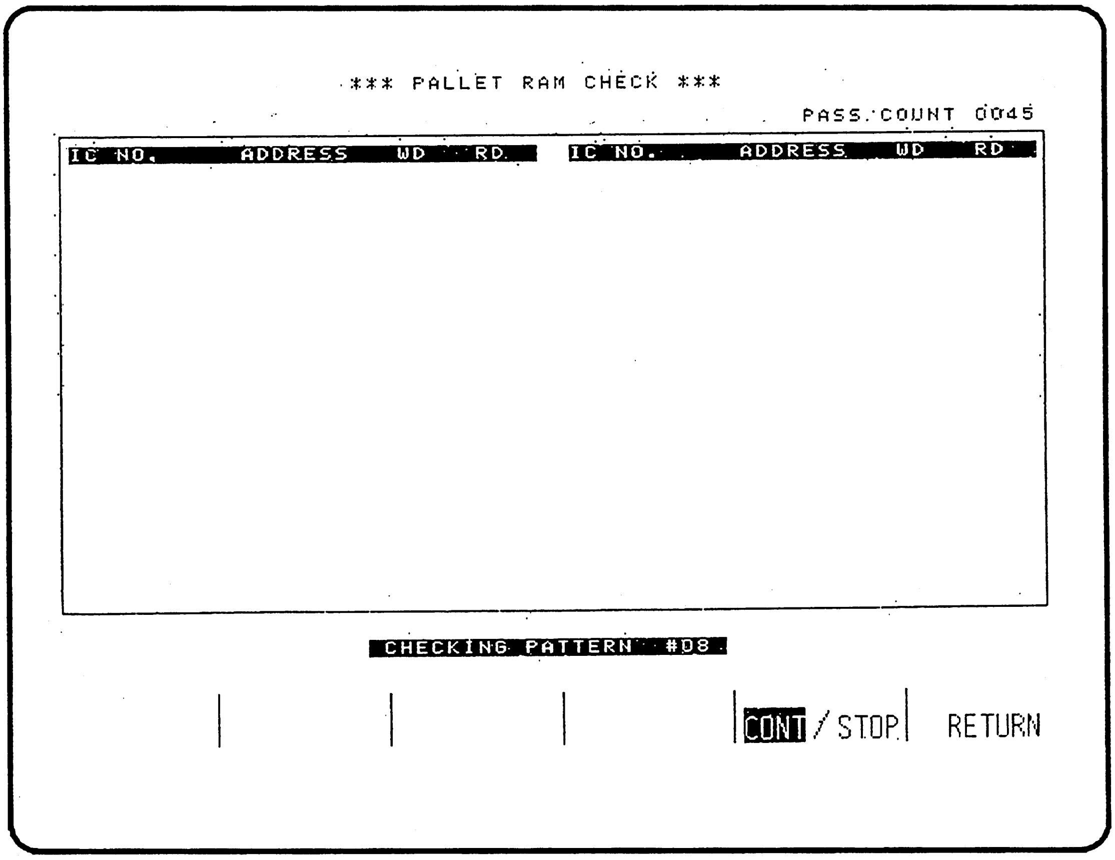
  The check is the same as the CHARACTER RAM CHECK.



```
                     *** GRAPHIC RAM CHECK ***
                                                   PASS COUNT 0000
IC NO.        ADDRESS    WD    RD    IC NO.        ADDRESS    WD    RD

                      CHECKING PATTERN  #01
```

- **PALETTE RAM check**

  Pattern No.1 ~ 4 of Table -3 are used as the check pattern. The check is the same as the WAVE RAM CHECK on the CRTC board.



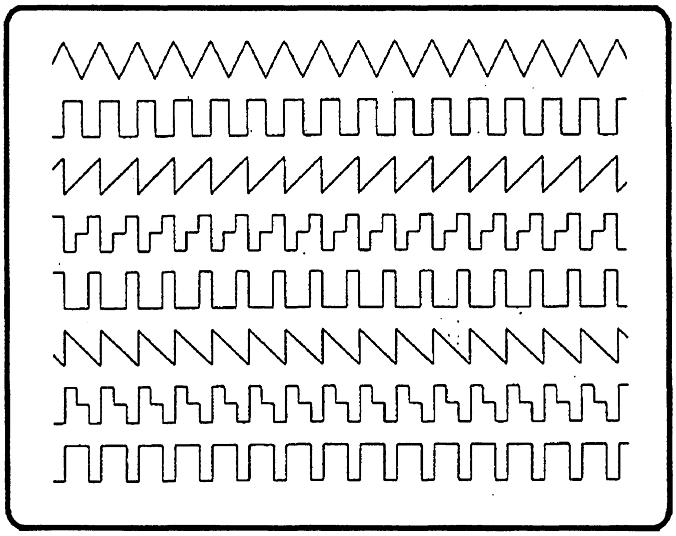
```
*** PALLET RAM CHECK ***
                                         PASS COUNT 0045
IC NO.   ADDRESS   WD   RD     IC NO.   ADDRESS   WD   RD

CHECKING PATTERN #08
```

[TABLE - 3]

No.	PATTERN	
1	2A	(Byte)
2	15	(Byte)
3	3F	(Byte)
4	00	(Byte)

- **WAVE Display check**

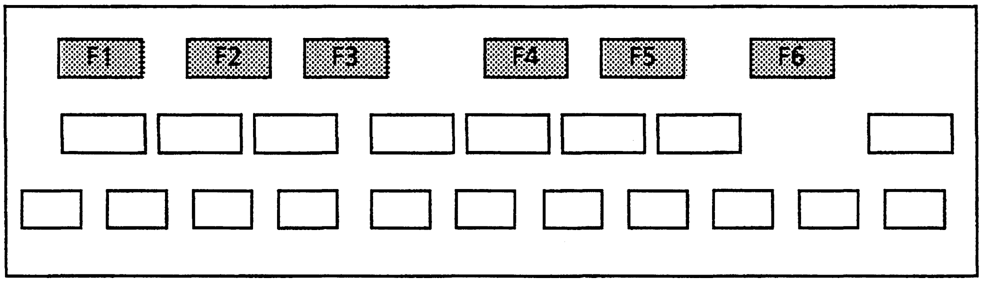
  8 traces of sweeping waveform appear on the display unit screen.



The following shaded keys on the keypad operate this check mode.

NOTE

To avoid confusion, the shaded keys are named from F1 ~ F6.

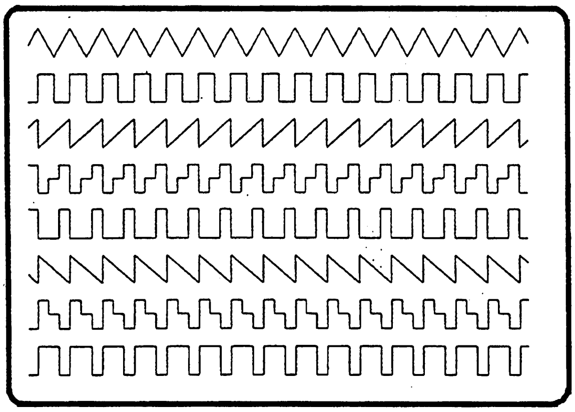


The Table-4 below shows the function of each shaded keys in this check mode.

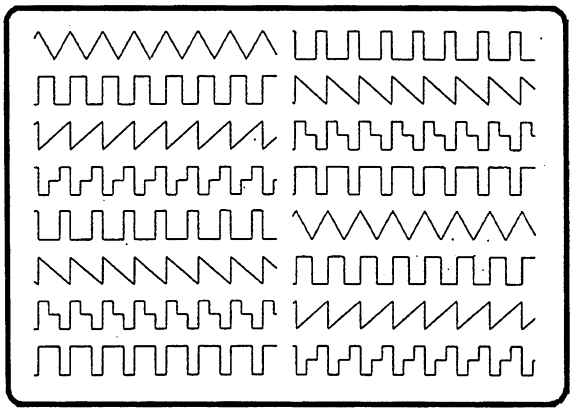
[TABLE - 4]

Key	Function
F1	Changes the wave display screen.
F2	Switches ON/OFF the trace waveform one by one.
F3	Sweeping /freezing the trace waveform.
F4	Changes the color of the trace waveform (only available when the wave display screen shows t8 traces of waveform).
F5	Not used.
F6	To return to the CRTC CHECK MENU

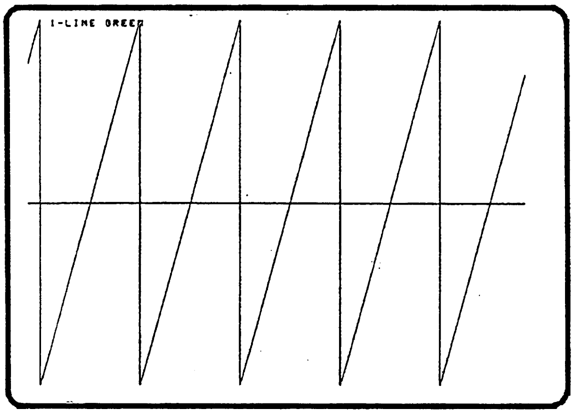
The wave display screen changes when the F1 key is pressed repeatedly.



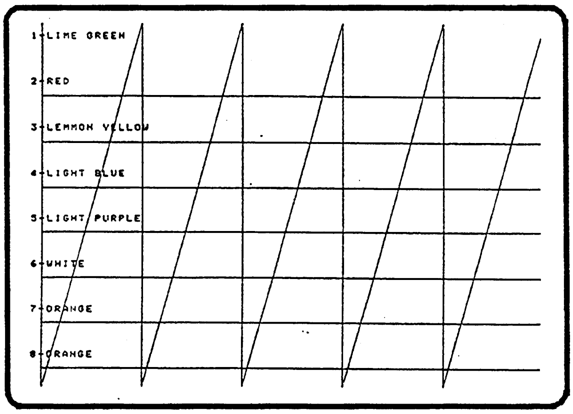
8 traces of waveform



16 traces of waveform

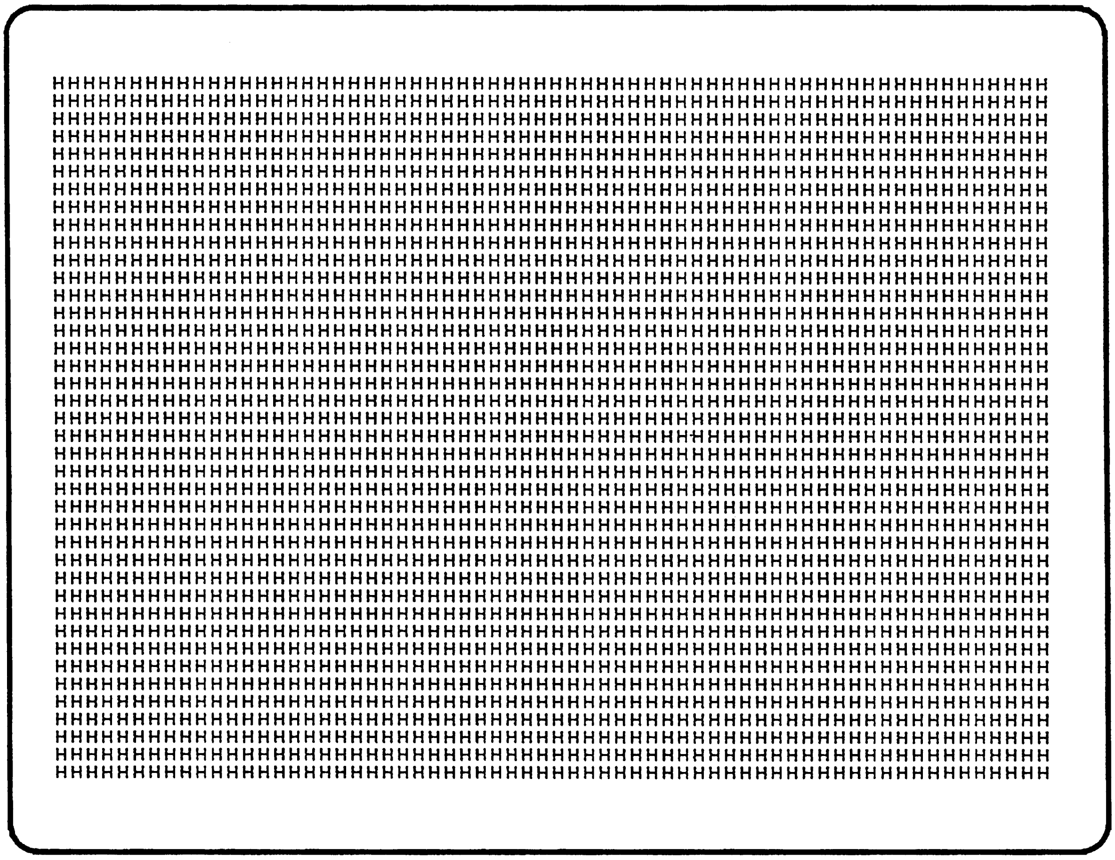

1-LIME GREEN

1 trace of sawtooth waveform with full amplitude and trace line


1 LIME GREEN
2 RED
3 LEMMON YELLOW
4 LIGHT BLUE
5 LIGHT PURPLE
6 WHITE
7 ORANGE
8 ORANGE

1 trace of sawtooth waveform with full amplitude and 7 trace lines

- **CHARACTER DISPLAY check**
  The following CHARACTER DISPLAY appears on the display unit screen.



```
HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
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HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
```
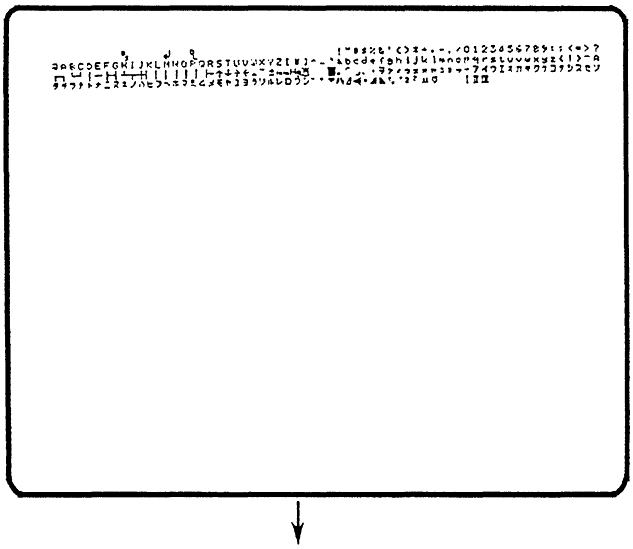
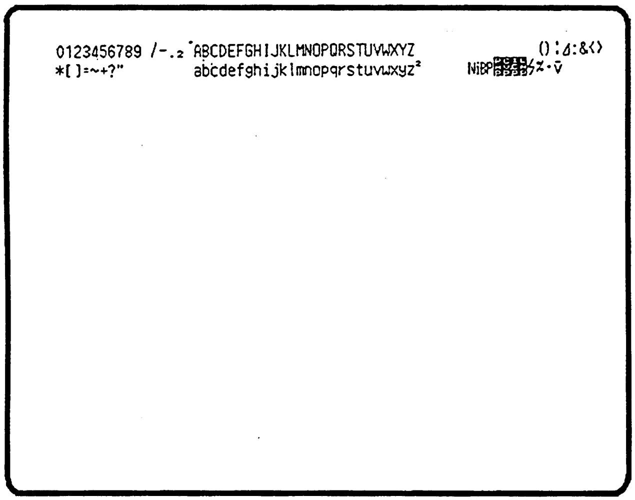

By pressing F2 key repeatedly, the display mode changes as follows:

1) Normal
2) Reversed light
3) Reversed blink

By pressing the F1 key repeatedly, the character pattern changes as follows:

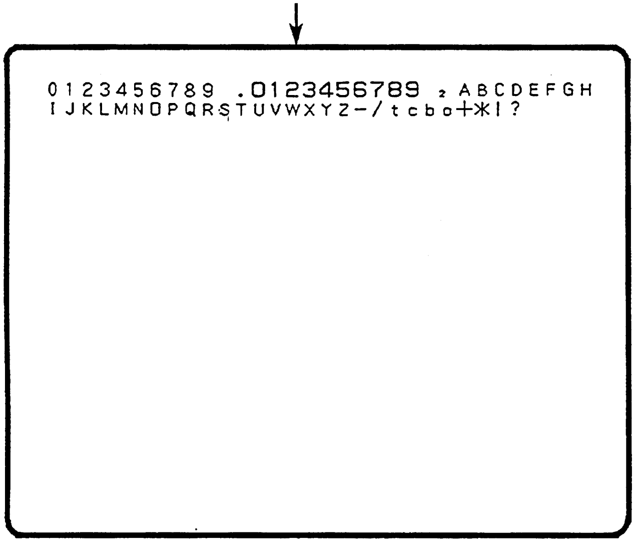


This display appears when the F1 key is pressed for the fifteenth times.



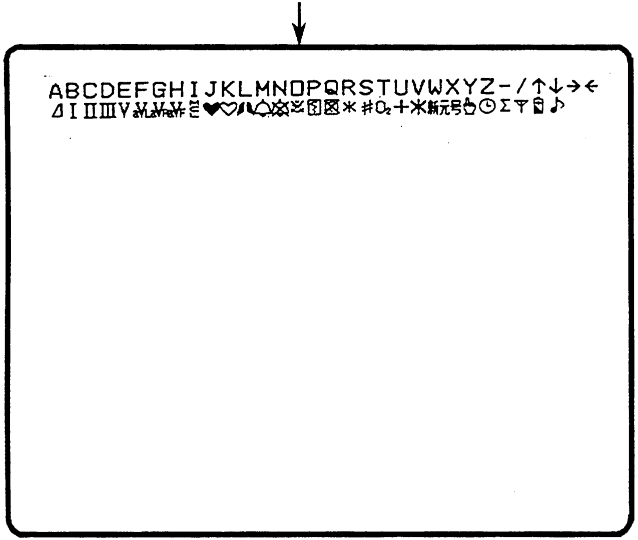
```
0123456789 /-.₂ ABCDEFGHIJKLMNOPQRSTUVWXYZ          ():Δ:&<>
*[]=~+?"        abcdefghijklmnopqrstuvwxyz²    NiBP    ⁄%·V̄
```

This display appears when the F1 key is pressed for the sixteenth times.
By pressing the F1 key from the seventeenth, the Japanese character display appears.



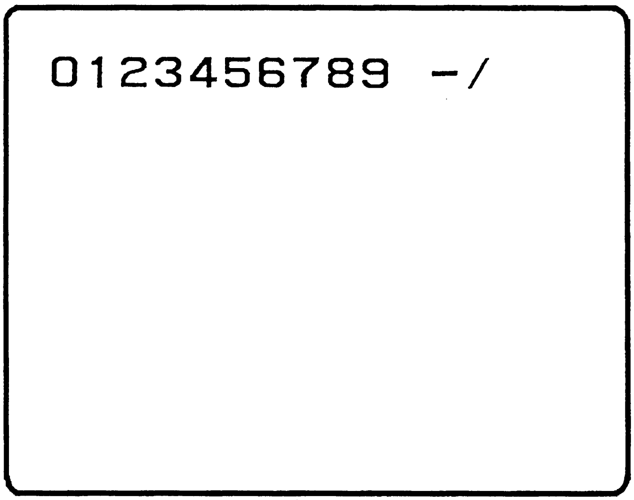
```
0123456789 .0123456789 ₂ABCDEFGH
IJKLMNOPQRSTUVWXYZ-/tcbo+✱|?
```

This display appears when the F1 key is pressed for the eighteenth times.
By pressing the F1 key from the nineteenth to the twenty-second times, the Japanese character displays appear.



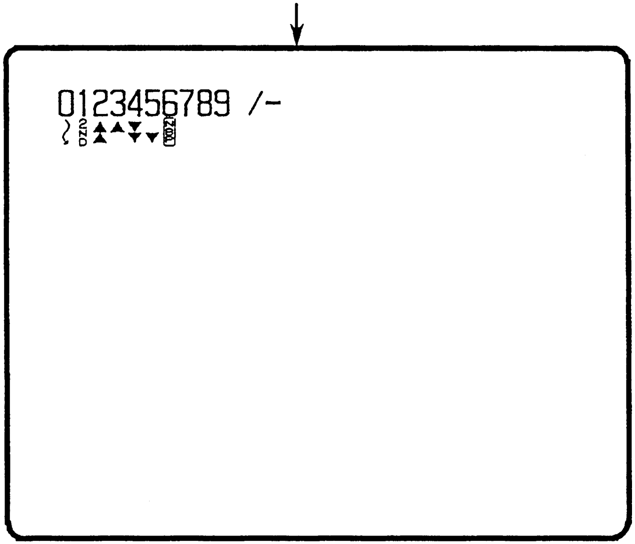
```
ABCDEFGHIJKLMNOPQRSTUVWXYZ-/↑↓→←
ΔIⅡⅢV    ♥♡       *#O₂+✱新元号 ⊙ΣΥ ♪
```

This display appears when the F1 key is pressed for the twenty-third times.



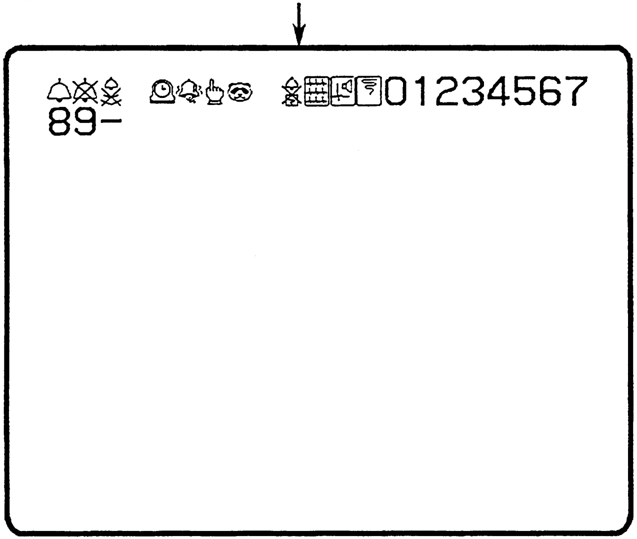
0123456789 -/

This display appears when the F1 key is pressed for the twenty-fourth times.



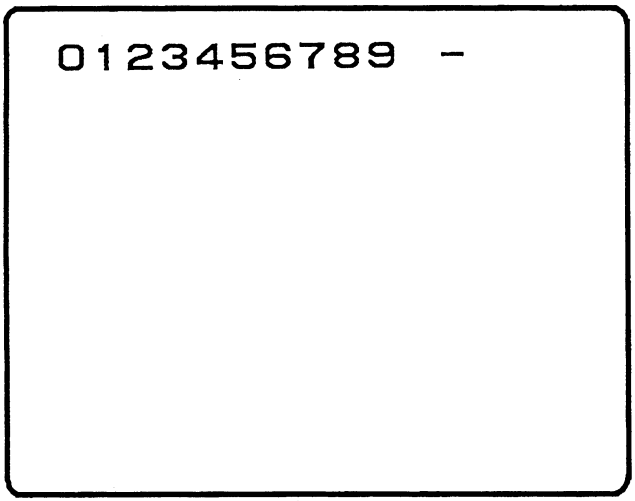
0123456789 /-

This display appears when the F1 key is pressed for the twenty-fifth times.

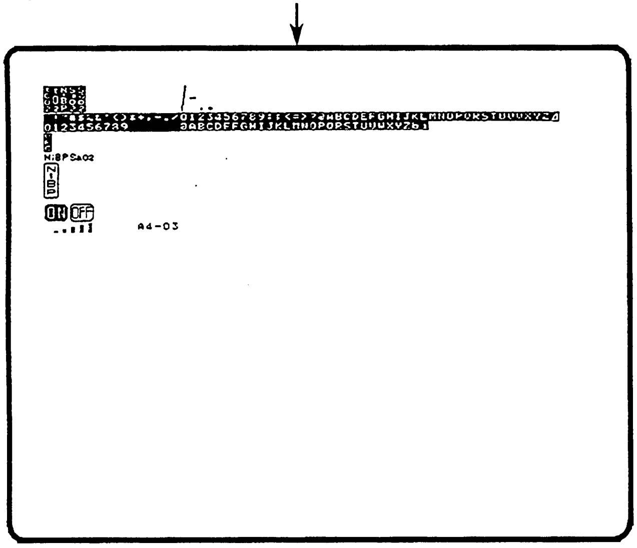


01234567
89-

This display appears when the F1 key is pressed for the twenty-sixth times.
By pressing the F1 key from the twenty-seventh and twenty-eight times, the Japanese character displays appear.


0123456789 -

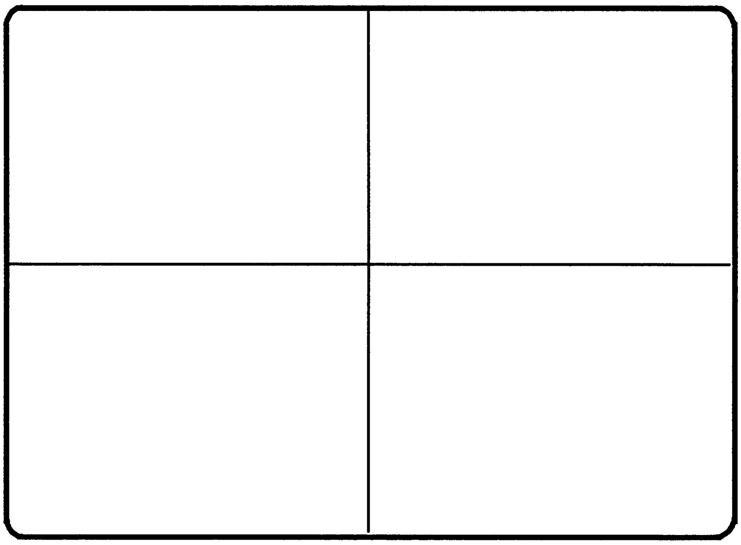
This display appears when the F1 key is pressed for the twenty-ninth times.


0123456789
N:BPSA02
ON
OFF
A4-03

This display appears when the F1 key is pressed for the thirtieth times. This is the last of the character display screen. When the the F1 key is pressed for the thirty-first times, the display screen returns back to the display shown on page 4.32.

- **GRAPHIC DISPLAY check**

The following graphic display appears on the CRT.

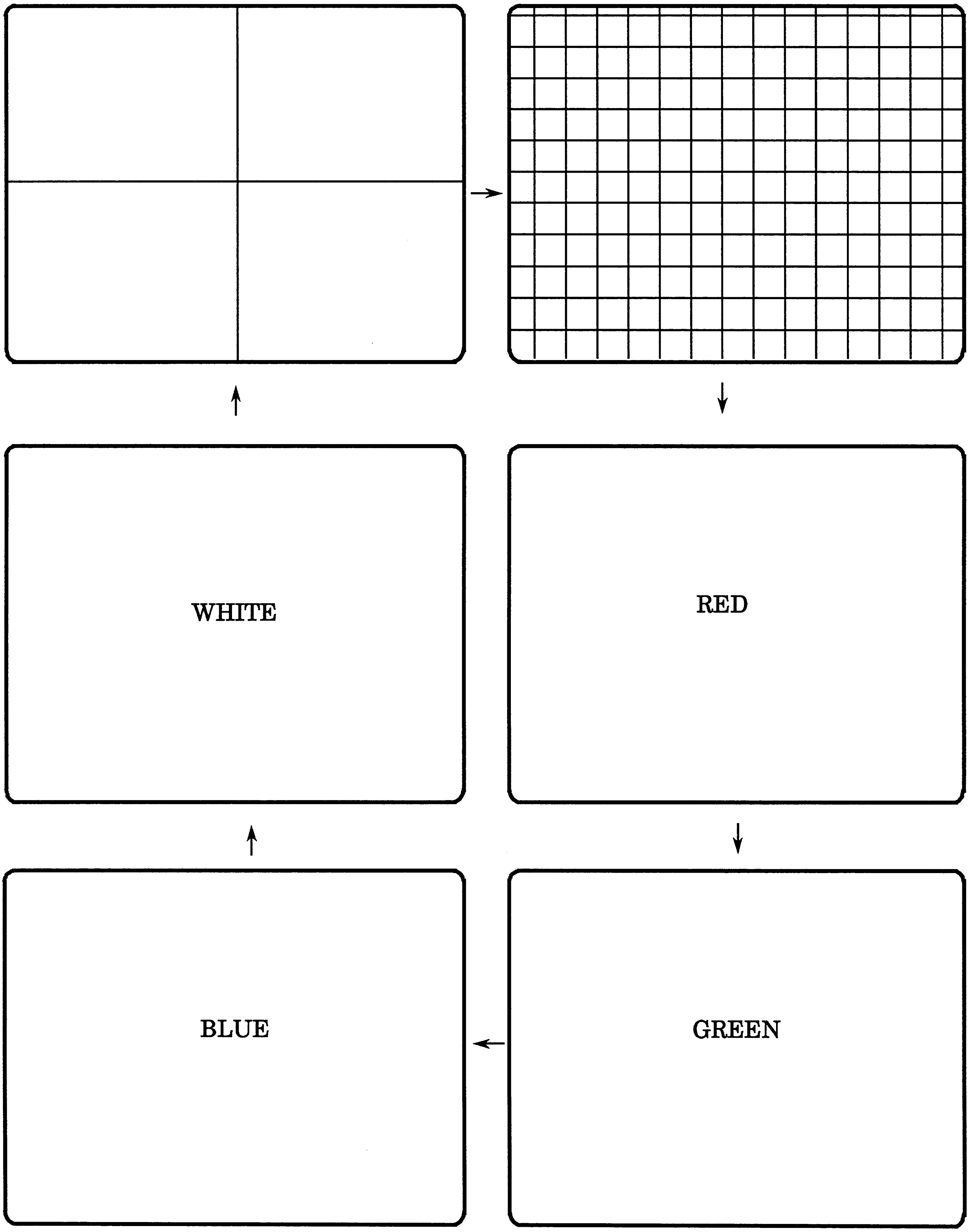


The Table-5 shows the function of the F1 ~ F6 keys in the GRAPHIC DISPLAY check mode.

[TABLE - 5]

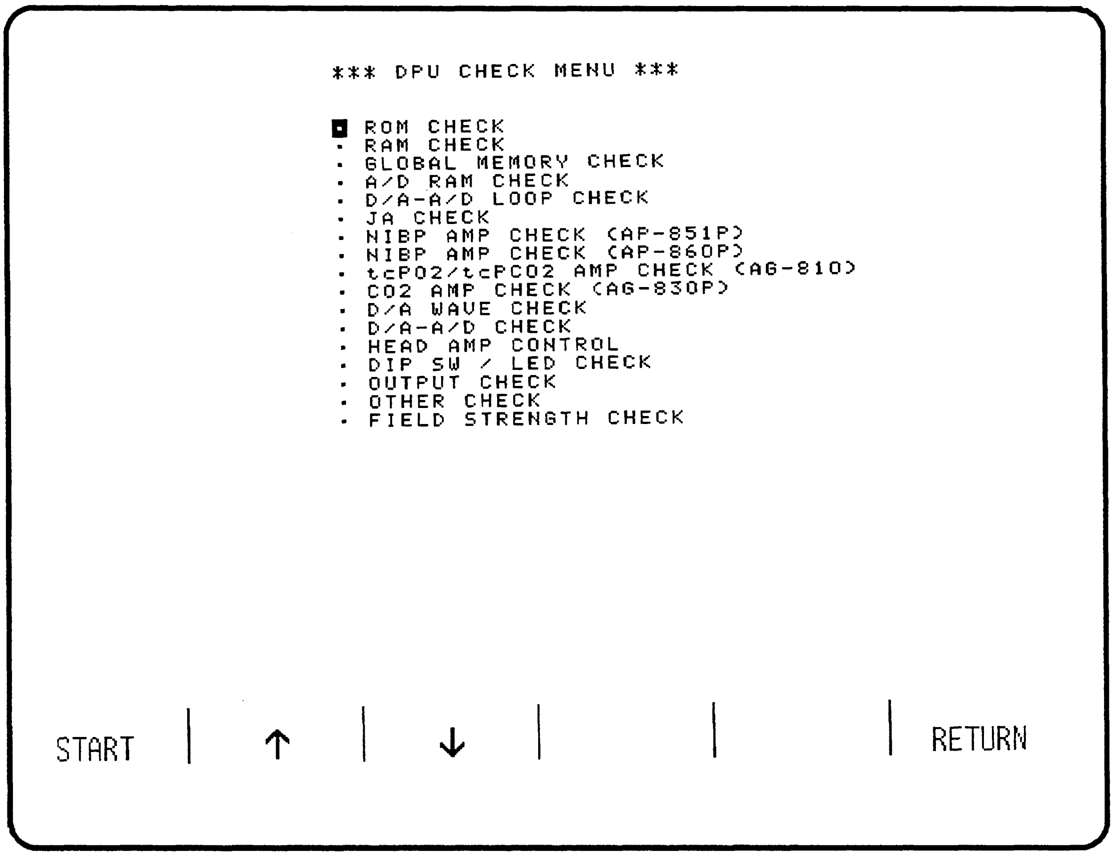
Key	Function
F1	Changes the graphic display screen.
F2	Move the screen downward.
F3	Move the screen upward.
F4	Move the screen to the left.
F5	Move the screen to the right.
F6	To return to the CRTC CHECK MENU

By pressing F1 key, the display changes as follows:


WHITE
RED
BLUE
GREEN

◆ DPU (Data Processing Unit board) check

The following display appears on the CRT by first pressing the REVIEW key and then pressing the "DPU CHECK" multifunction key in the CHECK MENU display.



```
*** DPU CHECK MENU ***

■ ROM CHECK
· RAM CHECK
· GLOBAL MEMORY CHECK
· A/D RAM CHECK
· D/A-A/D LOOP CHECK
· JA CHECK
· NIBP AMP CHECK (AP-851P)
· NIBP AMP CHECK (AP-860P)
· tcPO2/tcPCO2 AMP CHECK (AG-810)
· CO2 AMP CHECK (AG-830P)
· D/A WAVE CHECK
· D/A-A/D CHECK
· HEAD AMP CONTROL
· DIP SW / LED CHECK
· OUTPUT CHECK
· OTHER CHECK
· FIELD STRENGTH CHECK

START  |  ↑  |  ↓  |      |      |  RETURN
```

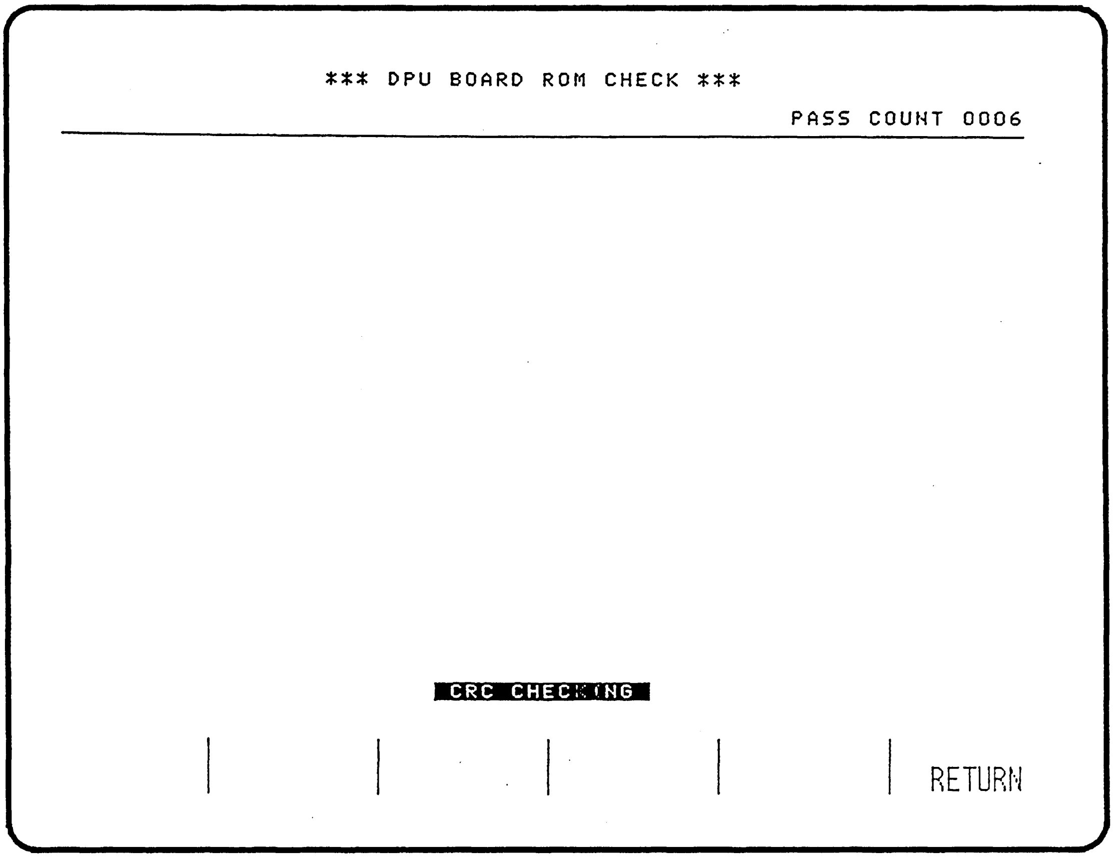
On the above display,

↑ ↓: to select a check item from the check items on the CRT

START: to execute the program for a selected check item while changing to the display for the check item

RETURN: to return to the CHECK MENU display

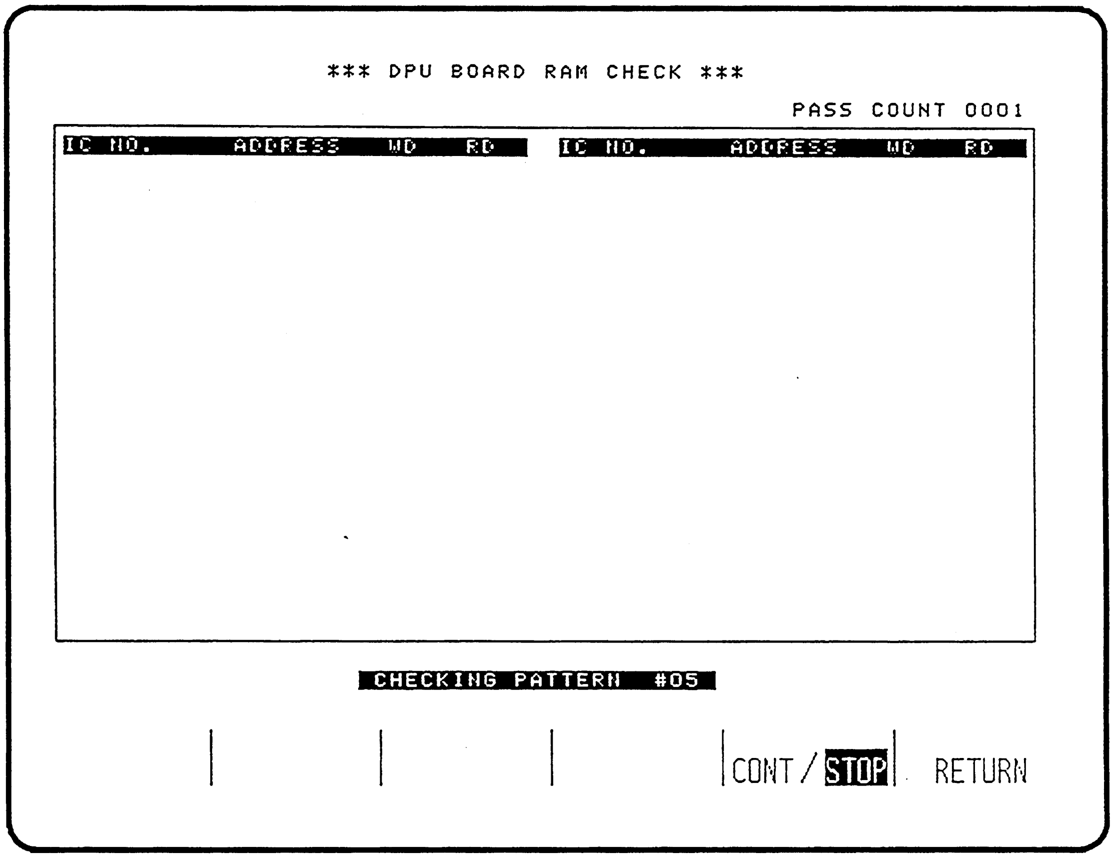
- **ROM check**



```
*** DPU BOARD ROM CHECK ***
                                   PASS COUNT 0006

                 CRC CHECKING
```

“CRC CHECKING” message blinks during the checking.
The check is executed with C.R.C. similar to the ROM CHECK on the CPU board.

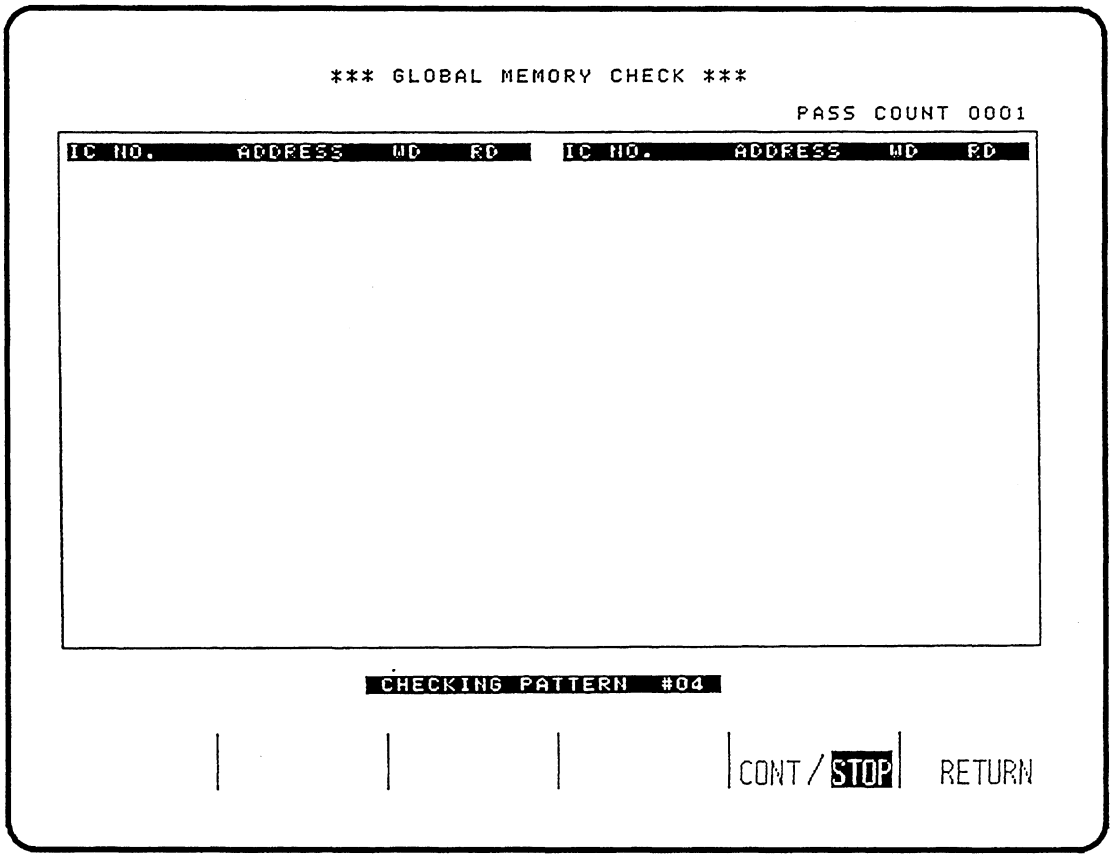
- **RAM check**



```
                *** DPU BOARD RAM CHECK ***
                                          PASS COUNT 0001
IC NO.       ADDRESS    WD    RD     IC NO.       ADDRESS    WD    RD

                  CHECKING PATTERN   #05
```

"CHECKING PATTERN #XX" message blinks during the checking. Patterns No. 1 to 15 of Table-1 are used as the check pattern. The check is the same as the RAM CHECK on the CPU board.

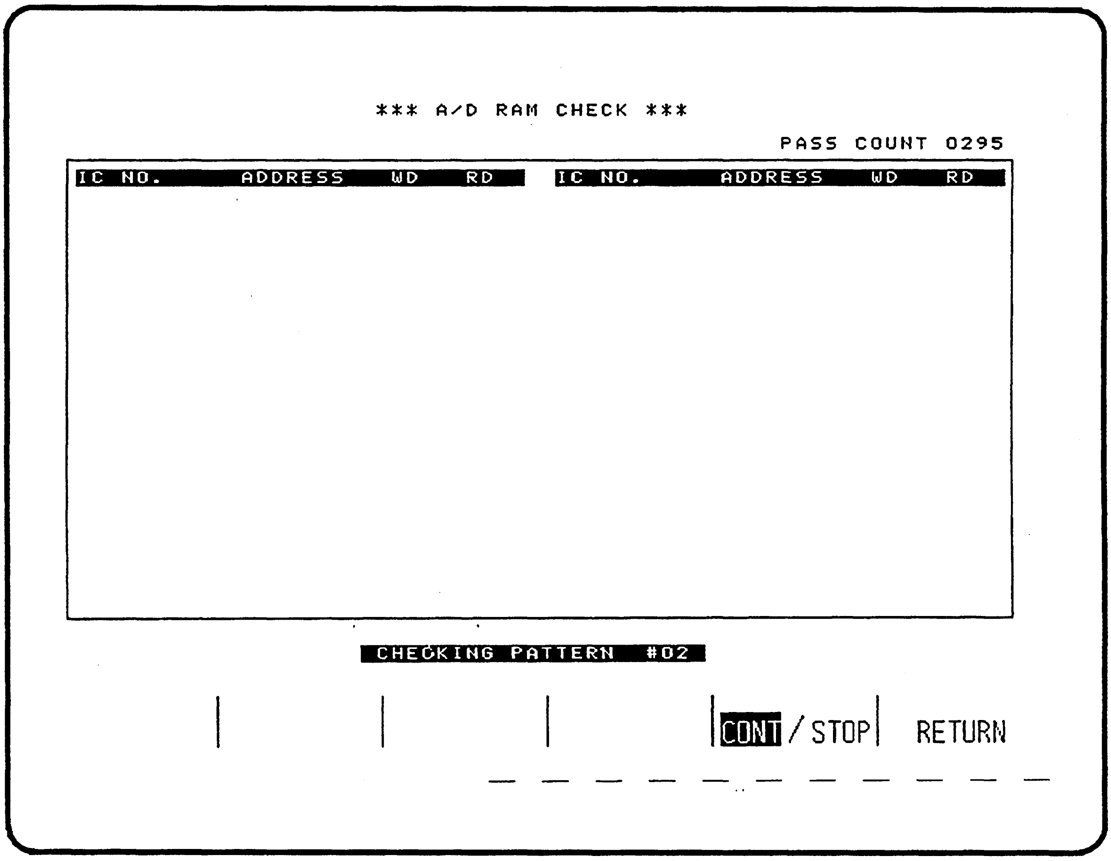
- **GLOBAL MEMORY check**



```
                 *** GLOBAL MEMORY CHECK ***
                                               PASS COUNT 0001
IC NO.      ADDRESS   WD   RD    IC NO.      ADDRESS   WD   RD





                 CHECKING PATTERN   #04

                                        CONT/STOP   RETURN
```

"CHECKING PATTERN #XX" blinks during the checking.
Patterns No. 1 to 15 of Table 1 are used as the check pattern. The check is the same as the GLOBAL MEMORY CHECK on the CPU board.

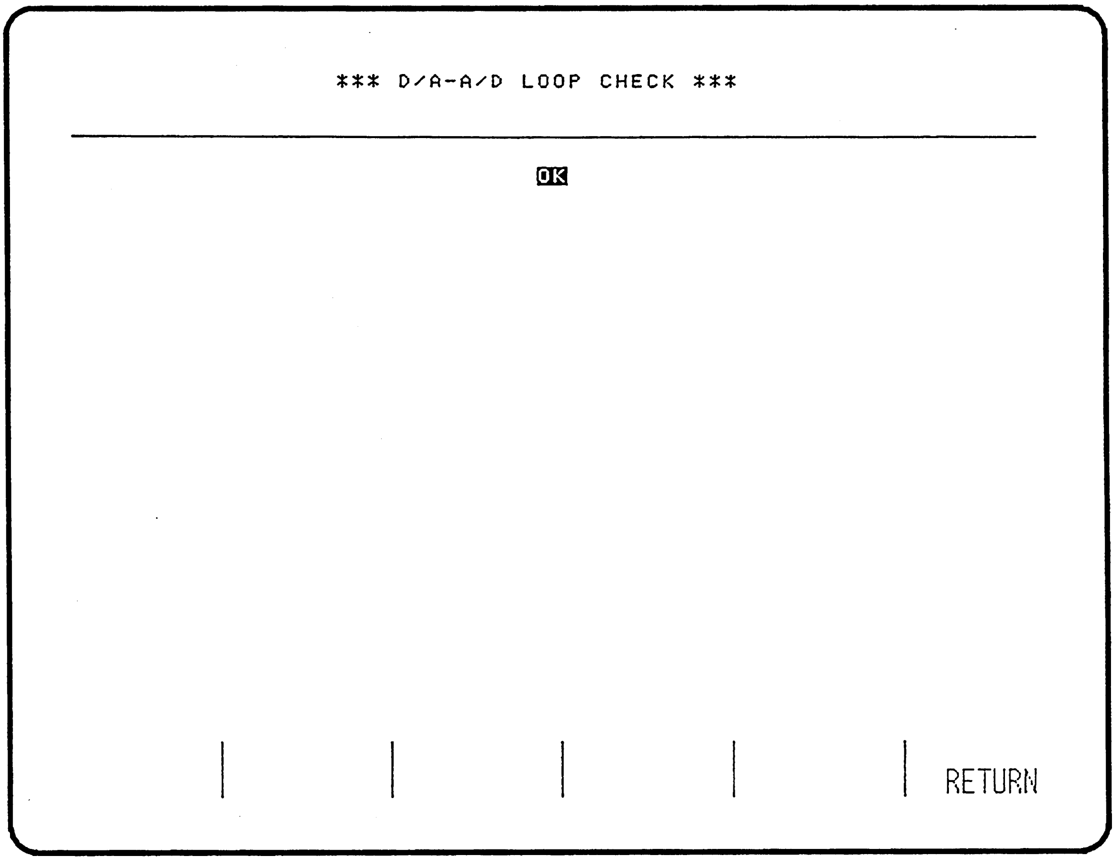
- **A/D RAM check**



```
                  *** A/D RAM CHECK ***
                                             PASS COUNT 0295
IC NO.     ADDRESS    WD    RD     IC NO.     ADDRESS    WD    RD




                  CHECKING PATTERN  #02
```

"CHECKING PATTERN #XX" blinks during the checking.
Patterns No. 1 to 15 of Table 1 are used as the check pattern. The check is the same as the RAM CHECK on the CPU board.

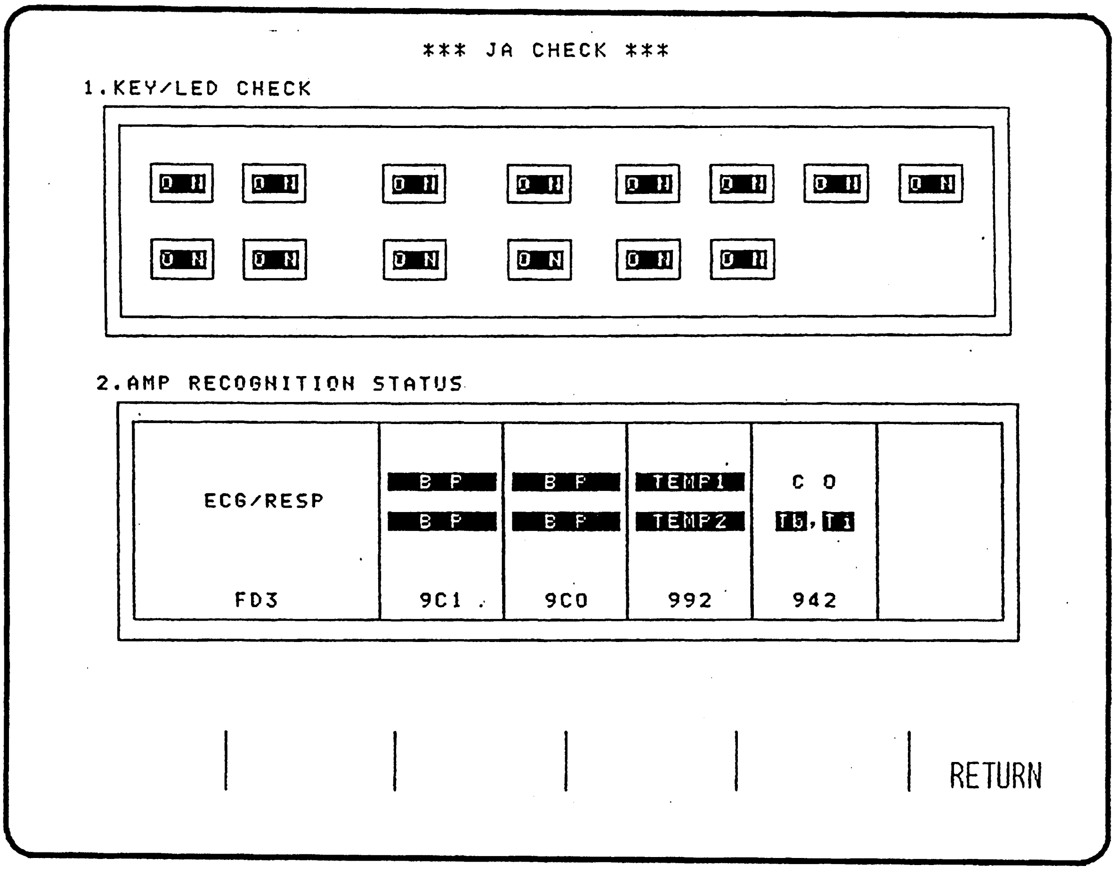
- **D/A - A/D Loop check**



```
*** D/A-A/D LOOP CHECK ***

OK
```

The result after checking the D/A - A/D LOOP, “OK” or “ERROR” is indicated. The check is the same as the D/A - A/D LOOP CHECK on the A/D - D/A CHECK display.

•**JA check (Input Box check)**



*** JA CHECK ***

1.KEY/LED CHECK

2.AMP RECOGNITION STATUS

ECG/RESP	B P B P	B P B P	TEMP1 TEMP2	C O Tb, Ti	
FD3	9C1	9C0	992	942	

1) KEY / LED CHECK

The "OFF" marks located according to the key switches on the operation panel of the Input box (JA-860PA/880PA) appear on the CRT. When a key switch is normal, the "OFF" mark changes to a reverse-lit "ON" mark accompanied by a high tone by pressing the key.

2) AMP RECOGNITION STATUS

When certain head-amplifiers are mounted, the amplifier name is indicated in the appropriate location. If an amplifier is not prepared for measurement, the indication is reverse-lit.

When a head-amplifier is not mounted, the corresponding position is blank. (See the right side of "CO Tb Ti 942" of above.)

NOTE

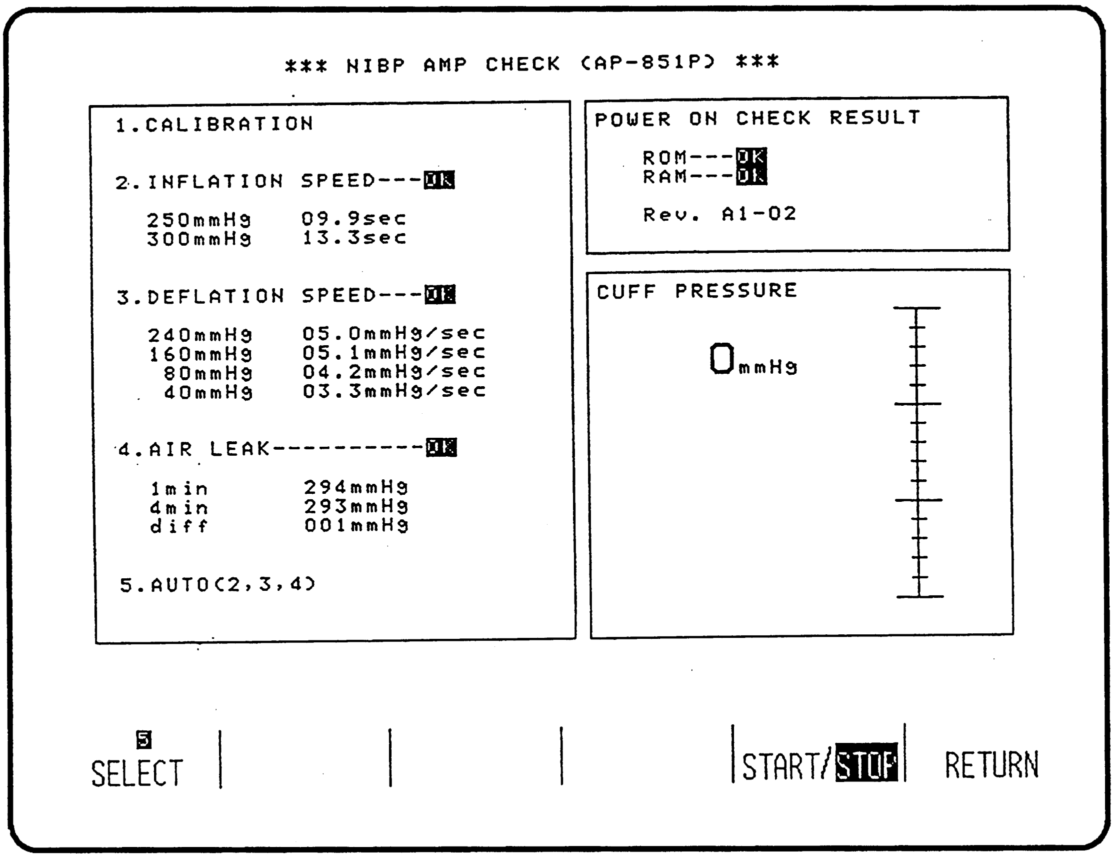
a) The ECG/RESP. head amplifier must be located next to the male receptacle for the connection cable between the input box and the main unit.

b) When one BP (Blood Pressure) head amplifier is mounted, the BP amp must be located next to the ECG/RESP. amp.

c) When the other BP amp is mounted, it must be located next to the BP amp already installed.

d) When no BP amp is mounted, the other head amplifier can be installed in any of the 5 slots of the JA-860PA Input Box, or, any of the 7 slots of the JA-880PA Input Box.

- **NIBP AMP check (AP-851P)**



```
*** NIBP AMP CHECK (AP-851P) ***

1.CALIBRATION                         POWER ON CHECK RESULT

2.INFLATION SPEED---OK                  ROM---OK
                                        RAM---OK
  250mmHg     09.9sec
  300mmHg     13.3sec                   Rev. A1-02

3.DEFLATION SPEED---OK                CUFF PRESSURE

  240mmHg     05.0mmHg/sec                 0mmHg
  160mmHg     05.1mmHg/sec
   80mmHg     04.2mmHg/sec
   40mmHg     03.3mmHg/sec

4.AIR LEAK----------OK

  1min        294mmHg
  4min        293mmHg
  diff        001mmHg

5.AUTO(2,3,4)
```

Approx. 10 sec after this mode is called up, the ROM and RAM check results, and software revision are displayed. Check items 1 to 5 require the dummy cuff chamber — a hermetically sealed box of 800 cc internal volume which is not deformed by a 300 mmHg pressure. Press the “SELECT” multifunction key to select the check item.

Calibration

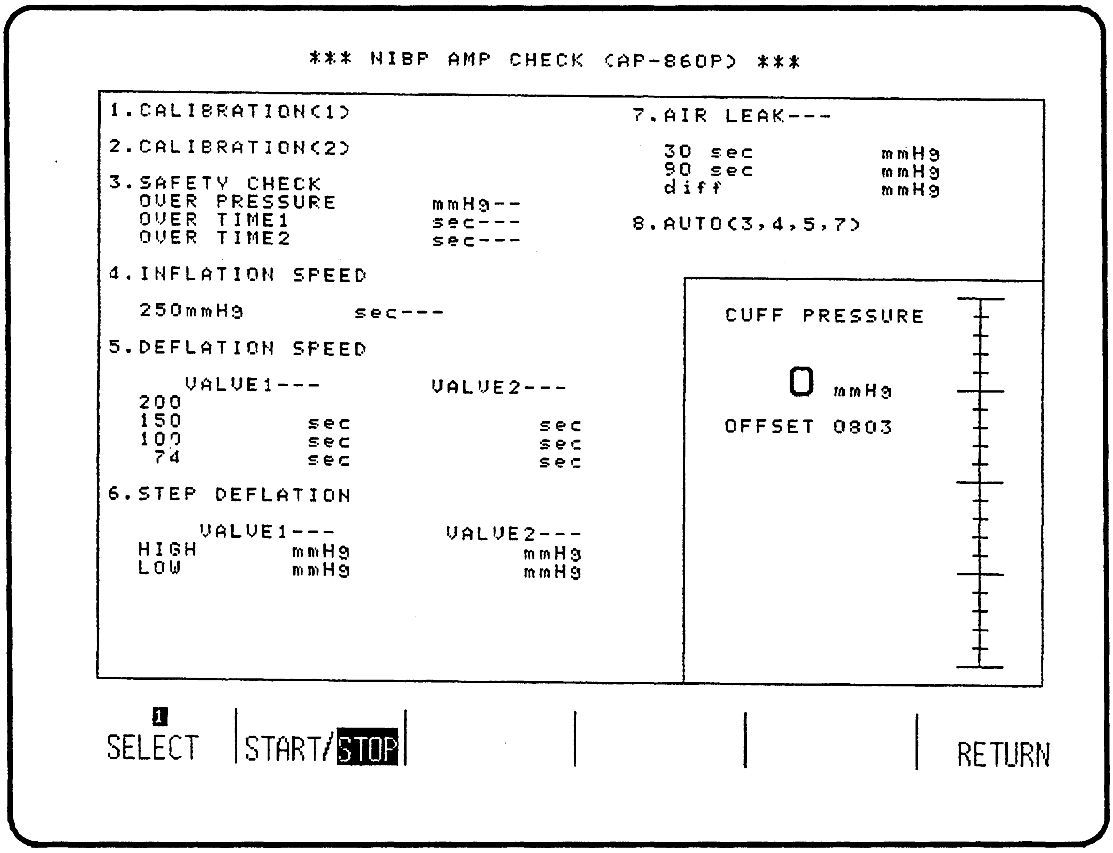
1. Connect the dummy cuff to the air hose connector.
2. Press the “START/STOP” multifunction key to start pressure inflation. Wait until the pressure becomes 180 mmHg.
3. Disconnect the dummy cuff from the air hose connector.
4. Connect the mercury manometer and external pump using the Y-tube joint.
5. Increase the pressure of the dummy cuff. Compare the reading on the manometer and the screen. Tolerance is ±3 mmHg (10 ~ 200 mmHg) and ±4 mmHg (201 ~ 300 mmHg).

Auto check for inflation speed, deflation speed, and air leak (Manual is also available)

1. Connect the dummy cuff to the air hose connector.
2. Press the “START/STOP” multifunction key. Check items 2 to 4 are automatically performed. If within the following tolerances, “OK” is displayed.

Inflation speed:	7 to 14 sec at 250 mmHg
Deflation speed:	4.7 to 6.0 mmHg/s at 240 and 160 mmHg, 3.5 to 5.0 mmHg/s at 80 mmHg, 2.3 to 4.2 mmHg/s at 40 mmHg
Air leak:	±3 mmHg difference between 1 min. and 4 min.

- **NIBP AMP check (AP-860P)**



```
*** NIBP AMP CHECK (AP-860P) ***

1.CALIBRATION(1)                          7.AIR LEAK---
2.CALIBRATION(2)                           30 sec          mmHg
                                           90 sec          mmHg
3.SAFETY CHECK                             diff            mmHg
  OVER PRESSURE          mmHg--
  OVER TIME1             sec---           8.AUTO(3,4,5,7)
  OVER TIME2             sec---
4.INFLATION SPEED
 250mmHg          sec---                   CUFF PRESSURE
5.DEFLATION SPEED
    VALUE1---            VALUE2---           0 mmHg
 200
 150         sec                sec        OFFSET 0803
 100         sec                sec
  74         sec                sec
6.STEP DEFLATION
     VALUE1---            VALUE2---
 HIGH         mmHg                mmHg
 LOW          mmHg                mmHg
```

WARNING

Do not connect the cuff to the patient when performing this check because some of the check programs in the NIBP AMP CHECK (AP-860P) menu exerts high pressure on the connected cuff.

Press the “SELECT” multifunction key to select the check item. If necessary, press the “START/STOP” multifunction key to start or stop the check of the selected check item.

1) CALIBRATION (1)
This check item requires an external hand bulb pump and a manometer to be connected to the two NIBP connectors on the NIBP head amplifier. Compare the pressure applied by the external pump on the manometer and that displayed on the NIBP AMP check display. Check whether the tolerance is within the values given in the table below, if not, performed the Pressure Gain Adjustment (refer to Sections 6-2-8).

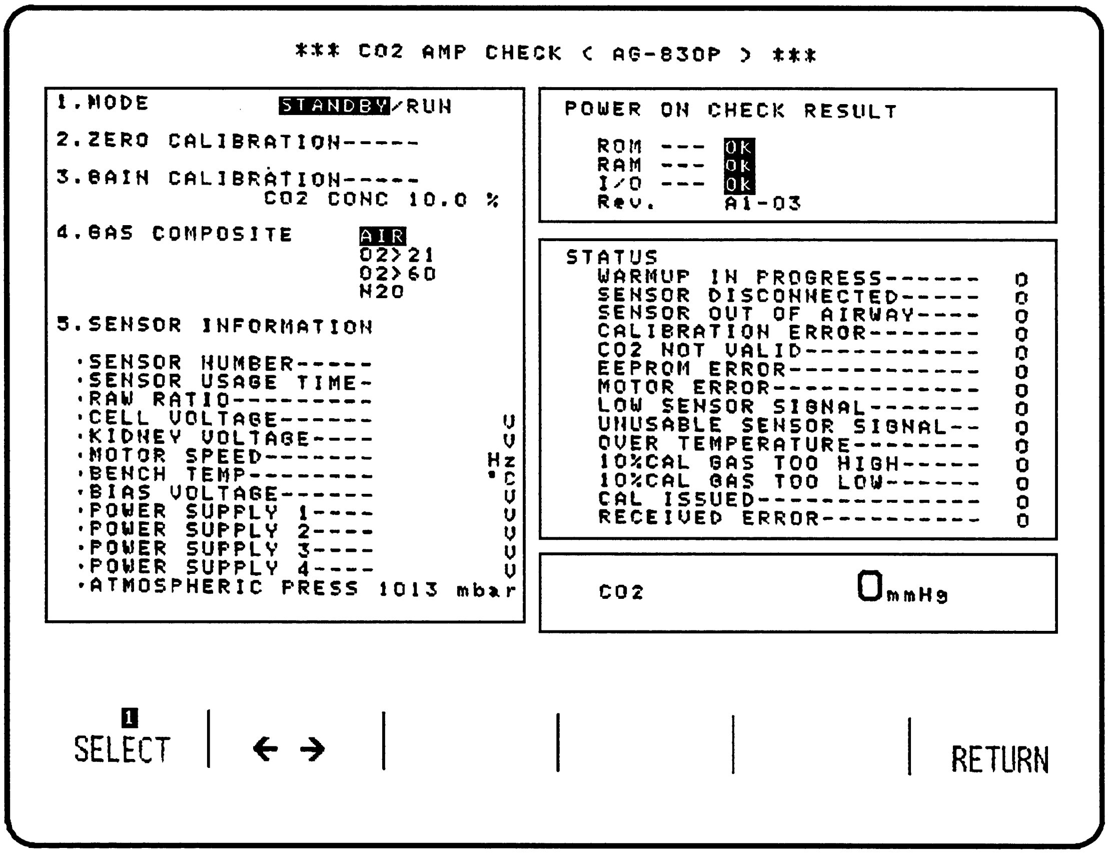
Applied Pressure Range	Tolerance
0 ~ 150 mmHg	±3 mmHg
150 ~ 290 mmHg	±2% reading

2) CALIBRATION (2)
The function of this check item is the same as that of CALIBRATION (1).

NOTE

Check items No. 3~8 are used in the factory during the production of the bedside monitor. Do not use these check items in the field.

- **CO2 AMP check (AG-830P)***



```
*** CO2 AMP CHECK < AG-830P > ***

1.MODE             STANDBY/RUN          POWER ON CHECK RESULT
2.ZERO CALIBRATION-----                   ROM --- OK
3.GAIN CALIBRATION-----                   RAM --- OK
              CO2 CONC 10.0 %             I/O --- OK
4.GAS COMPOSITE        AIR                Rev.    A1-03
                       O2>21
                       O2>60            STATUS
                       N2O                WARMUP IN PROGRESS------   0
5.SENSOR INFORMATION                      SENSOR DISCONNECTED-----   0
                                          SENSOR OUT OF AIRWAY----   0
 ·SENSOR NUMBER-----                      CALIBRATION ERROR-------   0
 ·SENSOR USAGE TIME-                      CO2 NOT VALID-----------   0
 ·RAW RATIO---------                      EEPROM ERROR------------   0
 ·CELL VOLTAGE------          V           MOTOR ERROR-------------   0
 ·KIDNEY VOLTAGE----          V           LOW SENSOR SIGNAL-------   0
 ·MOTOR SPEED-------         Hz           UNUSABLE SENSOR SIGNAL--   0
 ·BENCH TEMP--------         °C           OVER TEMPERATURE--------   0
 ·BIAS VOLTAGE------          V           10%CAL GAS TOO HIGH-----   0
 ·POWER SUPPLY 1----          V           10%CAL GAS TOO LOW------   0
 ·POWER SUPPLY 2----          V           CAL ISSUED--------------   0
 ·POWER SUPPLY 3----          V           RECEIVED ERROR----------   0
 ·POWER SUPPLY 4----          V
 ·ATMOSPHERIC PRESS 1013 mbar             CO2              0mmHg
```

*** Not available in the U.S.**

The CO2 AMP check item consists of the following:

1) Power On check
   The power on check checks the ROM, RAM, and input/output devices in the CO_2 head amplifier every time the CO2 AMP check is performed. The ROM, RAM, and input/output device checks are the same as those in the main unit of the bedside monitor. The result of the check is shown on the CO2 AMP check display.

2) CO_2 head amplifier status display
   Set the mode of the SELECT item No. 1 to RUN to display the status of the CO2 head amplifier. A status value of "1" means "YES" and "0" means "NO".

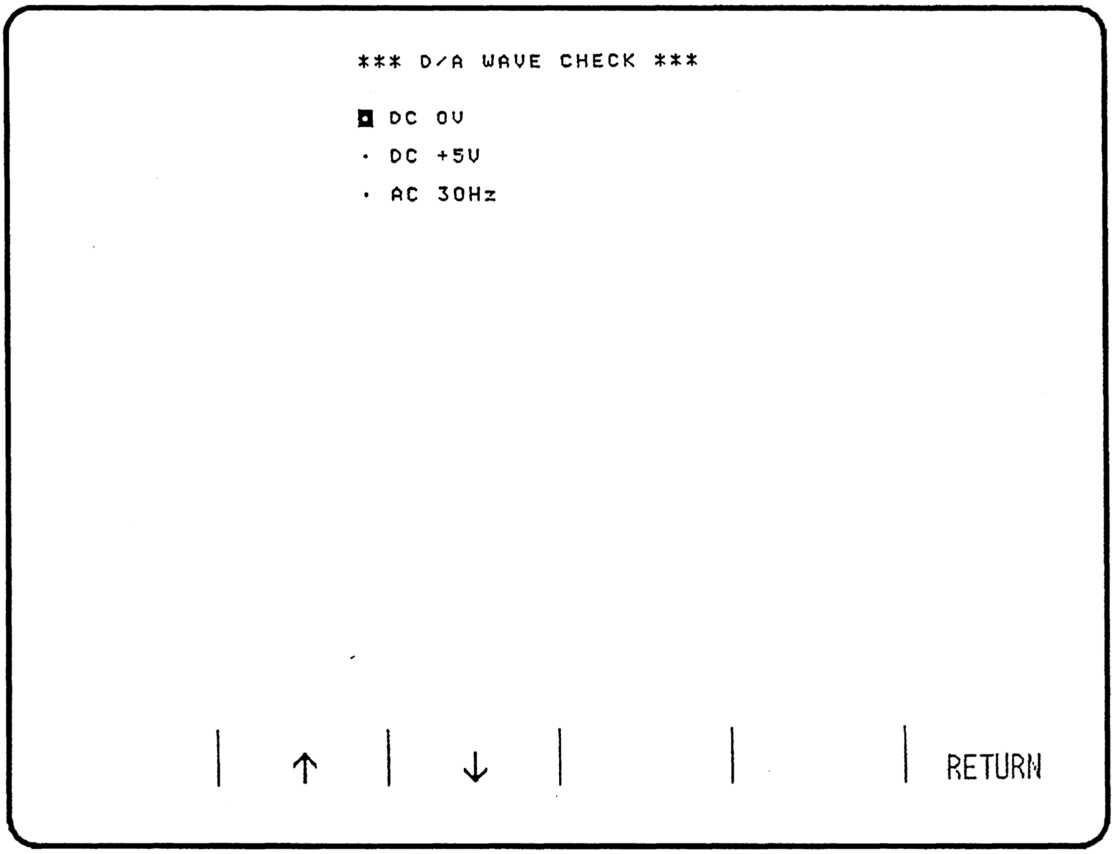
3) CO_2 sensor information
   In the RUN mode, select item No. 5 to display the CO_2 sensor information.

4) Calibration and setup items
   In the RUN mode, SELECT items No. 2 ~ 4 are used to calibrate and set the setting of the CO_2 head amplifier.

5) CO_2 measurement display
   Set the mode of the SELECT item No. 1 to RUN to display the measured CO_2 gas pressure reading.

The following sections are displayed by pressing the "REVIEW" and MANUAL CHECK keys simultaneously on the DIAGNOSTIC CHECK AND SYSTEM SETUP display. These sections are for your reference, since these check program are for product inspection at the factory.

- **D/A WAVE check**

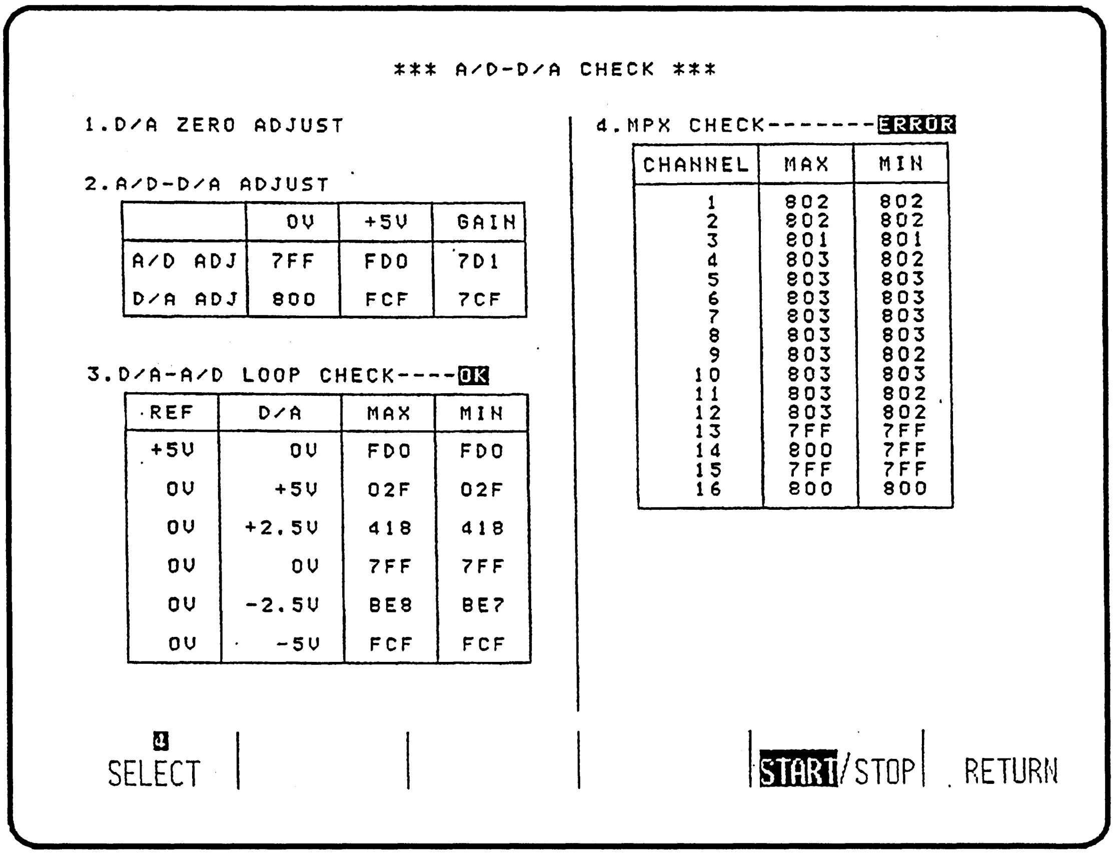


```
*** D/A WAVE CHECK ***

■ DC 0V
· DC +5V
· AC 30Hz
```

Check the waveform at the "DA" test pin (D/A converter output) on the DPU board. UP-0670 after selecting one of the following waveforms.

DC 0V: 0V is output at the test pin.
DC + 5V: + 5V d.c. is output at the test pin.
AC 60/30Hz: 6V$_{P\text{-}P}$ sine wave with 30.125 Hz is output for CH3 to CH8 at the test pin.
6V$_{P\text{-}P}$ sine wave with 60.25 Hz is output for ECG1W (CH1), ECG2 (CH2) at the test pin.
PSEUDO PACING WAVE: Pseudo pacing wave is output on ECG1 (CH1).

- **A/D - D/A check**



*** A/D-D/A CHECK ***

1.D/A ZERO ADJUST

2.A/D-D/A ADJUST

	0V	+5V	GAIN
A/D ADJ	7FF	FD0	7D1
D/A ADJ	800	FCF	7CF

3.D/A-A/D LOOP CHECK----OK

REF	D/A	MAX	MIN
+5V	0V	FD0	FD0
0V	+5V	02F	02F
0V	+2.5V	418	418
0V	0V	7FF	7FF
0V	-2.5V	BE8	BE7
0V	-5V	FCF	FCF

4.MPX CHECK-------ERROR

CHANNEL	MAX	MIN
1	802	802
2	802	802
3	801	801
4	803	802
5	803	803
6	803	803
7	803	803
8	803	803
9	803	802
10	803	803
11	803	802
12	803	802
13	7FF	7FF
14	800	7FF
15	7FF	7FF
16	800	800

SELECT:	to select a check item from check items No.1 to 4.
START/STOP:	to start or stop the check program for a selected item.

1) D/A ZERO ADJUST

The D/A converter output is set to 0V for the zero adjustment.

2) A/D - D/A ADJUST

[A/D ADJ]

When the D/A converter output voltage is set to 0V and the reference voltage (REF.) of the D/A converter is 0V or 5V, the respective A/D converter output value is indicated by the hexadecimal code in the table.

GAIN = (A/D value in 5V REF.) - (A/D value in 0V REF.)

[D/A ADJ]

When the reference voltage of the D/A is set to 0V and the D/A output voltage is 0V or 5V, the A/D output value is indicated by the hexadecimal code on the table.

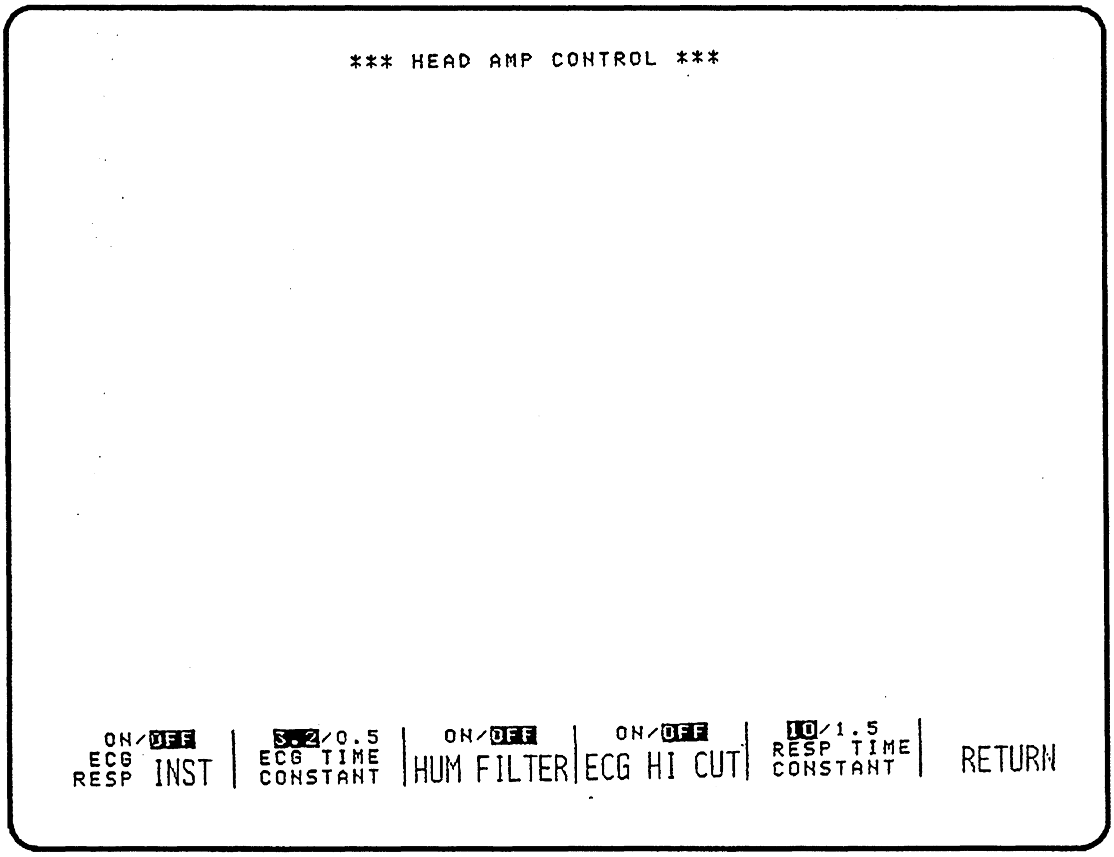
GAIN = (A/D value in 5V D/A out) - (A/D value in 0V D/A out)

3) D/A - A/D LOOP CHECK
When each REF. and D/A voltage is set as shown in the table, the maximum and Minimum values of the A/D output are indicated on the table after sampling the data. If the max. or min. value exceeds the regulated range, "ERROR" is indicated as shown in the table.

4) MPX CHECK (Multiplexer check) → Special jig is needed.
The input signals from the input box or the auxiliary input signals from external equipment (up to 16 channels) are switched for the one A/D with the two multiplexer in front of the A/D. The multiplexed signal is converted to a digital signal with the A/D converter. If the max. or min. value exceeds the regulated range, "ERROR" is indicated as shown next to "4.MPX CHECK".

- **HEAD AMP control**

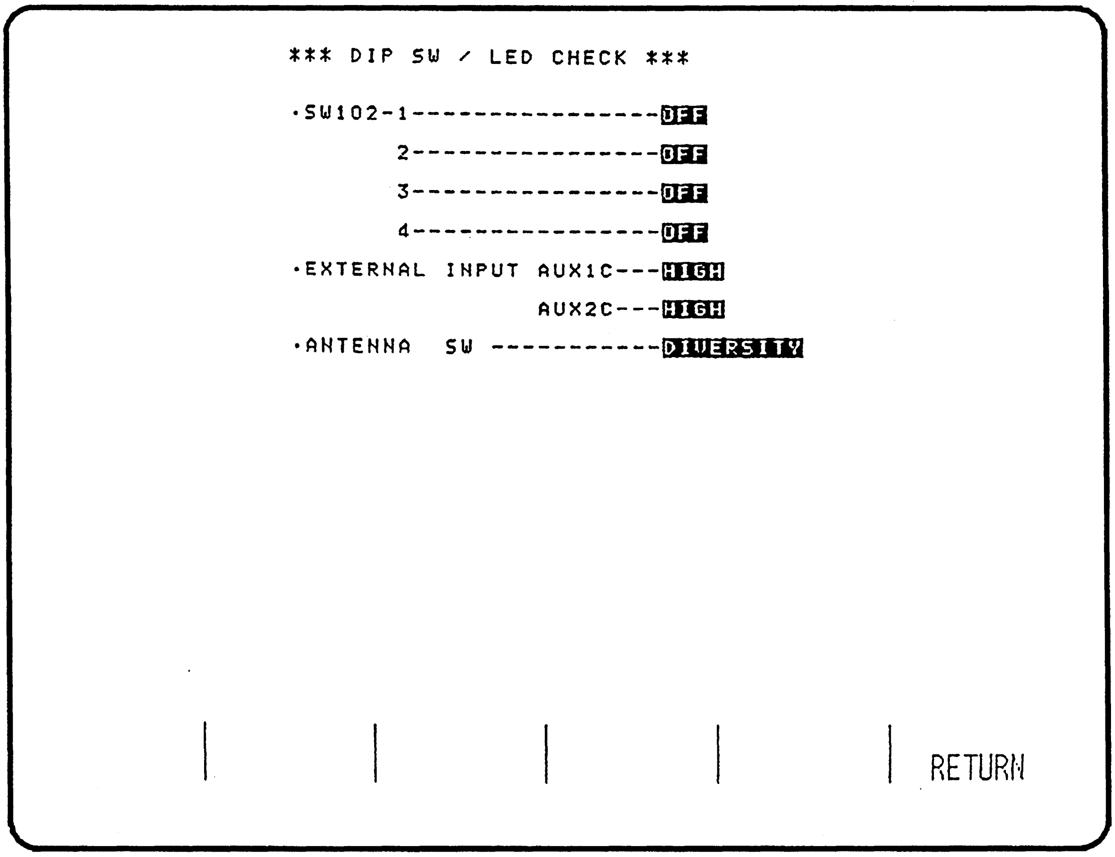
  The ECG/RESP Head-amplifier condition can be selected on this display for factory inspection only.



```
*** HEAD AMP CONTROL ***

ON/OFF      3.2/0.5                                        10/1.5
ECG         ECG TIME                                       RESP TIME
RESP INST | CONSTANT | ON/OFF HUM FILTER | ON/OFF ECG HI CUT | CONSTANT | RETURN
```

ECG/RESP INST:	ON/OFF selection of instantaneous short function against excessive voltage at the ECG/RESP input
ECG TIME CONSTANT:	3.2 sec. / 0.5 sec. selection of time constant (low cut filter) for ECG
HUM FILTER:	ON/OFF selection for ECG
ECG HI CUT:	ON/OFF selection of high cut filter (40Hz) for ECG
RESP TIME CONSTANT:	10 sec./ 1.5 sec. selection of time constant for Respiration waveform

- **DIP SW/LED check**



```
*** DIP SW / LED CHECK ***

·SW102-1----------------OFF
       2----------------OFF
       3----------------OFF
       4----------------OFF
·EXTERNAL INPUT AUX1C---HIGH
                AUX2C---HIGH
·ANTENNA  SW -----------DIVERSITY
```

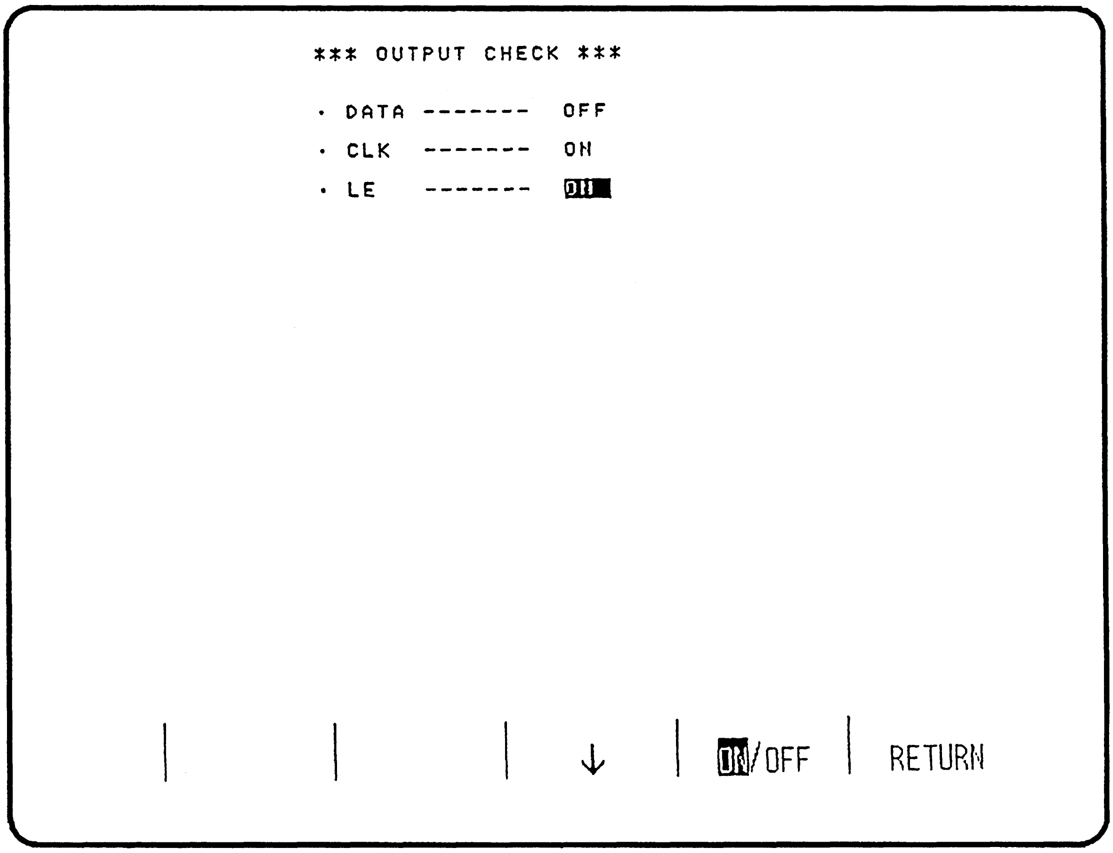
1) DIP SWITCH CHECK
   The set condition of the dip switch on the DPU board, SW102, appears on the CRT.

2) EXTERNAL INPUT CONTROL SIGNAL CHECK
   The control signals, AUX1C and AUX2C, must be indicated as "HIGH" when not connected with external equipment.

3) ANTENNA SWITCH CHECK
   The switch condition of the antenna (ANT1, DIVERSITY) is displayed.

4) LED CHECK
   Each LED on the DPU board sequentially lights and goes out one after another.

- **OUTPUT check**



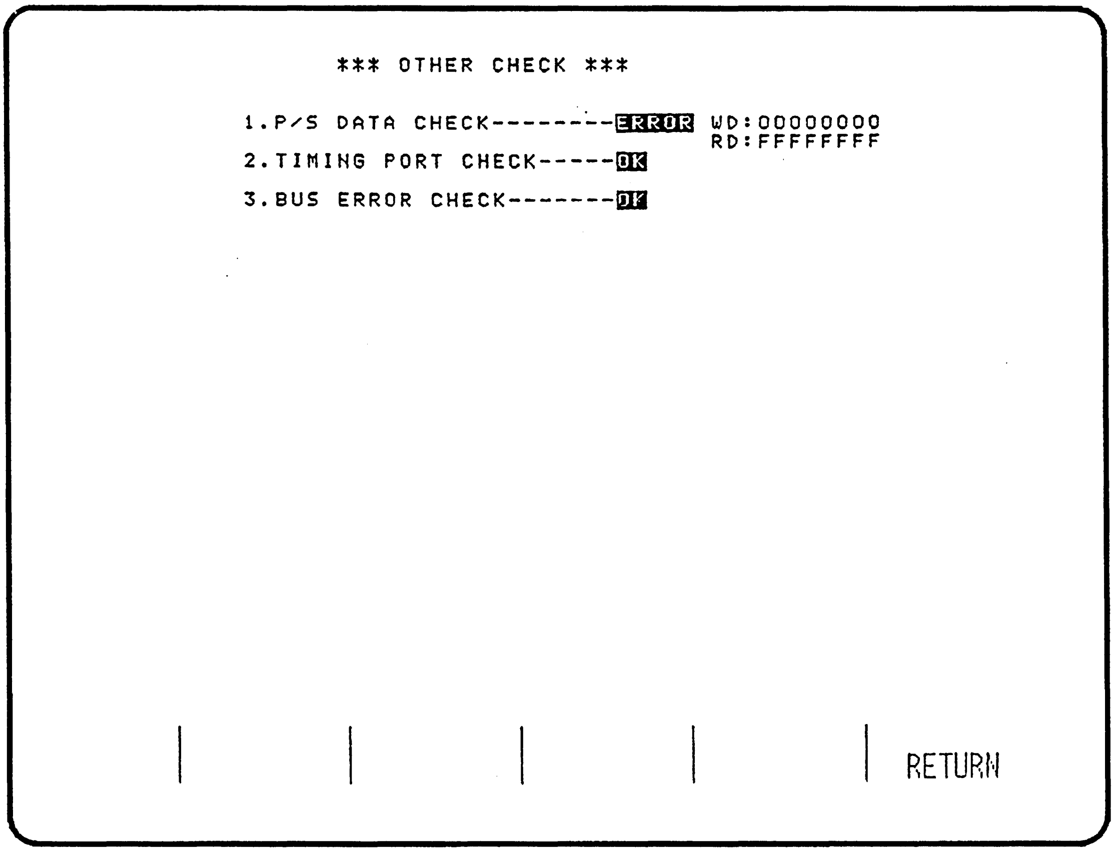
```
*** OUTPUT CHECK ***

· DATA -------  OFF
· CLK  -------  ON
· LE   -------  ON
```

1) DATA CHECK
High (ON) or Low (OFF) level signal is output.

2) CLK CHECK
High (ON) or Low (OFF) level signal is output on CLK line.

3) LE CHECK
High (ON) or Low (OFF) level signal is output on LE line.

- **OTHER check**



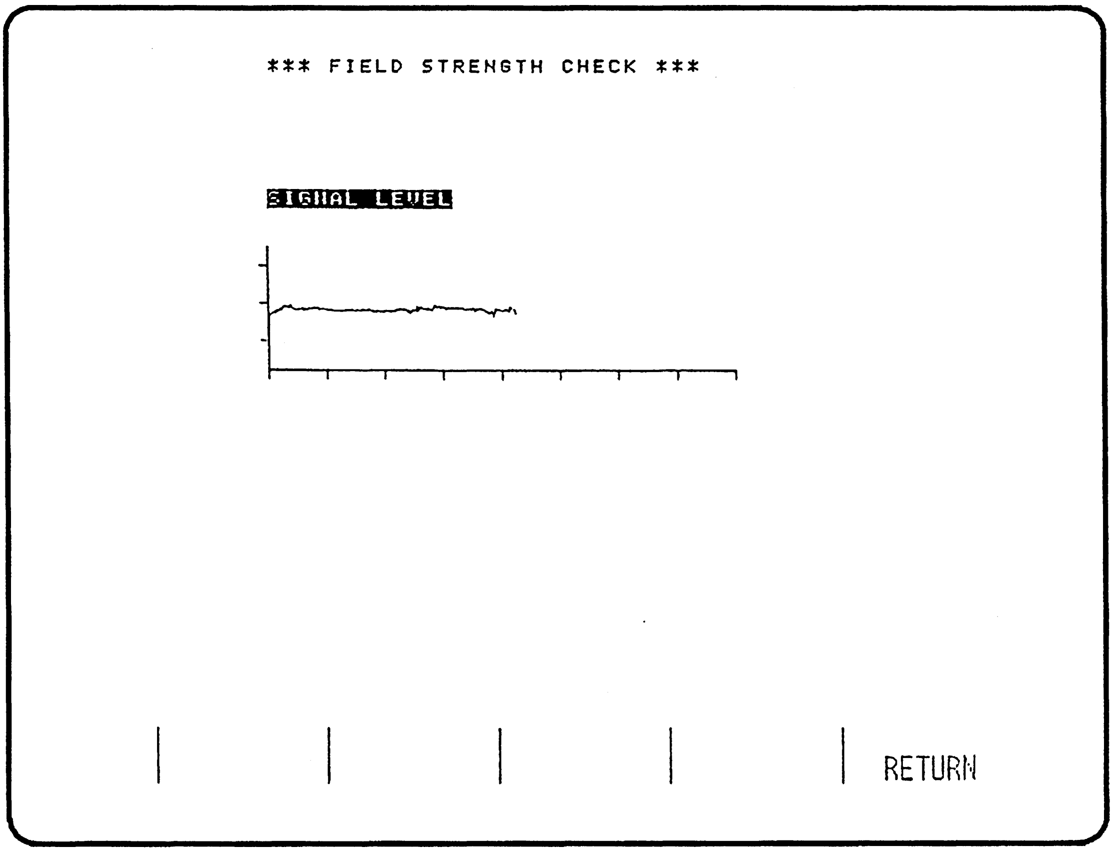
```
*** OTHER CHECK ***

1.P/S DATA CHECK---------ERROR WD:00000000
                               RD:FFFFFFFF
2.TIMING PORT CHECK-----OK
3.BUS ERROR CHECK-------OK
```

1) P/S DATA CHECK →jig for signal return is needed.
The check is executed by reading the S/P converter output via the jig instead of the input box after a 32bits data is inputted into the P/S converter.

2) TIMING PORT CHECK
The check is executed by confirming a increment of the data after reading a 4bits data of the Timing Port every 1 millisec.

3) BUS ERROR CHECK
The check is executed by confirming a Bus Error after accessing to the address where there is no memory area.

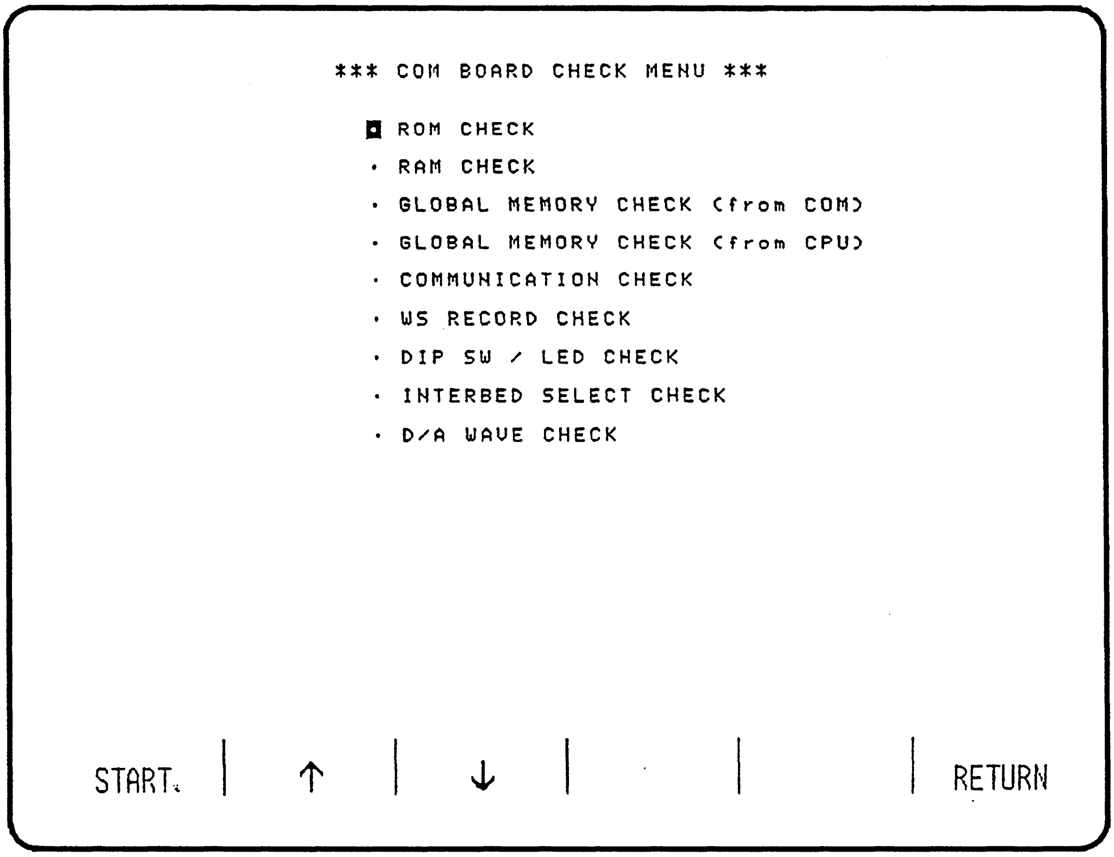
- **FIELD STRENGTH check**


*** FIELD STRENGTH CHECK ***
SIGNAL LEVEL
RETURN

Field strength of the receiving signal is displayed with a scale of 30 seconds.

◆COM check (Communication board check)

The following display appears on the CRT by first pressing the REVIEW key and then pressing the "COM CHECK" multifunction key in the CHECK MENU display.



```
*** COM BOARD CHECK MENU ***

■ ROM CHECK
· RAM CHECK
· GLOBAL MEMORY CHECK (from COM)
· GLOBAL MEMORY CHECK (from CPU)
· COMMUNICATION CHECK
· WS RECORD CHECK
· DIP SW / LED CHECK
· INTERBED SELECT CHECK
· D/A WAVE CHECK
```

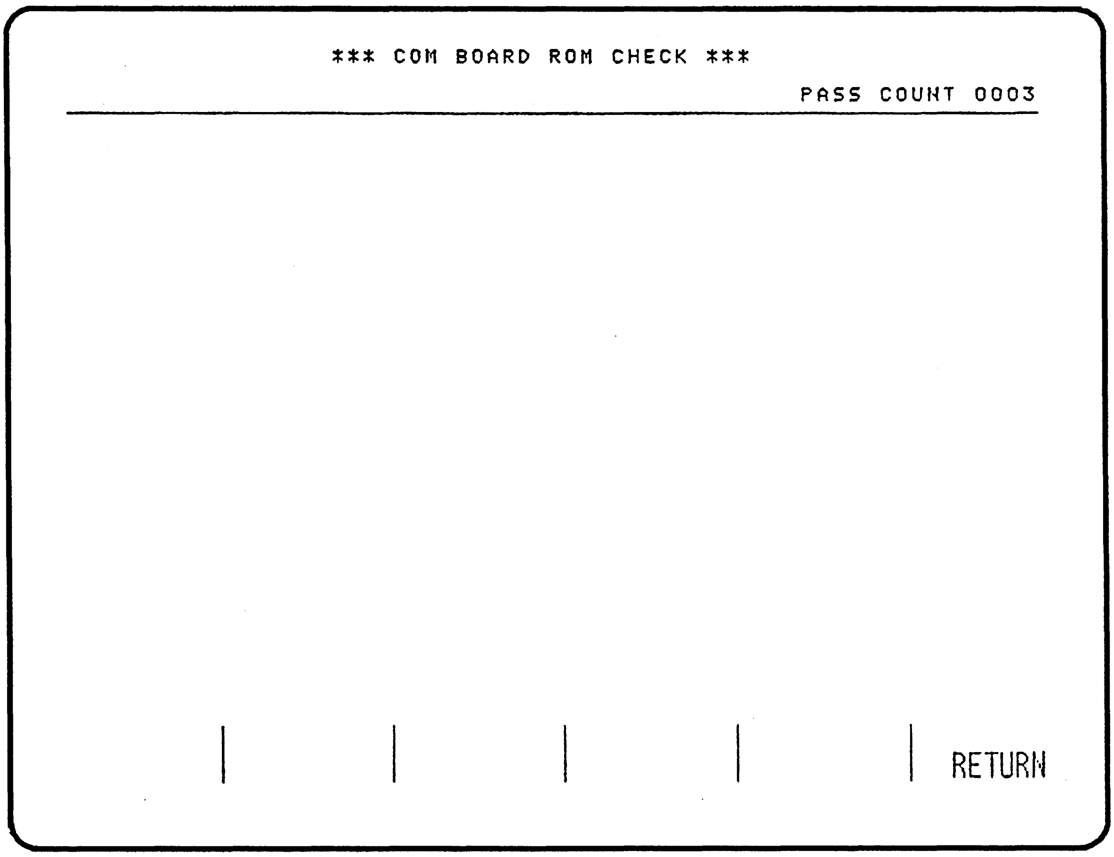
On the above display,

↑ ↓: to select a check item from the check items on the CRT

START: to execute the program for a selected check item while changing to the display for the check item

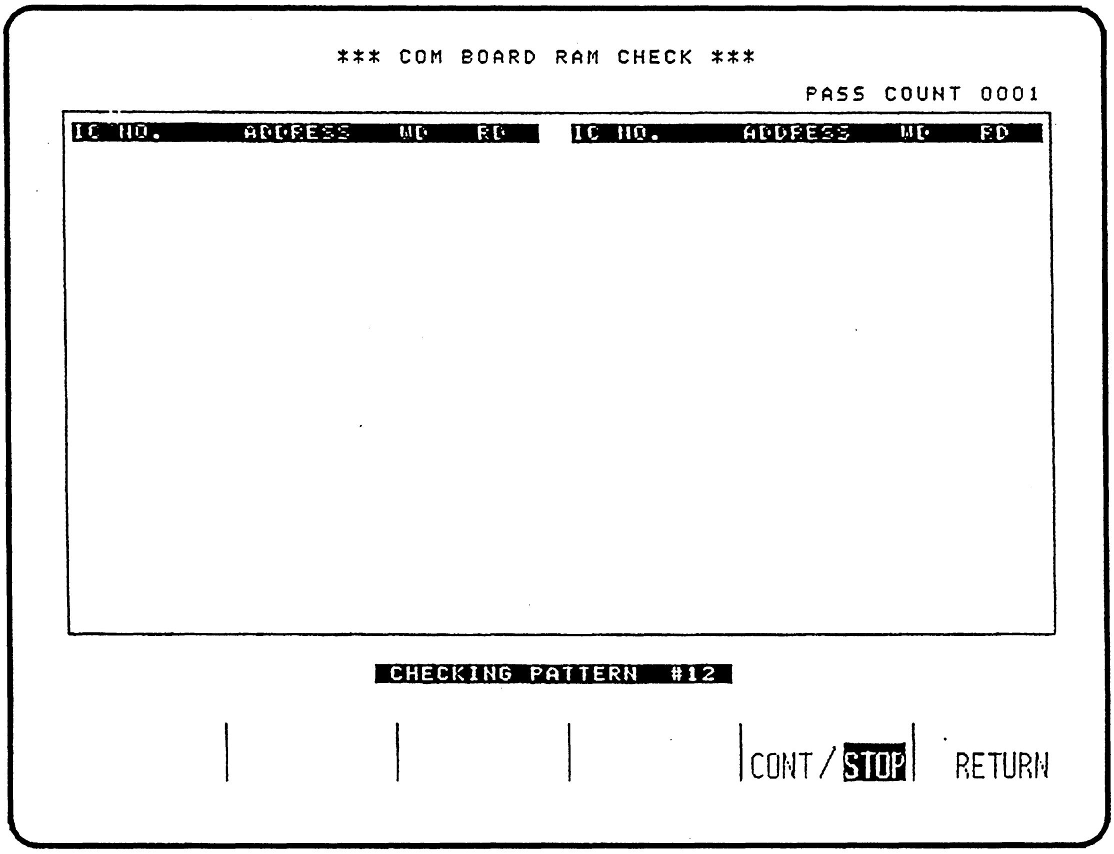
RETURN: to return to the CHECK MENU display

- **ROM check**
  The check is the same as the ROM check in "POWER-ON INITIAL SELF CHECK".



```
*** COM BOARD ROM CHECK ***
                                  PASS COUNT 0003
```

- **RAM check**

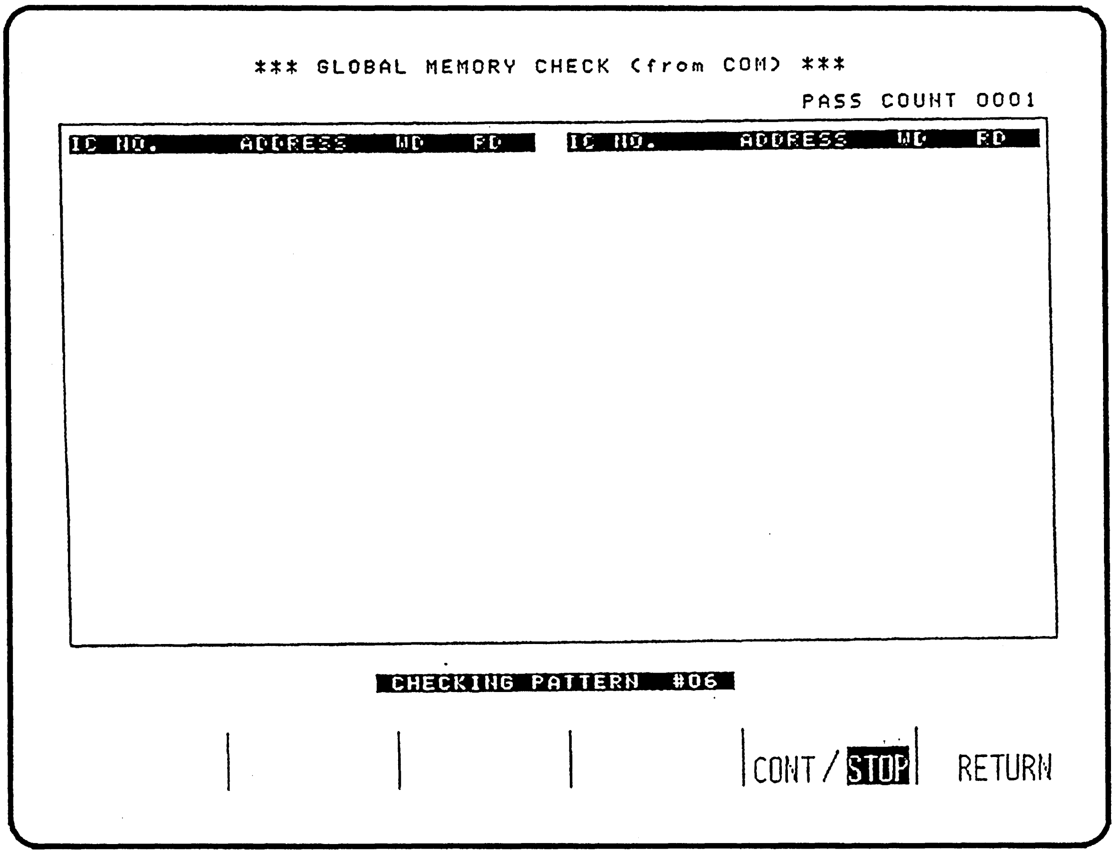


```
*** COM BOARD RAM CHECK ***
                                          PASS COUNT 0001
IC NO.      ADDRESS   WD   RD    IC NO.      ADDRESS   WD   RD



              CHECKING PATTERN #12
```

The following check patterns (No.1 to 20) are applied to this RAM check or the next GLOBAL MEMORY CHECK. The check is the same as the RAM CHECK on the CPU board.

No.	PATTERN	No.	PATTERN
1	55H	11	10H
2	AAH	12	EFH
3	01H	13	20H
4	FEH	14	DFH
5	02H	15	40H
6	FDH	16	BFH
7	04H	17	80H
8	FBH	18	7FH
9	08H	19	The same pattern as the COM RAM check pattern in "POWER-ON INITIAL SELF CHECK".
10	F7H	20	FFH

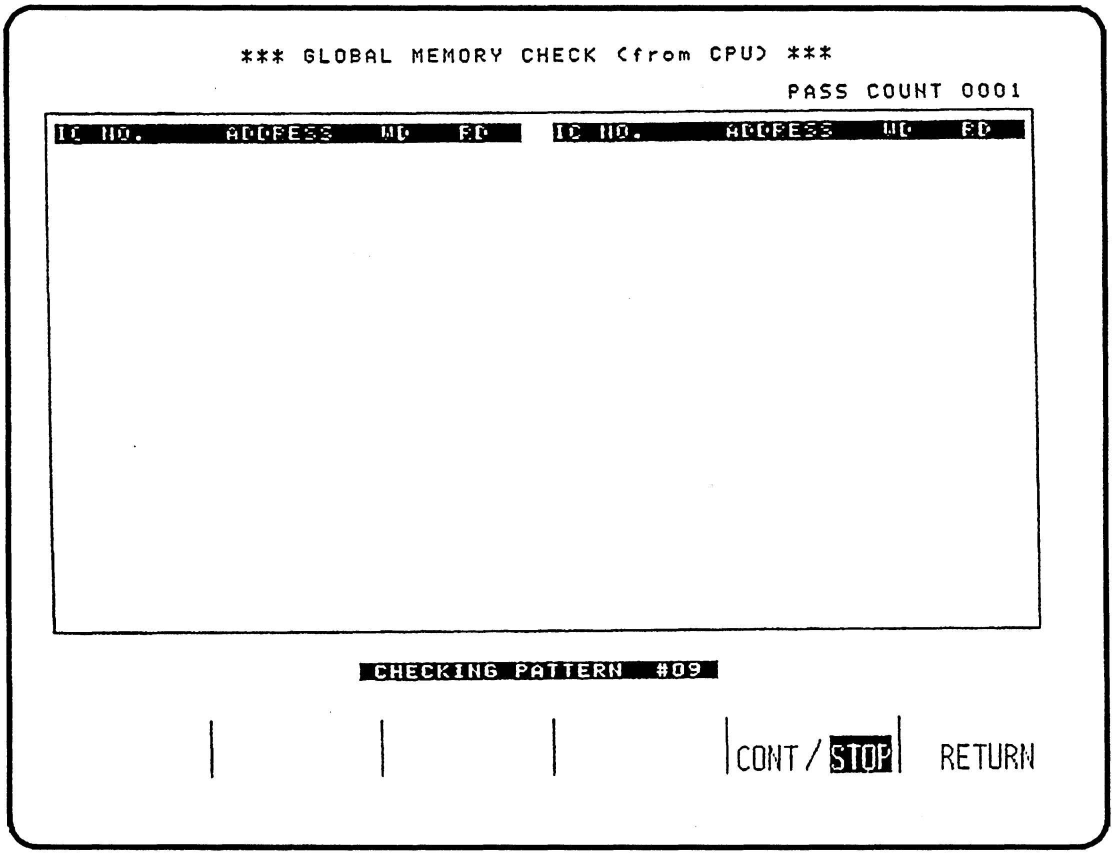
- **GLOBAL MEMORY check (from COM)**
  The Global memory is accessed from the MPU on the COM board. The check is the same as the RAM CHECK on the CPU board.



```
*** GLOBAL MEMORY CHECK (from COM) ***
                                      PASS COUNT 0001
IC NO.     ADDRESS   WD   RD   IC NO.     ADDRESS   WD   RD

                    CHECKING PATTERN  #06
```

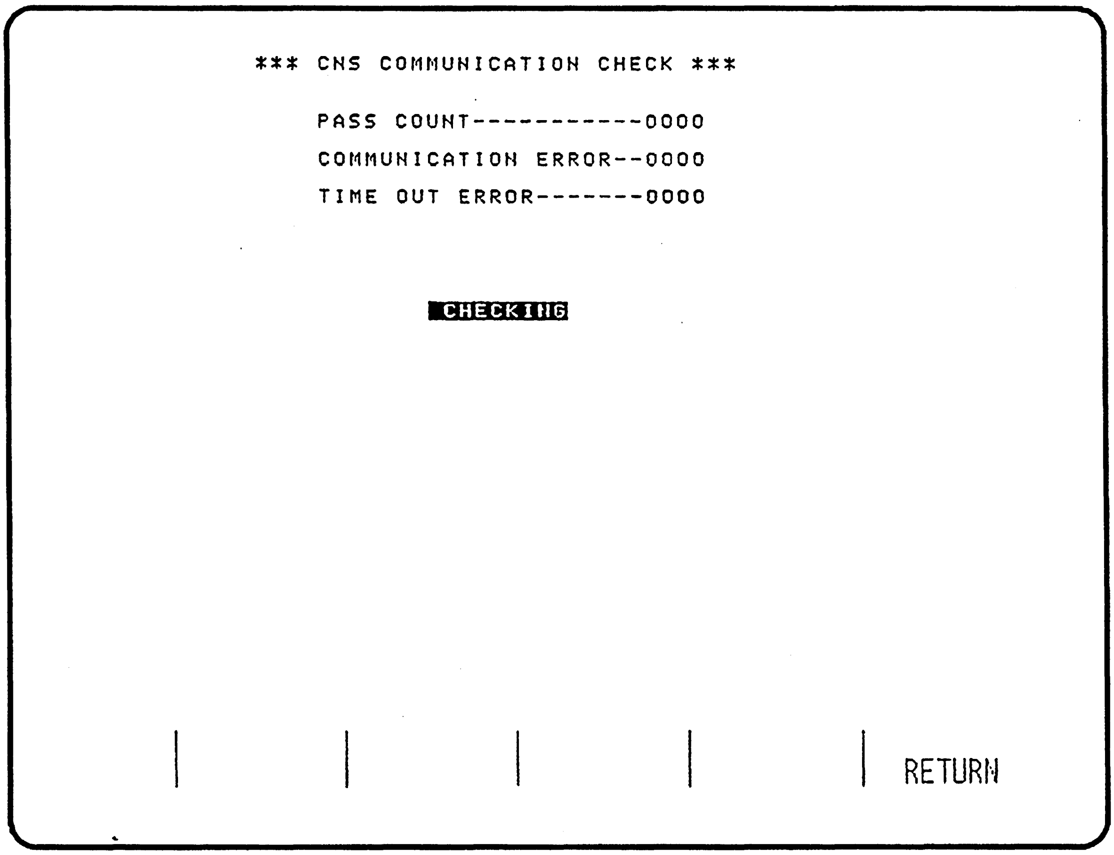
- **GLOBAL MEMORY check (from CPU)**

  The Global memory is accessed from the MPU on the CPU board. The check is the same as the RAM CHECK on the CPU board.



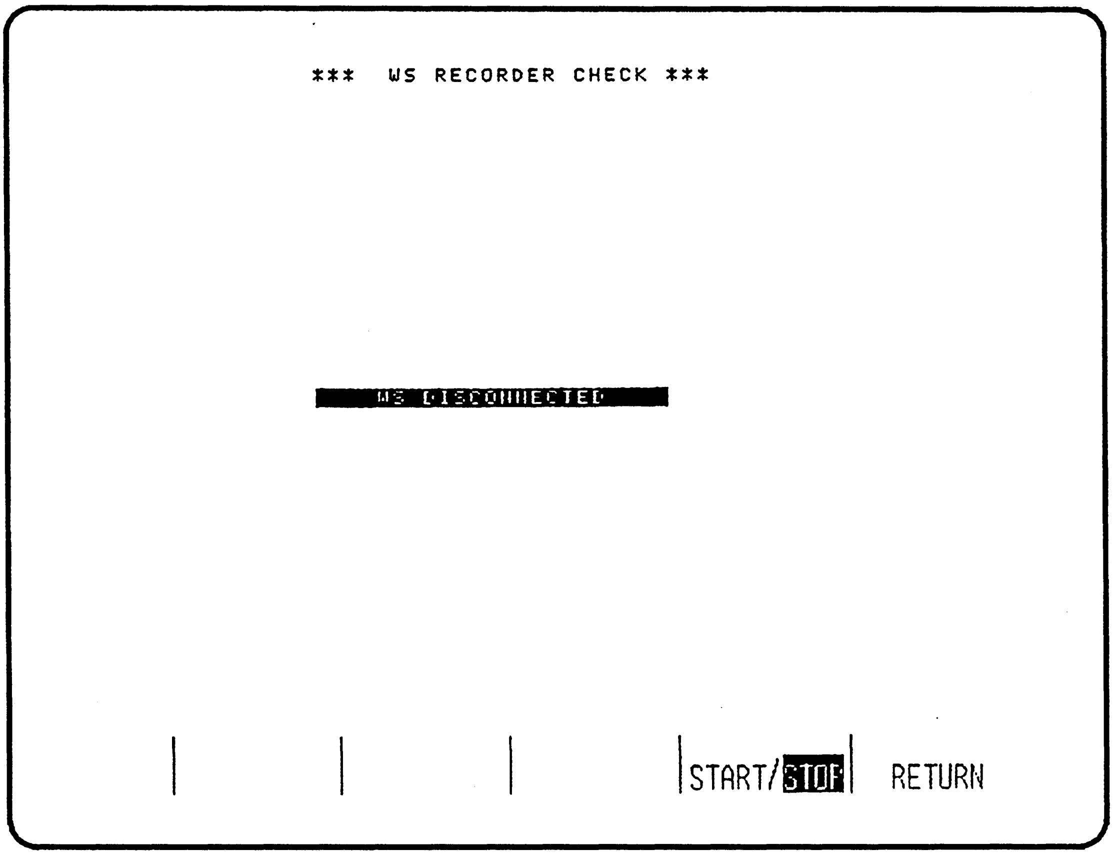
```
*** GLOBAL MEMORY CHECK (from CPU) ***
                                   PASS COUNT 0001
IC NO.      ADDRESS    WD   RD   IC NO.      ADDRESS    WD   RD

CHECKING PATTERN  #09
```

- **CNS COMMUNICATION check**
  The check is executed by transferring a regulated communication test data to a Central Monitor (CNS-8200).
  "CHECKING " message blinks during the checking.



```
*** CNS COMMUNICATION CHECK ***

    PASS COUNT-----------0000
    COMMUNICATION ERROR--0000
    TIME OUT ERROR-------0000


           CHECKING
```

- **WS RECORD check (recorder check)**



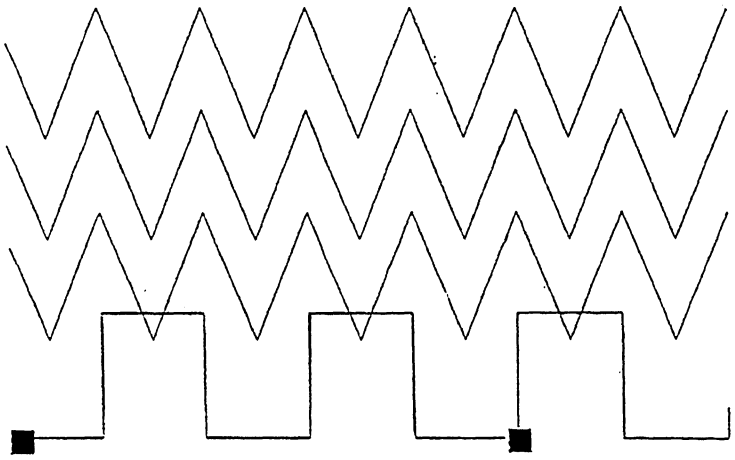
*** WS RECORDER CHECK ***

WS DISCONNECTED

On the above display,

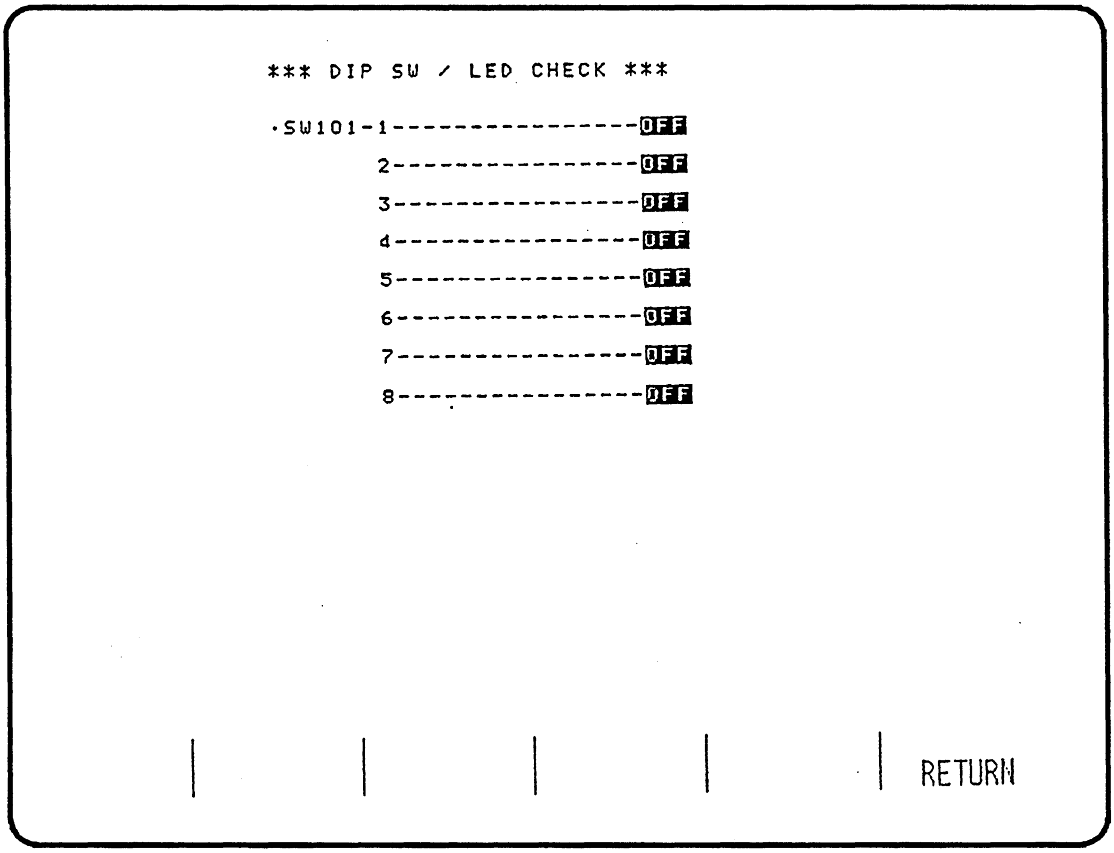
START/STOP:	to start to record sawtooth and square waveform on the recording paper or stop recording and printing
RETURN:	to return to the COM BOARD CHECK MENU

Recording example



The following sections are displayed by pressing the "REVIEW" and MANUAL CHECK keys simultaneously on the DIAGNOSTIC CHECK AND SYSTEM SETUP display. These sections are for your reference since these check programs are for product inspection at the factory.

- **DIP SW / LED Check**



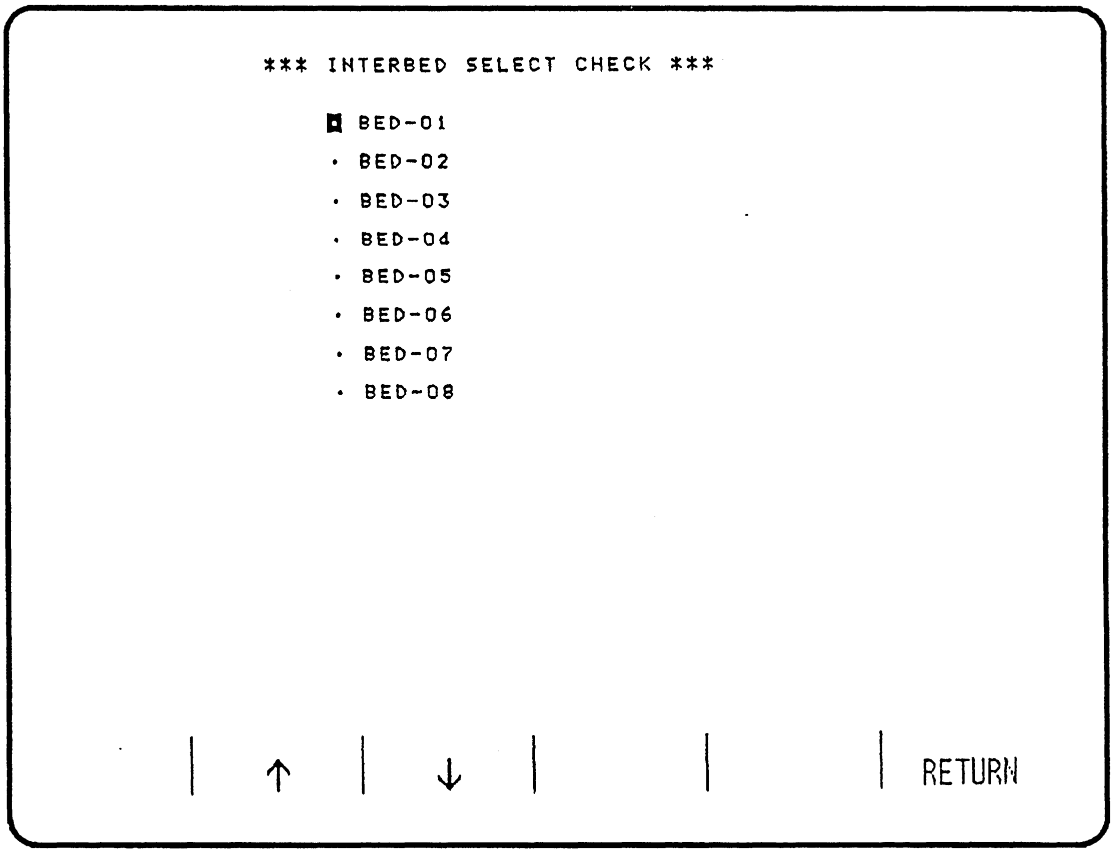
```
*** DIP SW / LED CHECK ***

·SW101-1----------------OFF
       2----------------OFF
       3----------------OFF
       4----------------OFF
       5----------------OFF
       6----------------OFF
       7----------------OFF
       8----------------OFF
```

1) DIP SWITCH CHECK
The set condition of the dip switch (SW101) on the COM board appears on the CRT.

2) LED CHECK
Each LED (8bits) on the COM board sequentially lights and goes out one after another.

- **INTERBED SELECT check**

The signal to select the other Bedside Monitor, "IBSEL", is output by this check.



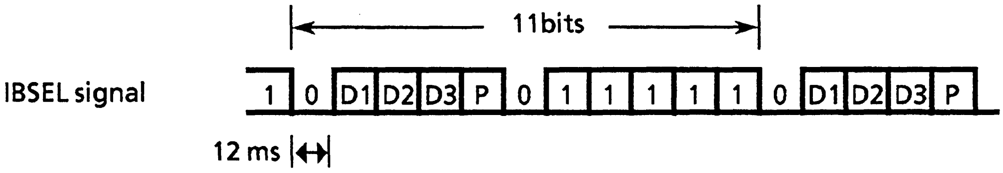
```
*** INTERBED SELECT CHECK ***

■ BED-01
· BED-02
· BED-03
· BED-04
· BED-05
· BED-06
· BED-07
· BED-08
```

On the above display,

↑ ↓: to select any other bed number

RETURN: to return to the COM BOARD CHECK MENU

The signal "IBSEL" (serial signal) consists of 11bits of serial format data.

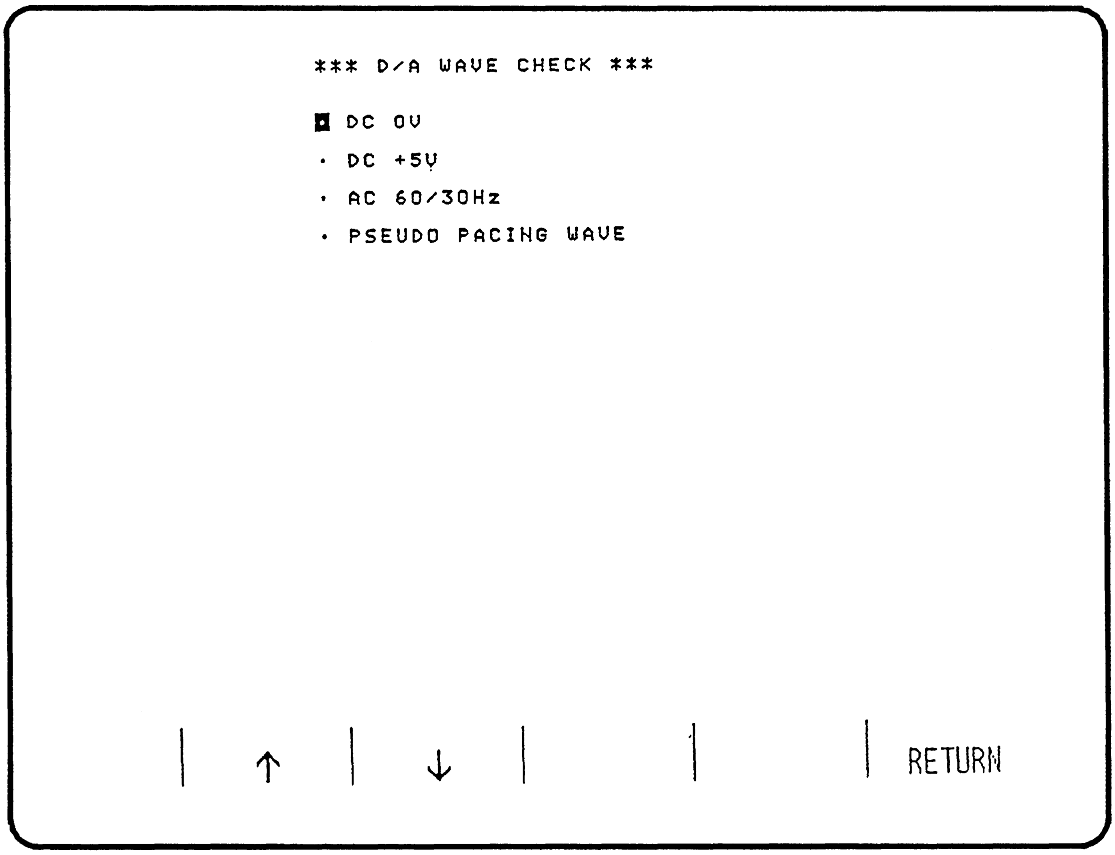


11bits
IBSEL signal
1
0
D1
D2
D3
P
0
1
1
1
1
1
0
D1
D2
D3
P
12 ms

Note: Selection of BED1 to BED8 depends on D1 to D3.

Check pin No.3 of the connector (CN105) to connect with a central monitor on the IO board (UP-0797).

- **D/A WAVE Check**



*** D/A WAVE CHECK ***

■ DC 0V
· DC +5V
· AC 60/30Hz
· PSEUDO PACING WAVE

On the above display,

↑ ↓: to select one waveform from three kinds of waveforms.

RETURN: to return to the COM BOARD CHECK MENU

Check the waveform at the test pin, "DA OUT".

1) DC 0V: 0 V is output at "DA OUT" for the D/A offset check. The offset must be ±10 mV or less.
2) DC+5V: 5 V d.c. is output for noise check. The noise must be ±10 mV or less.
3) AC 30Hz: 10 V p-p. a.c. (30Hz sine wave) is output for frequency characteristic check of delayed ECG ("MDW"). The amplitude of the 30Hz sine wave should be 7.0±0.4 V p-p. at the test pin "DHW".

4-4 Transmitter

When a new battery (more than 1.1 V should be output) is inserted into the transmitter, internal buzzer sounds approx. 1 sec. and operation starts.
When the transmitter is normally functioning, internal buzzer also sounds when "CALL" button is pressed.
If the internal buzzer continuously sounds or does not sound when the battery is inserted, the battery voltage is low or the transmitter is defective.

4-5 Receiver

Refer the self check of main unit.

Section 5 TROUBLESHOOTING

5-1 System Initialization 5.1

- 5-1-1 When Initialization Is Required 5.1
- 5-1-2 Initialization Procedure 5.2

5-2 Observed Malfunction Matrix 5.3

5-3 Error Code Malfunction Matrix 5.5

- 5-3-1 Error Status Indication 5.5
- 5-3-2 Error Code 5.6
- 5-3-3 Error Code List 5.7

5-4 Troubleshooting For Telemetry System 5.9

- 5-4-1 The Most Typical Trouble Sources 5.9
- 5-4-2 The Most Typical Symptom Actually Happened 5.9
- 5-4-3 Troubleshooting for 2 Cases in Section 5-4-2 .... 5.10

5-1 System Initialization

5-1-1 When Initialization Is Required

Initialize the instrument in the following cases.

- The system is locked-up due to CPU run away or any other reasons.
- The default setting is required.
- ROM is exchanged.
- The board is exchanged.

When the unit is initialized, the data and setting are as follows.

- All patient data is erased.
- The setting contents return to default condition.
- All error history is erased.
- Only data saved is date, time and language settings.

5-1-2 Initialization Procedure

1. Confirm that the power of the main unit is on.

SELF CHECK ○

2. Continue pressing the SELF CHECK key on the bedside monitor for about 3 sec until the screen disappears. DIAGNOSTIC CHECK AND SYSTEM SETUP screen is displayed.

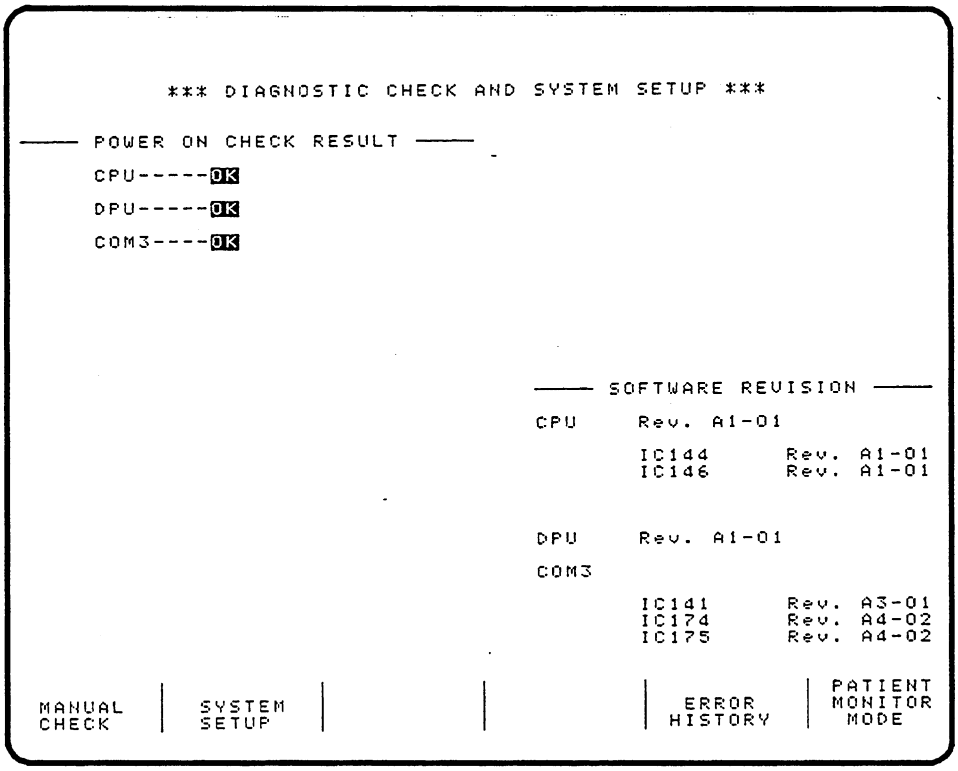
   OR

   When the main power is off, switching on the main power switch while pressing the SUSPEND key can also call up the DIAGNOSTIC CHECK AND SYSTEM SETUP screen.

REVIEW

3. Press the REVIEW key on the keypad. (The screen does not change.)

4. Press the "PATIENT MONITOR MODE" multi-function key. The following reverse shaded message "SYSTEM INITIALIZE" is displayed for 1sec and disappears. This operation finishes system initialization.



```
            *** DIAGNOSTIC CHECK AND SYSTEM SETUP ***

 ---- POWER ON CHECK RESULT ----
      CPU-----OK
      DPU-----OK
      COM3----OK




                                   ---- SOFTWARE REVISION ----
                                   CPU     Rev. A1-01
                                           IC144      Rev. A1-01
                                           IC146      Rev. A1-01

                                   DPU     Rev. A1-01
                                   COM3
                                           IC141      Rev. A3-01
                                           IC174      Rev. A4-02
                                           IC175      Rev. A4-02
```

5. Press the "PATIENT MONITOR MODE" multi-function key again to return the screen to the monitoring screen.

5-2 Observed Malfunction Matrix

Before replacing a doubtful Printed Circuit Board (PCB) to a malfunction according to the list, Check the following points as shown in the list.

A: Check patient cable and lead wires. Check electrodes at patient.
B: Check cable connection from patient to Main Unit (MU-881RA/RJ/RK).
C: Check patient cable, lead wires and electrodes.
D: Check to see if LOW mV or NOISE is being displayed on CRT.
E: Check if RESP OFF is selected on RESP SETUP display. Check cable connection from patient to Main Unit.
F: Check external interference and patient cable.
G: Check noise on respiration waveform after adjusting the respiration wave amplitude to be more than 4mm.
H: Check operation of blood pressure transducer.
I: Verify that zero is correct. Check the transducer.
K: Check temperature probe. Check cable connection from patient to Main Unit.
L: Check cable connection from patient to Main Unit. See operator's Manual for correct operation procedures.
M: Verify operation of recorder. Check cable connection from recorder to Main Unit.
N: Check connections between JJ and CNS. Verify that the communication indicator on JJ is lit for the connected CNS.
O: Check connections between JJ and BSM. Verify that the communication indicator on JJ is lit for the connected BSM.
P: Check the connection cable among units, such as the main unit, display unit and keypad
Q: Check whether the correct cables are connected to the input box.
R: Check the battery of the remote control.
S: Check the integrity speaker and its connection cables.
T: Check volume control for synchronizing tone.
U: Check the connections between the main unit and the display unit.
V: Check the main fuse.
W: Verify that the fan is connected.

BSM8800 MALFUNCTION CHECK LIST

MALFUNCTION		ERRONEOUS OPERATION	CPU BD UR-3027 Yellow	DPU BD UP-0670 Green	CRTC BD UP-0795 Red	COM3 BD QI-816P Black	I/O BD UP-0797 White	Power S.U. SC-018R	KEYPAD BD UR-3025	DISPLAY UNIT VD-881R	Input Box JA-880P	HEAD AMP XX-XXX	REMOTE CTRL RY-001P	NOTE
System Error	Constant LEADS OFF	1		3							4CC, 5AA	2DD		A
ECG	No ECG display	1		3							4BB	2DD		B
	Noisy ECG with HUM	1		5							3CC, 4AA	2DD		C
	HR=0 (ECG display OK)	1									3AA	2DD		D
RESP	No Resp. display	1		4							2AA, 5BB	3DD		E
	Artifact on Resp. wave	1		4							2AA	3DD		F
	No Resp. count	1									2AA			G
B.P.	No B.P. wave display	1		3							4BB	2EE		H
	B.P. value not correct	1		3								2EE		I
	Unable to auto–zero	1		3								2EE		H
TEMP	No Temp display			2							3BB	1FF		
	Temp value not correct	1		3								2FF		K
C.O.	C.O. not working	1		3							4BB	2GG		L
WS	No recorder operation	1				2								M
CNS/BSM	No communication with CNS/BSM	1				2	3							N
	No interbed ECG display	1		3		2								O
SWITCH	No key operation on Main Unit		3				2		1					P
	No key operation on Input Box			2							1CC, 3AA			Q
	No key operation on Remote Control		5				4			2LL, 3HH			1	R
SOUND	No sound generated		4		5		1			2HH, 3II				S
	No QRS sync tone	1	4	5			2			3HH, 6II				T
	No alarm sound		3				1			2HH, 4II				
	No LED or sound on Input Box			2							1CC, 3AA			
Display	No CRT display		5		2					1JJ, 3HH, 4KK				U
	Distorted display				2					1JJ, 3HH				
	Wave, character, or graph not normal				1									
POWER	Power lamp does not light	1						2						V
	Fan does not rotate							1						W
	60V fuse blows out							1						
OTHERS	Display changes to Self Check display from normal program display		1					3	2					

Note:
AA = JA I/F BD, UP-0270/0271
BB = JA MOTHER BD, UP-0762/0692
CC = JA OPERATION BD, UP-0693/0761
DD = ECG Head Amp, AC-800PA
EE = BP Head Amp, AP-800PA
FF = TEMP Head Amp, AM-800PA
GG = CO Head Amp, AH-800PA
HH = OPERATION CONTROL BD, UP-0801
II = OPERATION (VR) BD, UP-0802
JJ = CRT Unit
KK = Display Unit's Power Supply Unit, SC-019R
LL = LED BD, UP-0806

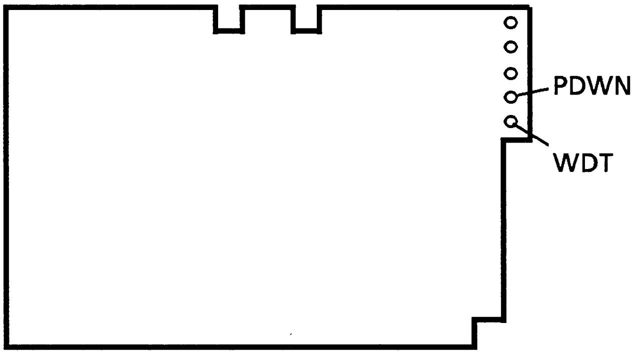
5-3 Error Code Malfunction Matrix

5-3-1 Error Status Indication

1) **Error indication on the CRT:** In an on-line Error, the Error code is indicated on the CRT while the error is registered on the ERROR HISTORY list.

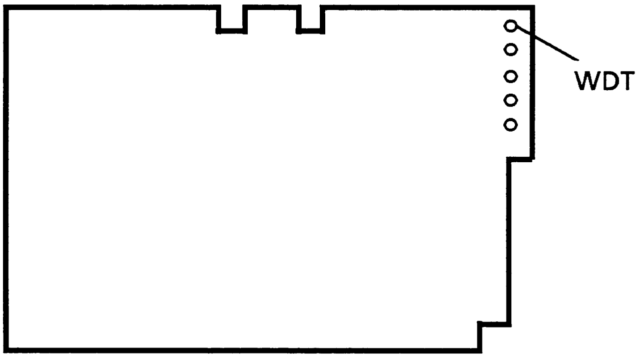
2) **Error indication on each board:** LEDs for WDT or PDWN (Power Down) are located and operate as follows.

◆ **CPU board, UR-3027**



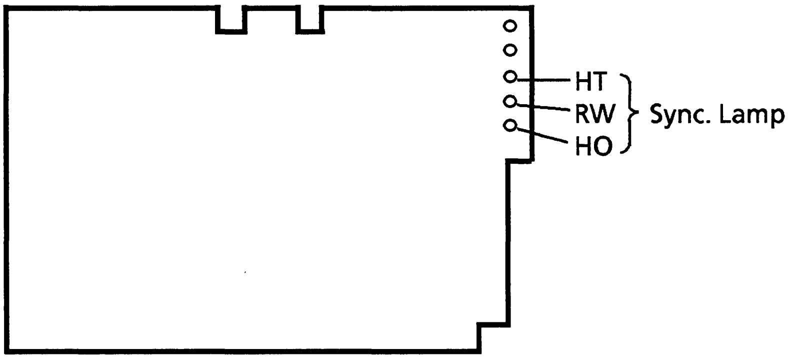
Status	WDT LED	PDWN LED
Normal	ON	ON
MPU Runaway/Stop	OFF	ON
Power down	OFF	OFF

◆ **COM3 board, UP-0563 (QI-816P)**



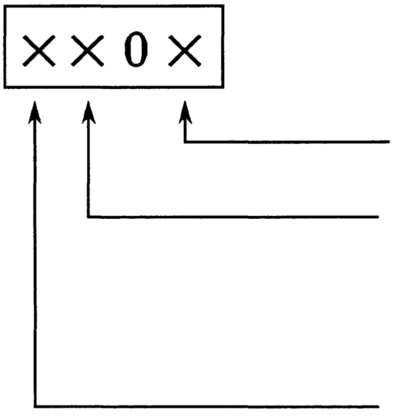
Status	WDT LED
Normal	ON
MPU Runaway/Stop	OFF

◆DPU board, UP-0670



5-3-2 Error Code

The error code is registered with a 4-digit hexadecimal number in ERROR HISTORY according to the following list if an error is found.



Error No.

Classification
- 0: Power ON Error
- 1: INT7 Error
- 3: Software Error (EXCEPTION)
- 4: Software Error (OS)

Board ID
- 1: CPU board
- 2: DPU board
- 3: COM3 board

NOTE

In case of software error, check CPU board for poor contact between ROM and ROM socket, connectors, or replace CPU board.

5-3-3 Error Code List

BSM8800 ERROR CODE LIST

ERROR CODE	CPU Board UR-3027 Yellow	DPU Board UP-0670 Green	CRTC Board UP-0795 Red	COM3 Board QI-816P Black	I/O Board UP-0797 White	Power Trans-former Unit SC-018R	KEYPAD RY-881P	DISPLAY UNIT VD-881R	Input Box JA-880P	HEAD AMP XX-XXX
POWER ON ERROR										
1001	1									
1002	1									
1004	1									
1005	1									
1006	2				1					
1009	1									
100A	3	1		2						
100B	2	1								
100D	2			1						
2001		1								
2002		1								
2006		1								
200A		1								
200E		1								
3001				1						
3002				1						
3004				1						
3006				1						
300A				1						

◆Error Code List by Board

● CPU Board

	Error code	Suspect area
Power on error	1001	ROM
	1002	RAM
	1004	71051
	1005	8279
	1006	72001
	1009	E^2PROM
	100A	Global Memory (DPU, COM3)
	100B	Communication (CPU-DPU)
	100D	Communication (CPU-COM3)

● DPU Board

	Error code	Suspect area
Power on error	2001	ROM
	2002	RAM
	2006	Timing Port
	200A	Global Memory
	200E	A/D-D/A

● COM3 Board

	Error code	Suspect area
Power on error	3001	ROM (on COM3)
	3002	RAM (on COM3)
	3004	8251
	3006	RTC
	300A	Global Memory

5-4 Troubleshooting For Telemetry System

In telemetry system, the most frequent trouble is no communication between transmitters and receivers, i. e., telemetry signals cannot be received.
Referring signal flow, do troubleshooting.

NOTE

Transmitter and receiver can not be adjusted locally. See Section 6 for details.

5-4-1 The Most Typical Trouble Sources

Transmitter side

1. Defect of analog circuit
2. Defect of coding/modulation system

Between transmitter and receiver

3. Defect from antenna of transmitter to antenna of receiver

Receiver side

4. Wiring trouble from antenna to splitter
5. Defect of splitter (ZA-003P)
6. Wiring trouble from splitter to receiver
7. Defect of receiver
8. Defect of DPU which controls the receiver
9. Wiring trouble for DPU board

5-4-2 The Most Typical Symptom Actually Happened

1. All waves cannot be received.
2. Telemetry signal can be received. However, waveform and/or status information is abnormal.

   Examples: a) Noise is superimposed on the wave.
   b) The shape of the wave is abnormal.
   c) NURSE CALL is displayed in spite of that CALL button is not pressed on the transmitter.

5-4-3 Troubleshooting for 2 Cases in Section 5-4-2

Since the troubleshooting procedures differ for 2 cases, they are explained separately as follows:

1. All waves cannot be received.
   There are several points to be checked as follows;
   (A) Defect of antenna system
      a) Poor installation of antenna system(Ex., Cut down of antenna cables)
      b) Wiring trouble between the main unit and the distributor of antenna system.
      c) Defect of distributor of antenna system
         In this case, when the transmitter is closely placed to the main unit, telemetry signal can be received.
      d) Power supply trouble to distributor of antenna system
   (B) Defect of main unit
      a) Defect of DPU board
      b) Power supply trouble to receiver

2. Telemetry signal can be received. However, waveform and/or status information is abnormal.
   Examples: a) Noise is superimposed on the wave.
      b) The shape of the wave is abnormal.
      c) NURSE CALL is displayed in spite of that CALL button is not pressed on the transmitter.

   Exchanging frequencies of receivers between the troubled one and normal one, check operation for both channels.
   If the symptom is transferred to the other channel, the probable trouble source is the transmitter.
   If the symptom still remains, the probable trouble source is DPU board.

Section 6 ADJUSTMENT

6-1 Main Unit 6.1

  6-1-1 Regulator Board, UP-0813 .... 6.1

    ◆ + 5 V Adjustment (VR101) 6.1

    ◆ Ampere Adjustment (VR102) : for operation of over current protection 6.1

  6-1-2 DPU Board, UP-0670 .... 6.1

    ◆ REF2.5 Adjustment (VR601) 6.1

    ◆ D/A and A/D Converter Adjustment (VR102 - VR105) 6.1

  6-1-3 CRTC Board, UP-0795 .... 6.2

    ◆ DCLK Adjustment (VC101) 6.2

  6-1-4 CPU Board, UR-3027 .... 6.2

    ◆ Real Time Clock Adjustment (VC101) 6.2

  6-1-5 COM3 Board, UP-0563 (QI-816P) 6.3

    ◆ REV2.5 Adjustment (VR104) 6.3

    ◆ D/A, A/D Converter Adjustment (VR-101 to VR-103) 6.3

  6-1-6 I/O Board, UP-0797 .... 6.3

    ◆ AUX 1 Offset (VR101) 6.3

    ◆ AUX 2 Offset (VR103) 6.3

    ◆ AUX 1 Gain (VR102) 6.3

    ◆ AUX 2 Gain (VR104) 6.3

6-2 Head Amplifier 6.4

  6-2-1 ECG Head Amp Board, UP-0272 .... 6.4

    ◆ ECG Gain Adjustment (VR001) 6.4

    ◆ ECG Gain Simplified Adjustment (VR001) 6.5

  6-2-2 Blood Pressure Head Amp Board, UP-0369 .... 6.6

    ◆ Blood Pressure Channel-1 (P1) Adjustment (VR001) 6.6

    ◆ Blood Pressure Channel-2 (P2) Adjustment (VR002) 6.6

  6-2-3 C.O. Head Amp Board, UP-0318 .... 6.7

    ◆ CO input Jig Adjustment 6.7

    ◆ Tb Adjustment (VR003/001) 6.8

    ◆ Ti Adjustment (VR002/004) 6.9

    ◆ ΔT Adjustment 6.10

6-2-4 Temp Head Amp Board, UP-0319 .... 6.11
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6-2-5 Thermister Resp Head Amp Board, UP-0548 .... 6.13
◆ Offset Adjustment(VR001) 6.13
6-2-6 CO_2 Head Amp Board, UP-0588 .... 6.13
◆ D/A Convertor Reference Adjustment(VR001) 6.13
6-2-7 O_2 Head Amp Board, UP-0592 .... 6.14
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6-3 Display Unit (Internal), VD-881R 6.16
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6-4 Display Unit (External), VD-881R 6.16
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1 Vertical Position 6.17
2 Vertical Size 6.17
3 Vertical Hold 6.17
4 Horizontal Position 6.17
6-5 Receiver Unit, ZR-800P 6.18
6-6 Transmitter 6.18

6-1 Main Unit

UP-0278 extension board is required in the adjustment of the Main Unit.

6-1-1 Regulator Board, UP-0813

◆ + 5 V Adjustment (VR101)

Adjust the VR101 to set 5.10 ± 0.01 V between test pin + 5 V and E2 without a load.

◆ Ampere Adjustment (VR102) : for operation of over current protection

Connect a load and a voltmeter in parallel between + 5 V and E2 and connect an ammeter in series with the load.

Adjust the VR102 for protecting the 5 V Switching Regulator Circuit against excessive current so that the 5 V starts to drop down at test pin + 5 V when the load current becomes 9 A.

6-1-2 DPU Board, UP-0670

◆ REF2.5 Adjustment (VR101)

Adjust the VR101 to set 2.500 V between test pin REF2.5 and AGND (E1).

◆ D/A and A/D Converter Adjustment (VR102 - VR105)

Call up A/D-D/A CHECK display on the CRT in the Manual Self Check program (refer to page 4.52 of this service manual).

(1) D/A OFFSET-1 (VR105)
  a) Select the check item No.1 (SELECT①) on the CRT.
  b) Press the START/STOP key to load the program.
  c) Adjust the VR105 to set 0.000 V at test pin DA.

(2) A/D GAIN-1 (VR103)
  a) Select SELECT② on the CRT.
  b) Press the START/STOP key to load the program.
  c) Adjust the VR103 to set 7D0H at A/D ADJ. GAIN on A/D-D/A ADJUST table.

(3) A/D OFFSET (VR102), A/D GAIN-2 (VR103)
- a) Adjust the VR102 to set 800H at A/D ADJ. 0V on the table.
- b) Repeat the adjustment procedure of (2)-c) or adjust the VR103 to set 7DOH on the table.
- c) Adjust VR102 again with the same procedure of a). After these adjustments, do no rotate VR102 and VR103.

(4) D/A GAIN (VR104), D/A OFF SET (VR105)
- a) Adjust the VR104 to set 7D0H at D/A ADJ. GAIN on the table.
- b) Adjust the VR105 to set 800H at D/A ADJ. 0V on the table.
- c) Adjust VR104 again with the same procedure of a).

(5) D/A-A/D LOOP
- a) Select SELECT③.
- b) Press the START/STOP key to load the program.
- c) Confirm that the OK mark is indicated next to the D/A-A/D LOOP CHECK title.

6-1-3 CRTC Board, UP-0795

◆ DCLK Adjustment (VC601)

Adjust the VC601 until there is no display distortion on the GRAPHIC DISPLAY CHECK SCREEN, and also WAVE DISPLAY CHECK screen.

6-1-4 CPU Board, UR-3027

◆ Real Time Clock Adjustment (VC101)

Adjust the VC101 so that a 1 Hz clock ±0.000011 is acquired between test pin TP10 and E2.

6-1-5 COM3 Board, UP-0563 (QI-816P)

◆ REV2.5 Adjustment (VR104)

Adjust the VR104 to set 2.5000 V between TP REF2.5 and AGND.

◆ D/A, A/D Converter Adjustment (VR-101 to VR-103)

Call up D/A WAVE CHECK display on the CRT in the Manual Self Check program (refer to page 4.51 of this service manual).

(1) D/A OFFSET-1 (VR-102)
Adjust the VR102 so that DC 0 V display on the screen indicates 0 V and the voltage at the test point DA OUT is 0 V ±10 mV.

(2) D/A GAIN-1 (VR-103)
Adjust the VR103 so that DC +5 V display on the screen indicates +5 V and the voltage at the test point DA OUT is 5 V ±10 mV.

(3) D/A OFFSET-2 (VR101)
Adjust the VR101 so that DC 0 V display on the screen indicates 0 V and the voltage at the test point MDW is 0 V ±100 mV.

6-1-6 I/O Board, UP-0797

◆ AUX 1 Offset (VR101)

Short pin No. 1 and 3 of the connector CN103. Adjust VR101 so that the voltage at test pin TPAUX1 is less than ±2 mV.

◆ AUX 2 Offset (VR103)

Short pin No. 2 and 3 of the connector CN103. Adjust VR103 so that the voltage at test pin TPAUX2 is less than ±2 mV.

◆ AUX 1 Gain (VR102)

Short test pin ±5 V and the individual input pins of connector CN103. Adjust VR102 so that the voltage at test pin TPGAIN1 is ±5.000 ±0.002 V.

◆ AUX 2 Gain (VR104)

Short test pin ±5 V and the individual input pins of connector CN103. Adjust VR104 so that the voltage at test pin TPGAIN2 is ±5.000 ±0.002 V.

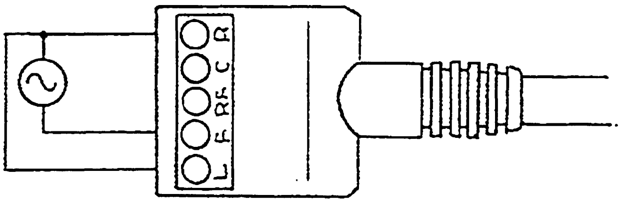
6-2 Head Amplifier

YS-008P3 extension board is required in the adjustment of the head amplifier.

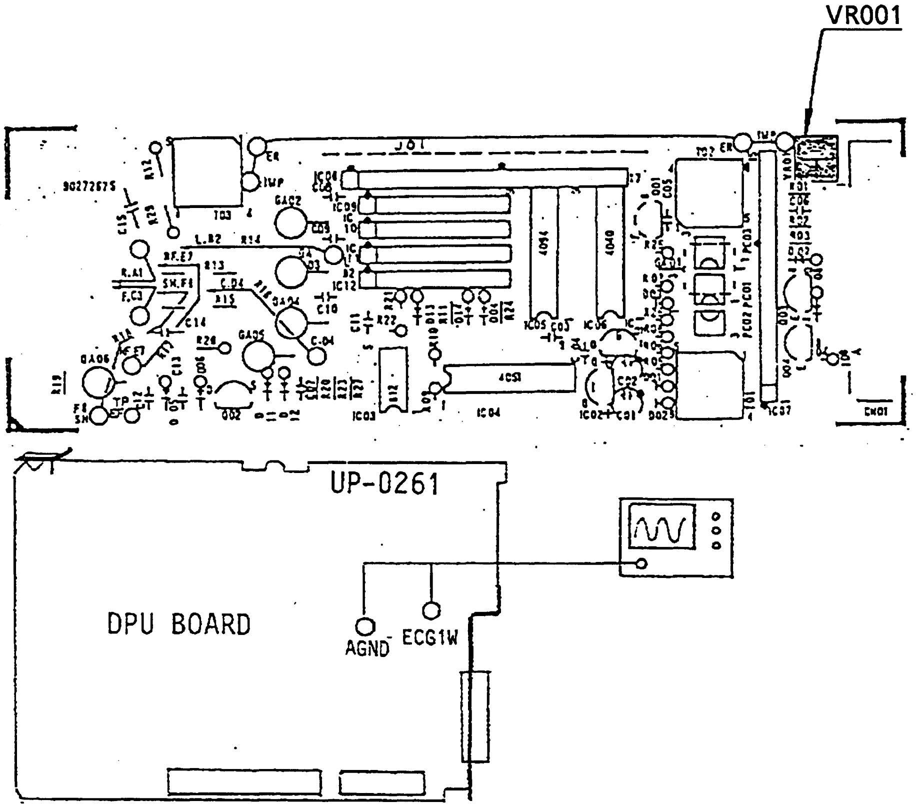
6-2-1 ECG Head Amp Board, UP-0272

◆ ECG Gain Adjustment (VR001)

1) Select Lead-Ⅱ of 3-electrode leads on the SETUP display.
2) Apply a 10 Hz sine wave (6 mVp-p) between R(RA) and F(LL) with an oscillator.

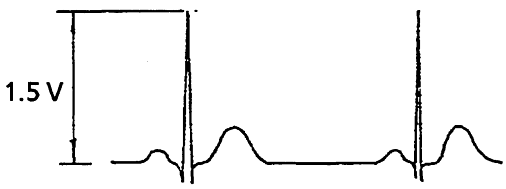


3) Adjust the VR001 on the board for 6 ± 0.3 Vp-p between test pin ECG1 W and AGND on the DPU board (UP-0670) with an oscilloscope.


VR001
J01
CN01
UP-0261
DPU BOARD
AGND
ECG1W

◆ECG Gain Simplified Adjustment (VR001)

1) Apply normal QRS (Mode: WAVE-1) to the ECG input connector with the vital signs simulator, AX-800P.
2) Press the ECG LEAD key to select Lead-Ⅱ
3) Adjust the VR001 for a 1.5 V amplitude of the R-wave at the ECG OUT connector on the front panel with an oscilloscope.



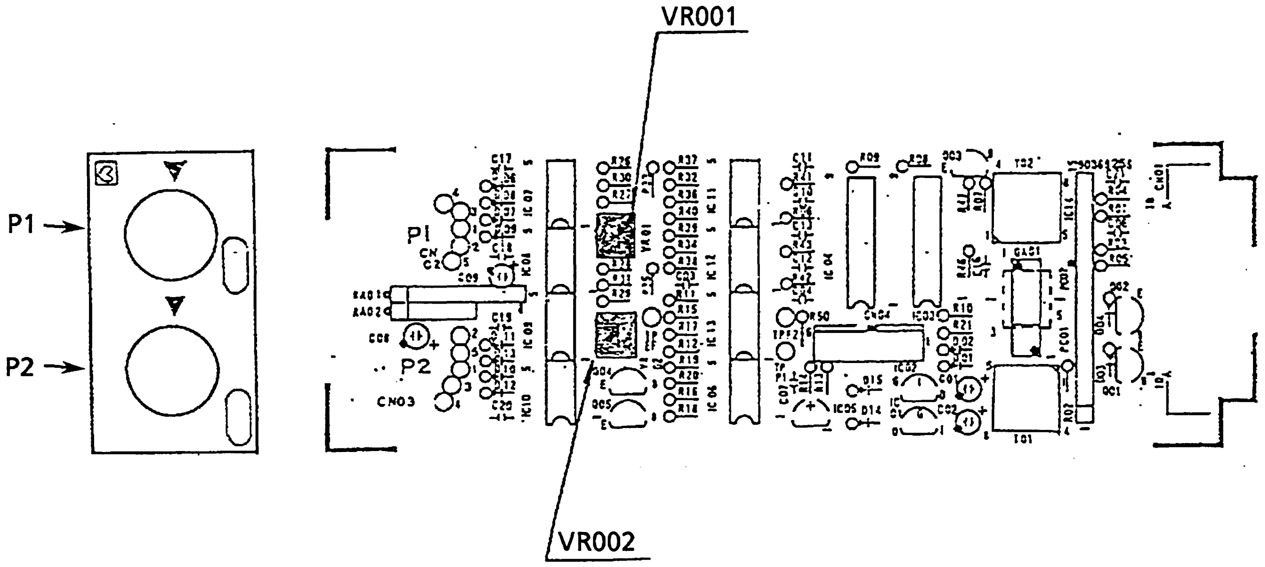
6-2-2 Blood Pressure Head Amp Board (AP-851PA), UP-0369

◆ **Blood Pressure Channel-1 (P1) Adjustment (VR001)**

1) Connect the P1 output of the AX-800P to the P1 input connector on the head amplifier (AP-800PA).
2) Apply 0 mmHg (Mode: 2) to the P1 input connector with the AX-800P.
3) Zero a P1 value on a blood pressure waveform display by pressing the BP1 ZERO key on the operation panel of the input box.
4) Applying 200 mmHg (Mode: 4) to the P1 input connector with the AX-800P.
5) Adjust the VR001 to indicate 200 mmHg (P1 value) on the B.P. Display.

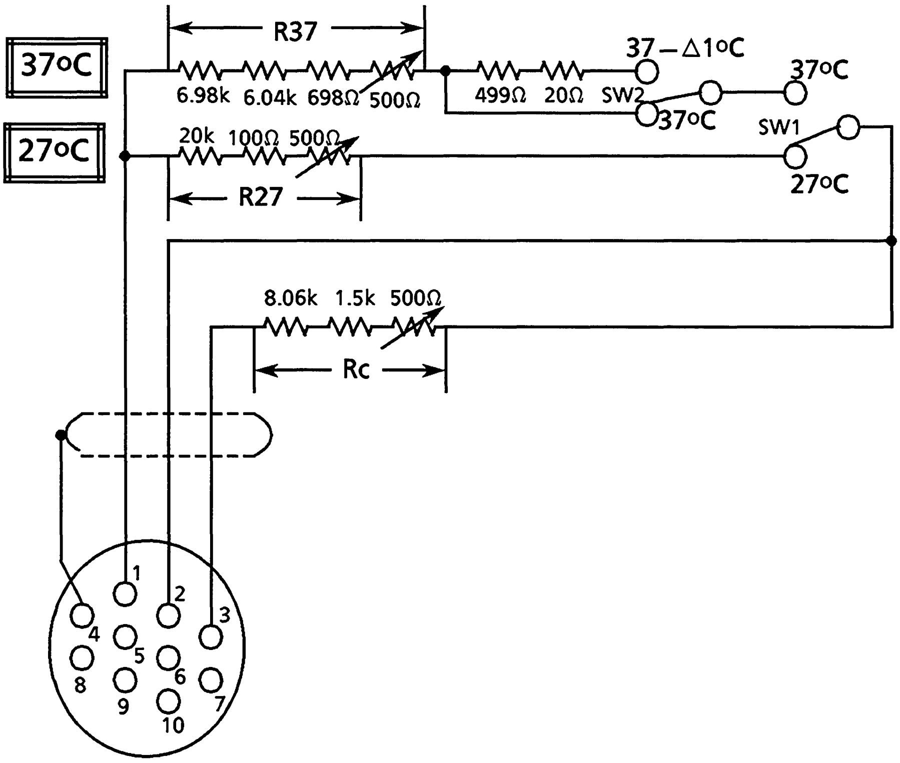
◆ **Blood Pressure Channel-2 (P2) Adjustment (VR002)**

1) Connect the P1 output of the AX-800P to the P2 input connector.
2) Apply 0 mmHg (Mode: 2) to the P2 input connector with the AX-800P.
3) Zero the P2 value on the B.P. Display by pressing the BP2 ZERO key.
4) Apply 200 mmHg (Mode: 4) to the P2 input connector.
5) Adjust the VR002 to indicate 200 mmHg (P2 value) on the B.P. Display.



6-2-3 CO Head Amp Board, UP-0318

The CO Head Amp board should be adjusted with not only the Vital Signs Simulator (AX-800P) but also the following special CO Input Jig.


37oC
27oC
R37
6.98k 6.04k 698Ω 500Ω
499Ω 20Ω
37−Δ1oC
37oC
SW2
37oC
SW1
20k 100Ω 500Ω
R27
27oC
8.06k 1.5k 500Ω
Rc
1
2
3
4
5
6
7
8
9
10

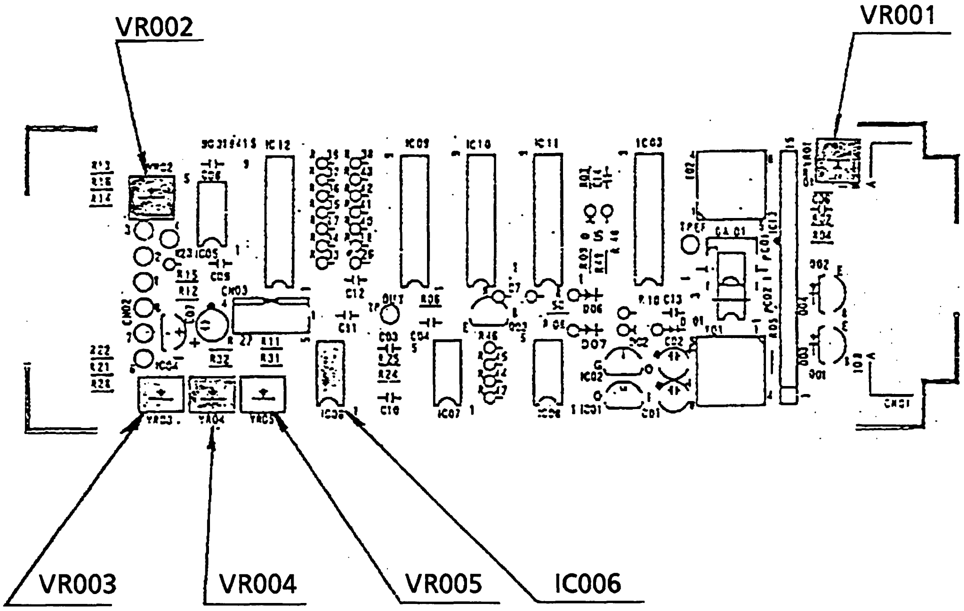
NOTE

All the above resistors are F-type resistors.

◆ **CO input Jig Adjustment**

Adjust each variable resistor (500 Ω) of R27, R37 and Rc to be the following values with a digital voltmeter (Valid digits: 4 and 1/2 or more).

R27: 20.359 kΩ ± 5 Ω
R37: 13.999 kΩ ± 5 Ω
Rc: 9.755 kΩ ± 5 Ω



◆ **Tb Adjustment (VR003/001)**

1) Put a CO Head Amplifier (AH-800PA) into the slot farthest from the JAInterface unit (QI-802P) of the input box.
2) Call up the DEBUG PROGRAMdisplay by pressing the DISPLAY key and ALARM LIMIT key on the Main Unit simultaneously.
3) Select Item-7, A/D TEST PROGRAM, on the display.
4) Apply 27° C to the CO input connector on AH-800PA with the CO Input Jig.
5) Adjust the VR003 to indicate 800 ± 1(H) at the crossing point of CH#8 and TS6 on the A/D TEST PROGRAM display.

[A/D TEST PROGRAM DISPLAY]

AD TEST	TS1 TS2 TS3 TS4 TS5	TS6	TS7 TS8
CH#1 ⋮		↓	
CH#8	------------------→	800 801	
⋮ CH#12			

6) Apply 37° C to the CO input connector on AH-800PA with the CO Input Jig.
7) Adjust the VR001 to indicate B20 ± 1(H) at the crossing point of CH#8 and TS6 on the display.

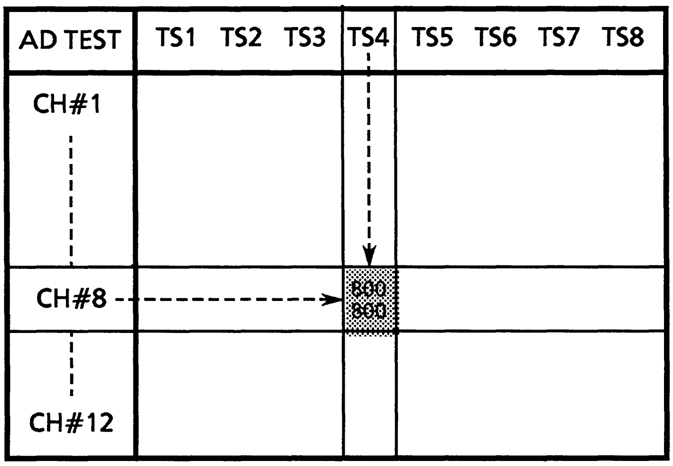
◆ Ti Adjustment (VR002/004)

NOTE

Execute Ti Adjustment only after finishing Tb Adjustment.

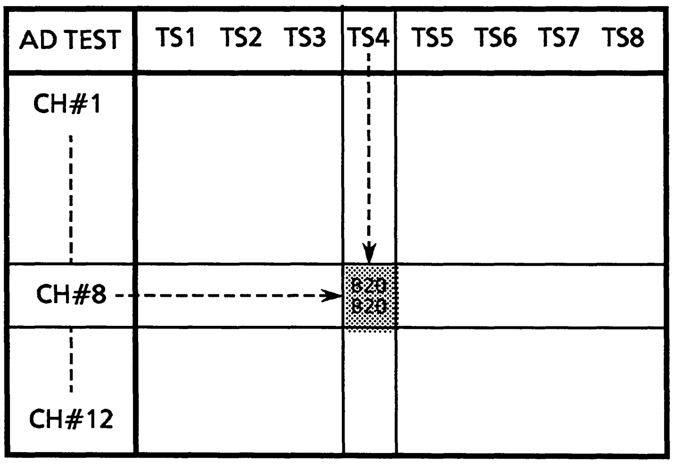
1) Apply 0° C(Mode: 1) to the CO input connector with the AX-800P.
2) Call up the A/D TEST PROGRAM display.
3) Adjust the VR002 to indicate 800 ± 1(H) at the crossing point of CH#8 and TS4 on the display.

[A/D TEST PROGRAM DISPLAY]


AD TEST
TS1 TS2 TS3 TS4 TS5 TS6 TS7 TS8
CH#1
CH#8
800
800
CH#12

4) Apply 20° C(Mode: 3) to the CO input connector with the AX-800P.
5) Adjust the VR004 to indicate B20 ± 1(H) at the crossing point of CH#8 and TS4 on the display.

[A/D TEST PROGRAM DISPLAY]


AD TEST
TS1 TS2 TS3 TS4 TS5 TS6 TS7 TS8
CH#1
CH#8
B20
B20
CH#12

◆ ΔT Adjustment

NOTE

Execute ΔT Adjustment only after finishing Tb and Ti Adjustment.

1) Execute CO START on the CO MEASURE screen after applying 37° C to the CO input connector with the CO Input Jig.
2) Measure the voltage at Pin-6 and Pin-7 on IC006B.
   The voltage at Pin-6: $E_{37\text{⑥}}$
   The voltage at Pin-7: $E_{37\text{⑦}}$
3) Measure the voltage at Pin-6 and Pin-7 on IC006B after setting the switch (SW2) on the CO Input Jig to $37-\Delta1$°C.
   The voltage at Pin-6: $E_{\Delta1\text{⑥}}$
   The voltage at Pin-7: $E_{\Delta1\text{⑦}}$
4) Adjust the VR005 for the following equation.
   $E_{37\text{⑦}}-E_{\Delta1\text{⑦}}=-10\ \mathrm{X}\ (E_{37\text{⑥}}-E_{\Delta1\text{⑥}})$

Reference

Output voltages to Tb and Ti of the calibrated AH-800PA are shown as follows:

Tb Temperature(°C)	Tb Output Voltage
22	−0.955 V
37	+2.000 V
45	+3.612 V

Ti Temperature(°C)	Ti Output Voltage
0	0 V
10	+0.995V
20	+2.012 V

Relation between Tb and Thermistor Resistance in catheter (Rb) is shown as follows:

Tb	Rb(Ω)	Tb	Rb(Ω)	Tb	Rb(Ω)	Tb	Rb(Ω)	Tb	Rb(Ω)	Tb	Rb(Ω)
15	32871	21	25760	26	21161	31	17481	36	14519	41	12123
16	31544	22	24755	27	20359	32	16837	37	13999	42	11700
17	30277	23	23795	28	19591	33	16220	38	13500	43	11294
18	29068	24	22877	29	18857	34	15629	39	13022	44	10905
19	27914	25	22000	30	18154	35	15062	40	12563	45	10531
20	26813										

Relation between Ti and Thermistor Resistance in Injection Temperature Probe (Ri) is shown as follows:

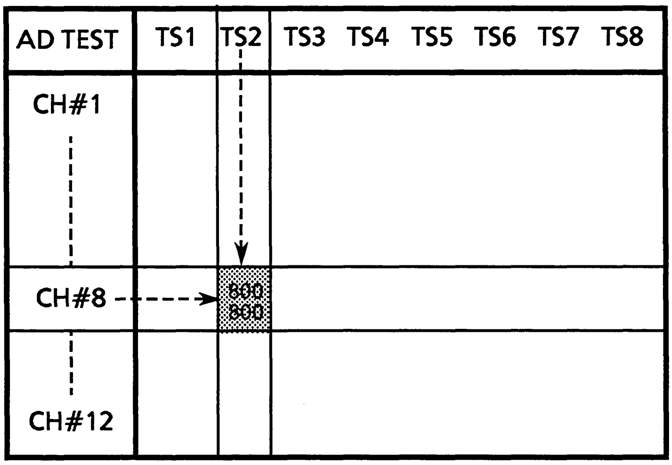
Ti	Ri(kΩ)	Ti	Ri(kΩ)	Ti	Ri(kΩ)	Ti	Ri(kΩ)
0	257.58	7	187.04	14	137.59	21	102.48
1	245.87	8	178.87	15	131.83	22	98.349
2	234.75	9	171.11	16	126.33	23	94.408
3	224.20	10	163.73	17	121.09	24	90.648
4	214.18	11	156.70	18	116.10	25	87.057
5	204.67	12	150.02	19	111.34	26	83.628
6	195.63	13	143.65	20	106.10	27	80.352

6-2-4 Temp Head Amp Board, UP-0319

◆ REF0 Adjustment (VR002)

1) Put a Temperature Head Amplifier (AW-800PA) into the slot farthest from the QI-802P/815P.
2) Call up A/D TEST PROGRAM display. Refer to the section 6-2-3 Tb Adjustment.
3) Adjust the VR002 to indicate 800 ± 1(H) at the crossing point of CH#8 and TS2.

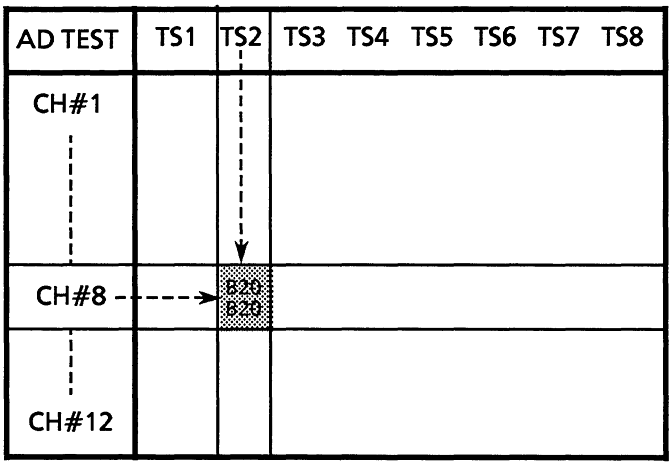
[A/D TEST PROGRAM DISPLAY]


AD TEST
TS1
TS2
TS3
TS4
TS5
TS6
TS7
TS8
CH#1
CH#8
CH#12
800
800

◆ CAL37 Adjustment (VR001)

Adjust the VR001 to indicate B20 ± 1(H) at the crossing point of CH#8 and TS2.

[A/D TEST PROGRAM DISPLAY]


AD TEST
TS1
TS2
TS3
TS4
TS5
TS6
TS7
TS8
CH#1
CH#8
CH#12
B20
B20

◆ T1, T2 Verification

Verify that Errors of T1 value or T2 value are within ±0.1° C on a normal operating display when 22, 37, or 45° C signal is applied to the input connectors (T1 or T2) on the AW-800PA.

Reference

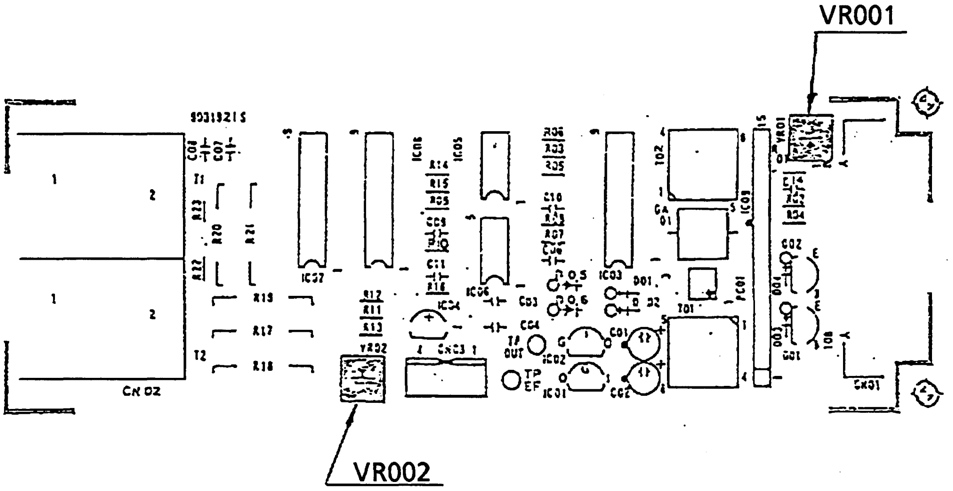
Output voltages to T1 or T2 of the calibrated AW-800PA are shown as follows:

Temperature (T1 or T2)	Output Voltage (T1 or T2)
22 °C	−0.950 V
37 °C	+2.000 V
45 °C	+3.590 V

The relation between temperature (T) and thermistor resistance (Rt) in Temperature Probe (YSI-400) is shown as follows:

T	Rt	T	Rt	T	Rt	T	Rt	T	Rt
0	7355	10	4483	20	2814	30	1815	40	1200
1	6990	11	4273	21	2690	31	1740	41	1153
2	6645	12	4075	22	2572	32	1668	42	1108
3	6319	13	3887	23	2460	33	1599	43	1065
4	6011	14	3708	24	2354	34	1534	44	1024
5	5720	15	3539	25	2253	35	1471	45	984.2
6	5444	16	3379	26	2156	36	1412		
7	5184	17	3226	27	2065	37	1355		
8	4937	18	3082	28	1977	38	1301		
9	4704	19	2944	29	1894	39	1249		

NOTE
T (°C)
Rt (Ω)



6-2-5 Thermister Resp Head Amp Board, UP-0548

NOTE

When IC005 or VR001 is replaced, offset adjustment (VR001) is required.

◆ **Offset Adjustment(VR001)**

1) Connect the respiration pickup to the respiration head amplifier.
2) Measure voltage with a digital voltmeter across the pin-29 (CH7W/RW) and pin-33 (GND) of the CNS connector(or WS connector) on the rear of the MU-802R bedside monitor main unit.
3) Adjust the VR001 so that the voltmeter reads DC ±10 mV.

6-2-6 CO_2 Head Amp Board, UP-0588

NOTE

When the D/A convertor IC002 is replaced, the D/A Converter Reference Adjustment (VR001) is required.

◆ **D/A Converter Reference Adjustment(VR001)**

1) Read DC voltage across the TP E1(analog ground) and IC008 pin-8 with a digital voltmeter.
2) Disconnect the CO_2 sensor and adjust the VR001 so that the voltmeter reads -4.8 V ± 0.01 V.

6-2-7 O_2 Head Amp Board, UP-0592

NOTE

When the IC009 or IC010 is replaced, this offset adjustment (VR001 and VR002) is required.

◆ **Offset Adjustment(VR001, VR002)**

1) Insert the O_2 head amplifier into the last slot of the input box.
2) Call up the A/D Test Screen of the bedside monitor main unit.
3) Shorten the input connector pins 2, 3, and 5 to the pins 1 and 4 (EF: floating ground) and adjust each volume so that Test pins TS6 and TS8 becomes within ±10mV of REFO.

Reference

TS2 value and TS4 value of #5 (O_2) lines in the table indicate REF0V voltage. TS6 value indicates the offset voltage of IC009. TS8 indicates the offset voltage of IC010.

Unit of the value is mV and upper numerals show maximum value and lower numerals show minimum value in one second.

AD TEST	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8
CH#1 (ECG1)	•••••	5117 5117	•••••	5117 5117	•••••	5117 5117	•••••	5117 5117
CH#2 (ECG2)		-10 2		-10 2		-10 5		-10 5
CH#3 (RESP)		0 7		-2 7		0 10		-2 7
CH#4 ( )	•••••	5 12	•••••	5 12	•••••	7 12	•••••	-15 -10
CH#5 (02)	•••••	-4870 -4865	•••••	-4870 -4865	•••••	-4875 -4870	•••••	-4872 -4865
CH#6 ( )	•••••	2 10	•••••	2 7	•••••	2 10	•••••	2 10
CH#7 ( )	5 12	5 10	2 10	5 10	5 12	2 7	7 12	5 12
CH#8 ( )	5 10	5 10	7 10	5 10	5 12	5 10	5 12	2 10
CH#9 ( )	-17 -10	17 22	-12 -5	17 22	10 15	5 10	8 12	5 10
CH#10 ( )	2 7	2 7	2 10	2 7	5 10	2 7	5 10	2 10
CH#11(PARA)	97 102	5020 5025	457 462	5020 2025	5017 5022	5020 5025	5017 5022	5020 5025
CH#11( )	0 2	-5030 -5027	-2515 -2512	2 2	2512 2515	5027 5030	5020 5022	2 2
HEAD AMP INSTALLED	ECG	•••••	O_2	•••••	•••••	•••••	•••••	•••••

6-2-8 NIBP Head Amp Sub Board (AP-860PA), UP-0630

NOTE

This adjustment is for the NIBP Head Amplifier AP-860PA only.

◆ Pressure Zero Adjustment(VR201)

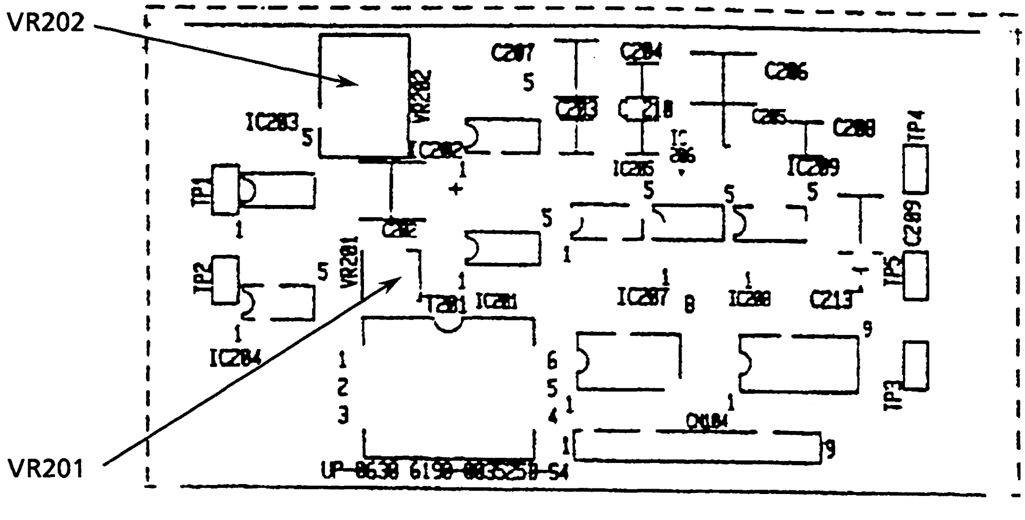
1) Disconnect the double air hose from the NIBP connectors on the NIBP head amplifier.
2) Adjust the VR201 to set 0 V ±10 mV between test pin TP5 and AGND.

◆ Pressure Gain Adjustment(VR202)

1) Call up NIBP AMP CHECK (AP-860P) display on the CRT in the Manual Self Check program (refer to page 4.47 of this service manual).
2) Select the check item No. 1, CALIBRATION (1), or No. 2, CALIBRATION (2).
3) Connect the external pump and manometer to the two NIBP connectors on the NIBP head amplifier.
4) Increase the pressure until the reading on the manometer reads 300 mmHg.
5) Adjust the VR202 to set the pressure reading on the NIBP AMP CHECK (AP-860P) display to read 300 mmHg ±1 mmHg.

NOTE

The bedside monitor automatically carries out the zero calibration every time the NIBP AMP CHECK (AP-860P) display is called up. Therefore, exit the NIBP AMP CHECK (AP-860P) display and call up the NIBP AMP CHECK (AP-860P) again every time the NIBP head amplifier is replaced during this check mode.


VR202
VR201
VR202
IC203
IC202
C207
C204
C206
C203
C218
C205
C208
IC205
IC209
TP4
TP1
C202
C209
TP2
VR201
T201
IC201
IC207
IC208
C213
TP5
IC204
TP3
CN104
UP-0630 6190-0035250-S4

6-3 Display Unit (Internal), VD-881R

6-3-1 Power Supply Unit Board, SC-019R

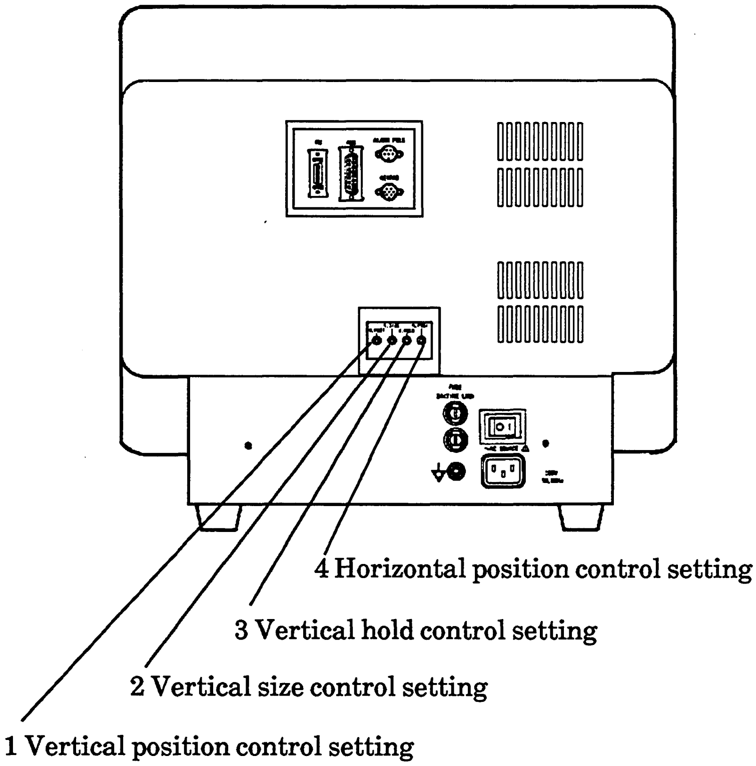
◆ **+5V Adjustment (VR101)**

Adjust the VR101 to set 5.10 V ±0.01 V between the test pin +5 V and E2 without a load.

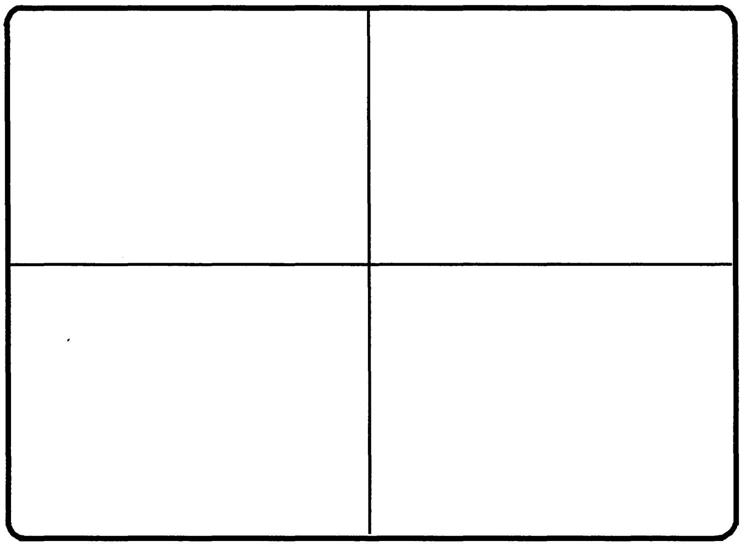
6-4 Display Unit (External), VD-881R

6-4-1 Display Unit's Rear Panel Adjustment Knob

Rear Panel


4 Horizontal position control setting
3 Vertical hold control setting
2 Vertical size control setting
1 Vertical position control setting

Call up the following screen of the GRAPHIC DISPLAY CHECK screen in the CRTC CHECK mode.



1 VERTICAL. POSITION

Adjust the V.POSI KNOB so that the left and right margins on the CRTC CHECK screen shown on the previous page are equal.

2 Vertical Size

This is to adjust the gain along the Y–axis. Adjust the V.SIZE knob so that the image on the screen is the same as the CRTC CHECK screen shown on the previous page.

3 Vertical Hold

If the image on the screen continuosly sweeps along the Y–axis, adjust the V. HOLD knob until the CRTC CHECK screen shown on the previous page appears stationary.

4 Horizontal Position

Adjust the H. POSI knob so that the upper and bottom margins on the CRTC CHECK screen shown on the previous page are equal.

6-5 Receiver Unit, ZR-800P

Do not perform the adjustment locally. The reason is as follows;

For the adjustment of this block, a personal computer, the related special software, shield room, high-frequency spectrum analyzer etc. are essential and it is out of level of the field service.
NIHON KOHDEN does not provide above device and information.
If the adjustment should perform locally without above facility, the specification can not be guaranteed.

6-6 Transmitter

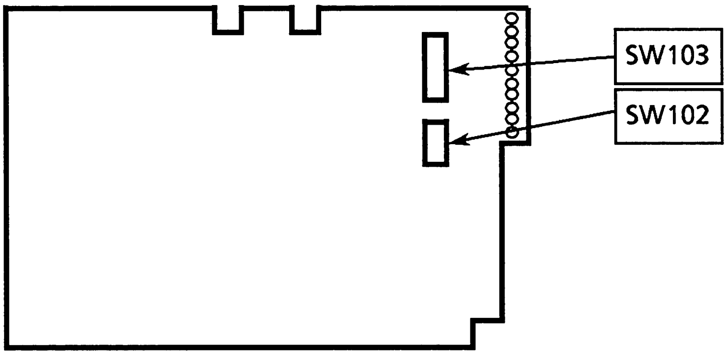
The same situation as above.

Section 7 INTERNAL SWITCH AND JUMPER SETTING

7-1 Main Unit, MU-881R 7.1
    7-1-1 CPU Board, UR-3027 ..... 7.1
    7-1-2 DPU Board, UP-0670 ..... 7.2
    7-1-3 COM3 (QI-816P) Board, UP-0563 ..... 7.3
    7-1-4 I/O Board, UP-0797 ..... 7.4
7-2 Display Unit, VD-881R 7.5
    7-2-1 OPERATION CONTROL Board, UP-0801 ..... 7.5
7-3 Keypad, RY-881PA 7.6
    7-3-1 OPERATION Board, UR-3025 ..... 7.6

7-1 Main Unit, MU-881R

7-1-1 CPU Board, UR-3027



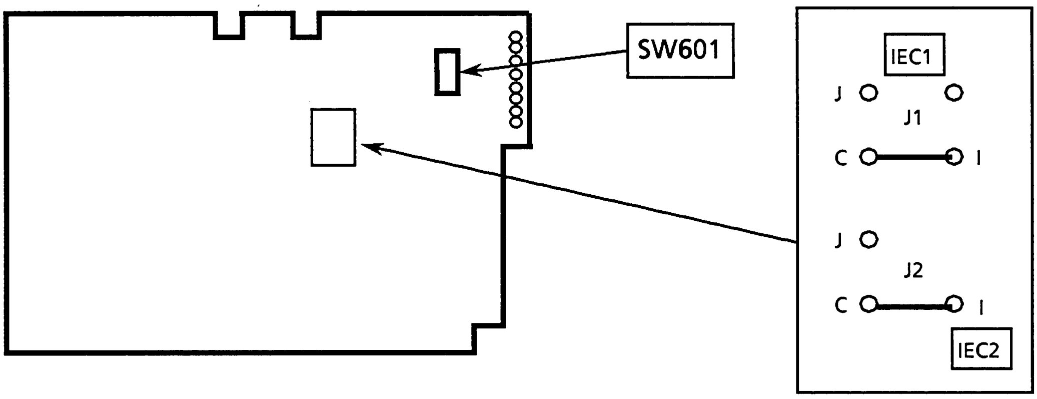
DIP Switch SW102

Bit	Function	Initial setting
1	Not used	OFF
2	Not used	OFF
3	Not used	OFF
4	ON : Watch dog timer does not function	OFF

DIP Switch SW103

Bit	Function	Initial setting
1	Not used	OFF
2	Not used	OFF
3	Not used	OFF
4	Not used	OFF
5	Not used	OFF
6	Not used	OFF
7	ON: Use for additional RAM	OFF
8	ON: Use in debug mode	OFF

7-1-2 DPU Board, UP-0670



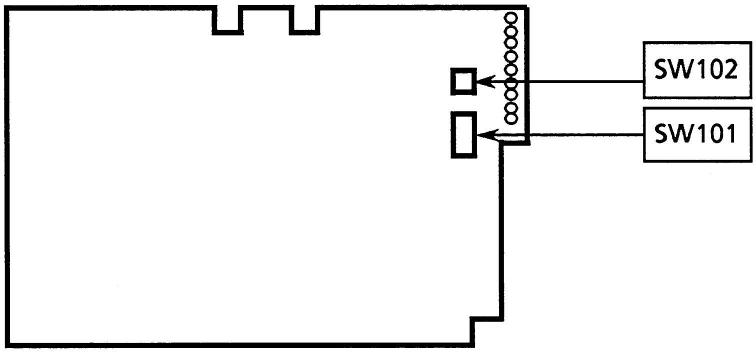
DIP Switches,SW601

Bit	Function	Initial setting
1	Telemetry channel selection (ON : USA ; OFF : Others)	ON
2	Not used	OFF
3	Not used	OFF
4	Not used	OFF

Jumpers J1 & J2: Shorted by wire

Jumper	Function	Initial setting
J1	Filter characteristics (I–C:IEC ; J–C:Japan standard)	I–C
J2	See the circuit diagram of UP-0670 18/19	I–C

7-1-3 COM3 (QI-816P) Board, UP-0563



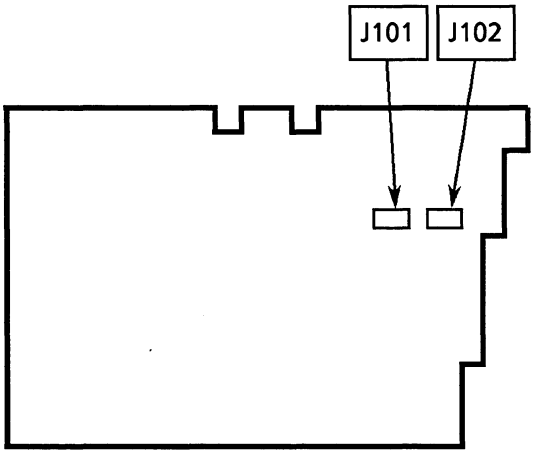
DIP Switch, SW101

Bit	Function	Initial setting
1	Not used	OFF
2	Not used	OFF
3	Not used	OFF
4	Not used	OFF
5	Not used	OFF
6	Not used	OFF
7	Not used	OFF
8	Not used	OFF

DIP Switch, SW102

Bit	Function	Initial setting
1	SYSTEM (Normal operating mode : ON , Debug mode : OFF	ON
2	WDTRST (Reset with WDT Error : ON/OFF)	OFF
3	WDTINT (Interrupt Request from WDT : ON/OFF)	ON
4	SWWDT (Software WDT Function : ON/OFF)	ON

7-1-4 I/O Board, UP-0797

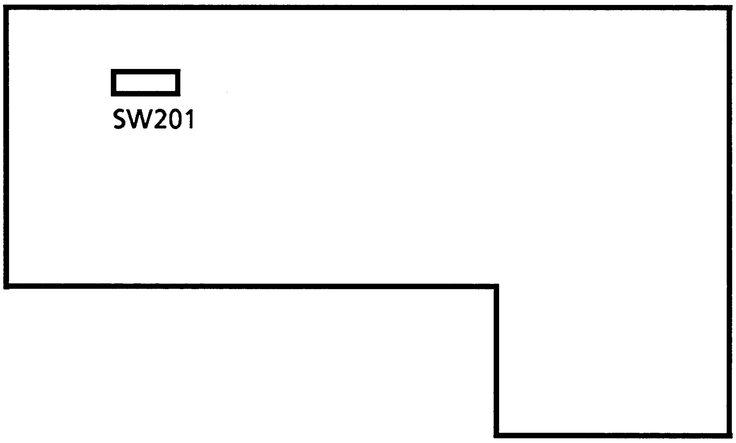


Jumpers J101 & J102: Shorted by wire

Jumper	Function	Initial setting
J101	AUX1W Gain select Short : ×1 Open : ×5	Short
J102	AUX2W Gain select Short : ×1 Open : ×5	Short

7-2 Display Unit, VD-881R

7-2-1 OPERATION CONTROL Board, UP-0801

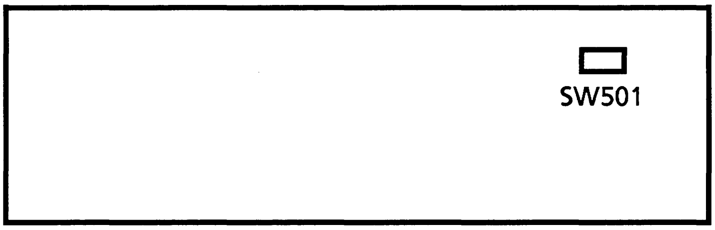


Dip switch SW201

Bit	Function	Initial setting
1	ON : Baud rate is 9600bps	OFF
2	ON : Alarm pole goes on and off (HT Sync)	OFF
3	Not used	OFF
4	Not used	OFF

7-3 Keypad, RY-881PA

7-3-1 OPERATION Board, UR-3025



Dip switch SW501

Bit	Function	Initial setting
1	ON : Baud rate is 9600bps	OFF
2	Not used	OFF
3	Not used	OFF
4	Not used	OFF

Section 8 CONNECTOR PIN ASSIGNMENT

8-1 Main Unit, MU-881R 8.1

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  - 6) CNS Connector 8.5
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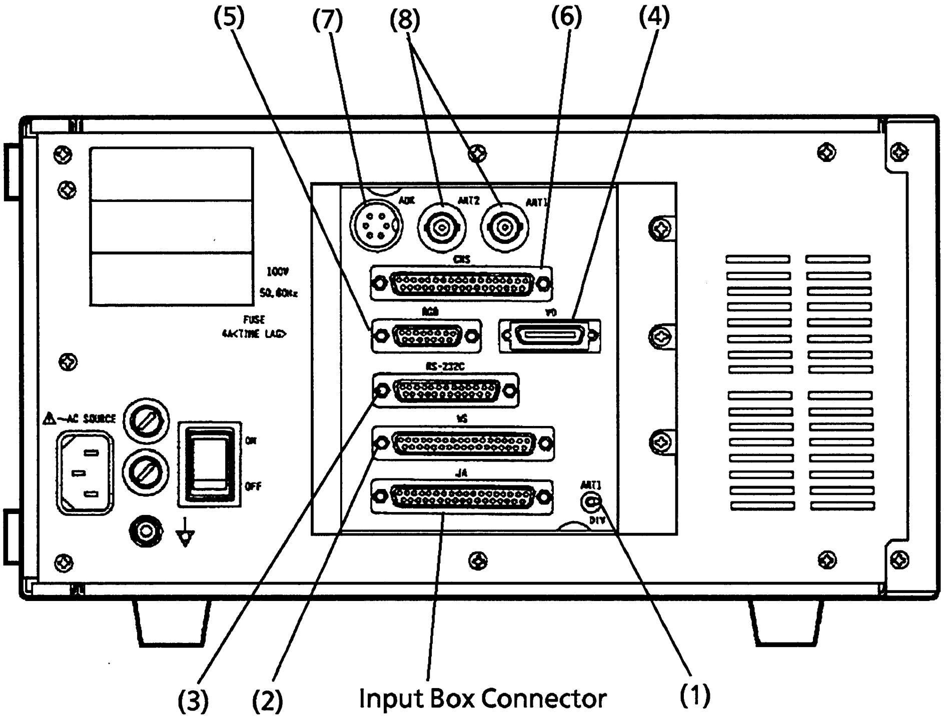
8-1 Main Unit, MU-881R

8-1-1 External Connectors and Switches on the Main Unit

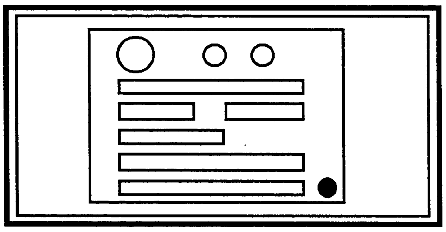
(See Section 1-8 CONNECTION DIAGRAM, and Section 2. SIGNAL LIST.)

Rear Panel


(5)
(7)
(8)
(6)
(4)
AUX
ANT2
ANT1
CNS
100V
50,60Hz
FUSE
4A<TIME LAG>
RCB
I/O
RS-232C
⚠~AC SOURCE
ON
OFF
VS
J4
ANT1
DIV
(3)
(2)
Input Box Connector
(1)

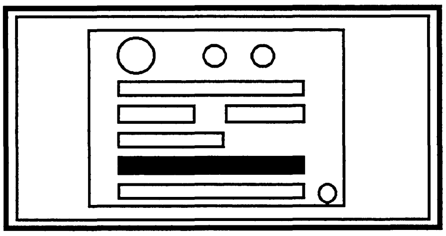
1) Antenna Selector Switch

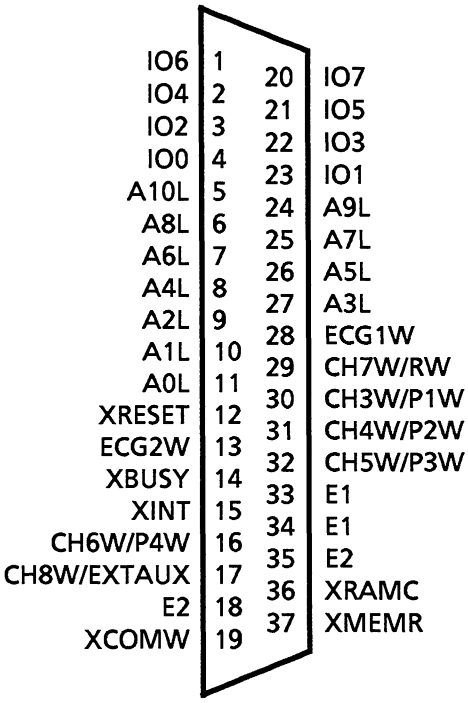
Model: ATE1D-6M3-10
Part No: 317319
Function: Selects the antenna operation; ANT 1 or Diversity



2) WS Connector

Circuit No.:	CN103
Model:	RDCD-37SE-LNA, Female
Part No.:	081092
Mating Type:	D Sub 37P Male Connector
Mating Connector:	BSM-WS Connector Cable
Part No.:	YS-015P3 (for WS-840R/841R) 367844 (for WS-880R)

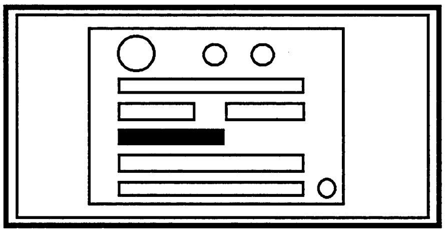


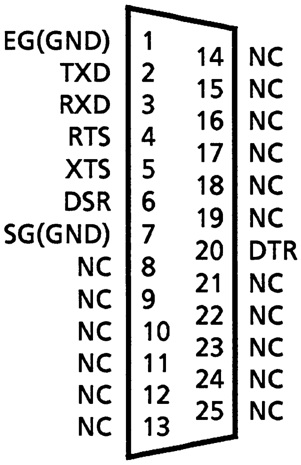

IO6 1
IO4 2
IO2 3
IO0 4
A10L 5
A8L 6
A6L 7
A4L 8
A2L 9
A1L 10
A0L 11
XRESET 12
ECG2W 13
XBUSY 14
XINT 15
CH6W/P4W 16
CH8W/EXTAUX 17
E2 18
XCOMW 19
20 IO7
21 IO5
22 IO3
23 IO1
24 A9L
25 A7L
26 A5L
27 A3L
28 ECG1W
29 CH7W/RW
30 CH3W/P1W
31 CH4W/P2W
32 CH5W/P3W
33 E1
34 E1
35 E2
36 XRAMC
37 XMEMR

Construction of D Sub 37P Male Connector			Model	Part No.
Connector	Caulked Type	Housing	CDC-37P	080404
		Contact Pin	CD-PC-121	080431
	Souldered Type		HDCD-37P	080725
Case			HDC-CTH1	080672

3) RS-232C Connector

Circuit No.:	CN103
Model:	RDBD-25SE-LNA, Female
Parts No.:	081109
Mating Type:	D Sub 25P Male Connector

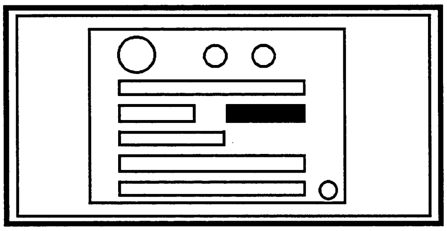



EG(GND) 1
TXD 2
RXD 3
RTS 4
XTS 5
DSR 6
SG(GND) 7
NC 8
NC 9
NC 10
NC 11
NC 12
NC 13
14 NC
15 NC
16 NC
17 NC
18 NC
19 NC
20 DTR
21 NC
22 NC
23 NC
24 NC
25 NC

Construction of D Sub 25P Male Connector			Model	Part No.
Connector	Caulked Type	Housing	CDB-25P	080413
		Contact Pin	CD-PC-121	080431
	Souldered Type		HDBB-25P	080779
Case			HDB-CTH1	080663

4) VD Connector

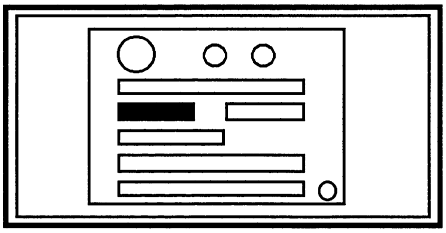
Circuit No.:	CN102
Model:	DX10M-26SE
Parts No.:	354359
Mating Connector :	VD Connector Cord
Part No.:	YS-023P8 (1.5 m) YS-024P5 (3 m) YS-025P2 (10 m)



R	1	14	HSYNC
RGND	2	15	VSYNC
G	3	16	TxD1
GGND	4	17	RxD1
B	5	18	XRESET1
BGND	6	19	XHT
	7	20	TxD2
GND	8	21	RxD2
	9	22	XP.SXTL2
ALSNDGND	10	23	MIS SEL
ALSND	11	24	READY
HTSNDGND	12	25	XRESET2
HTSND	13	26	

5) RGB Output Connector

Circuit No.:	CN103
Model:	RDAD-15SE-LNA, female
Parts No.:	367862
Mating Type:	D Sub 15P Male Connector



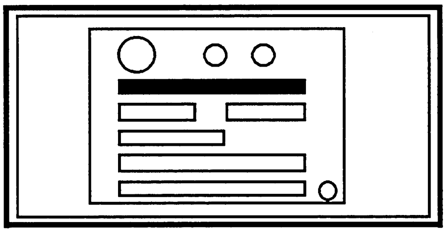
R	1	9	XC.SYNC
RGND	2	10	MIX SND
G	3	11	
GGND	4	12	E SND
B	5	13	HC
BGND	6	14	XHSYNC (25kHz)
	7	15	XVSYNC
GND	8		

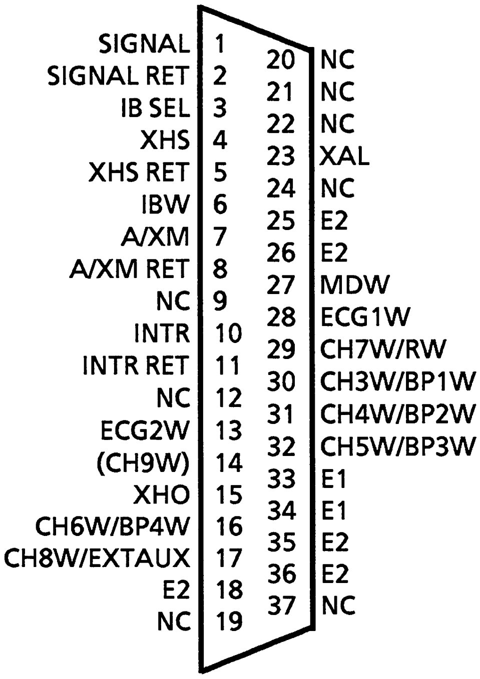
Construction of D Sub 25P Male Connector			Model	Part No.
Connector	Caulked Type	Housing	CDA-15P	080333
		Contact Pin	CD-PC-121	080431
	Souldered Type		HDAB-15P	080699
Case			HDA-CTH1	080564

6) CNS Connector

Circuit No.: CN105
Model: RDCD-37SE-LNA, Female
Part No.: 081092
Mating Type: D Sub 37P Male Connector

Mating Connector : BSM-JJConnector Cable, YS-006P2



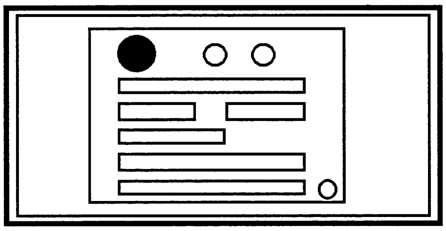

SIGNAL 1
SIGNAL RET 2
IB SEL 3
XHS 4
XHS RET 5
IBW 6
A/XM 7
A/XM RET 8
NC 9
INTR 10
INTR RET 11
NC 12
ECG2W 13
(CH9W) 14
XHO 15
CH6W/BP4W 16
CH8W/EXTAUX 17
E2 18
NC 19
20 NC
21 NC
22 NC
23 XAL
24 NC
25 E2
26 E2
27 MDW
28 ECG1W
29 CH7W/RW
30 CH3W/BP1W
31 CH4W/BP2W
32 CH5W/BP3W
33 E1
34 E1
35 E2
36 E2
37 NC

7) AUX IN Connector

Circuit No.:	CN104
Model:	RM12BRD-6S
Part No:	079772

(See Section 1-10, RELATED INSTRUMENTS CONNECTION for more information.)

Mating Connector :	RM12BPG-6P
Part No.:	078541



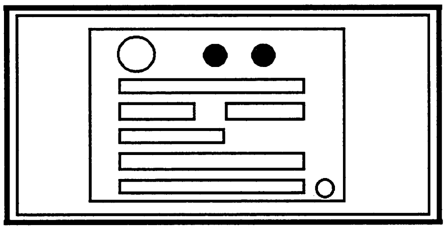
The table below lists the type of connectable auxiliary units and the signal name of each pin in this AUX IN connector.

Pin No..	Signal Name	Auxiliary Instrument For			
		CO_2	SpO_2	$tcPO_2/tcPCO_2$	Auxiliary Waveform Input
1	AUX1IN (±8 V)	$ETCO_2$ (20 mmHg/V)	SpO_2 (100%/V)	$tcPCO_2$ (200 mmHg/V*)	Not used
2	AUX2IN (±8 V)	CO_2W (20 mmHg/V)	Not used	$tcPO_2$ (200 mmHg/V*)	Auxiliary Waveform
3	AGND	Ground for Analog signal	Ground for Analog signal	Ground for Analog signal	Ground for Analog signal
4	AUX1C (Open collector type)	$ETCO_2$ alarm	SpO_2 alarm	$tcPCO_2$ alarm	Not used
5	AUX2C (Open collector type)	CO_2 measure	SpO_2 measure	$tcPO_2$ alarm	Not used
6	DGND	Ground for Digital signal	Ground for Digital signal	Ground for Digital signal	Not used

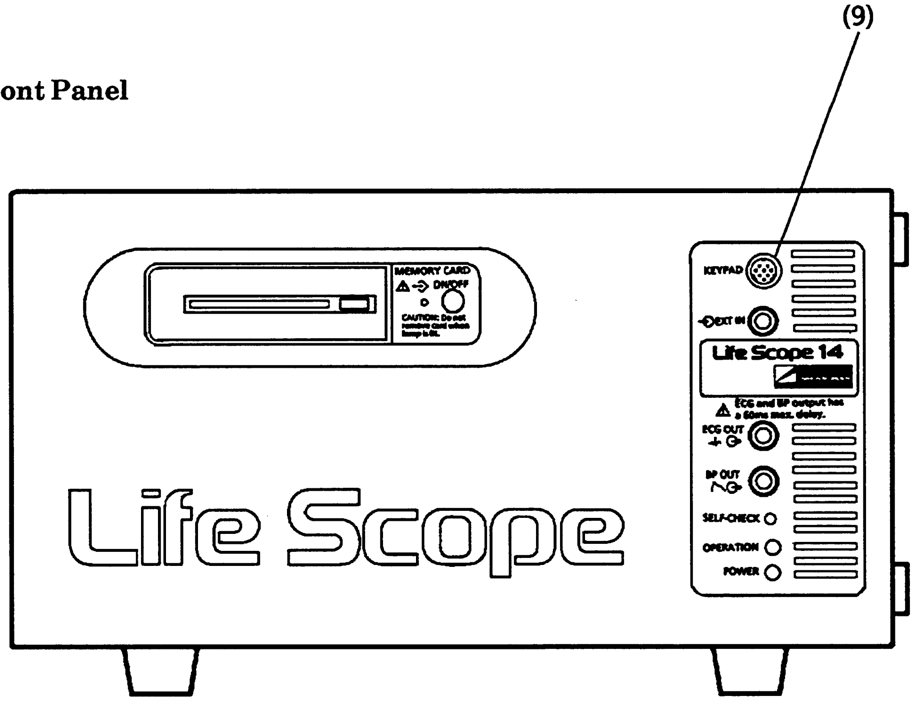
* To increase the gain to 1000 mmHg/V, cut the jumpers, J101 and J102 of the I/O board, UP-0797 (refer to 7-1-4).

8) ANT1, ANT2 Connector

BNC Connector



Front Panel


(9)
MEMORY CARD
ON/OFF
CAUTION: Do not remove card when lamp is lit.
Life Scope
KEYPAD
EXT IN
Life Scope 14
ECG and BP output has a 60ms max. delay.
ECG OUT
BP OUT
SELF-CHECK
OPERATION
POWER

9) Keypad Connector

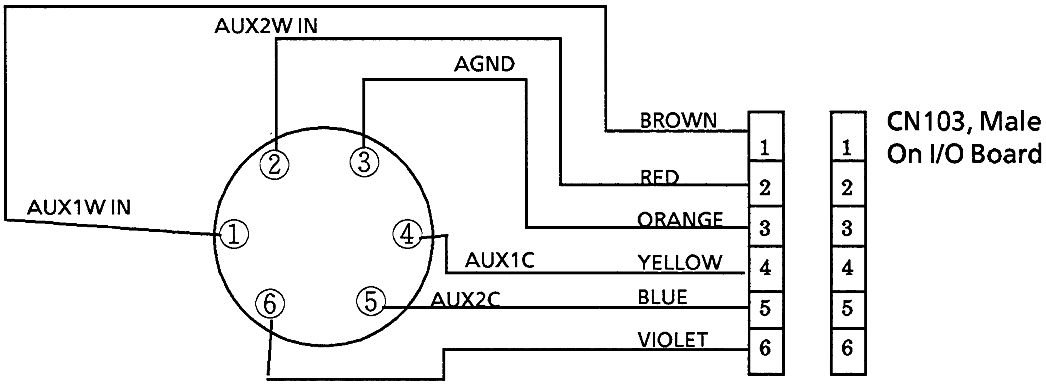
Circuit No.:	CN104 in the FRONT CONNECTOR board or CN108 in the OPERATION CONTROL board (Display Unit)
Model:	HR212-10R-8SDL
Parts No.:	356802
Mating Connector :	Keypad Connector Cord
Part No.:	359996

+ 5V	1	5	XKREADY
KREADY	2	6	E2
TxD2	3	7	E2
RxD2	4	8	XP.SCTL2

8-1-2 Internal Connectors and Wires in Main Unit

1) I/O Board Connector

Circuit No.:	CN103
Model:	M60-06-30-134P (to AUX Input)
Part No.:	089725
Connecting cable:	CN-ASSY M62-06-0004SA L=300
Part No.:	089645


AUX2W IN
AGND
AUX1W IN
AUX1C
AUX2C
①
②
③
④
⑤
⑥
BROWN
RED
ORANGE
YELLOW
BLUE
VIOLET
1
2
3
4
5
6
CN103, Male
On I/O Board

2) DPU Board Connector

Circuit No.:	CN104 (to J3 on ZR-800P/PA)
Model:	DF11-16DP-2DS
Part No.:	084356
Connecting Cable:	DF11-16DS-2C(20)
Part No.:	319282

DATA	1	9	NC
CLK	2	10	RT
LE	3	11	RD
NC	4	12	NC
+8V	5	13	NC
NC	6	14	NC
E1	7	15	NC
E1	8	16	E1

3) COM 3 Board Connector

Circuit No.:	CN104 (to I/O Board)
Model:	HIF3BA-40PA-2.54DS
Part No.:	085934
Connecting cable:	HIF3BA-40D-AC-10
Part No.:	319157

SIGNAL	1	2	NC
SIGNAL RET	3	4	NC
IB SEL	5	6	NC
XHS	7	8	XAL
XHS RET	9	10	NC
IBW	11	12	E2
A/XM	13	14	E2
A/XM RET	15	16	MDW
NC	17	18	ECG1W
INTR	19	20	CH7W/RW
INTR RET	21	22	CH3W/P1W
NC	23	24	CH4W/P2W
ECG2W	25	26	CH5W/P3W
(CH9W)	27	28	E1
XHO	29	30	E1
CH6W/P4W	31	32	E2
CH8W/EXTAUX	33	34	E2
E2	35	36	E2
E2	37	38	E2
E2	39	40	E2

4) MOTHER Board Connectors

- **To Fan Motor**

Circuit No.:	CN112 (to fan's motor)
Model:	M60-02-30-114P
Part No.:	090206
Socket Contact:	M62C84-4
Part No.:	090233
Socket Mould:	M62M84-02
Part No.:	090224

E5	1
+ 12V	2

- **To FRONT CONNECTOR Board**

Circuit No.:	CN113 (to CN101 of FRONT CONNECTOR Board)
Model:	FFC-20BSM1#02
Part No.:	091232A

Connecting Cable:	HKP-20FS02-10BT(30)
Part No.:	088904

+5VL	1	11	+5VB
+5VBL	2	12	EXTRDY
E2	3	13	IOTXD3
E2	4	14	IORXD3
P1W	5	15	XKEYRST2
ECG1W	6	16	STNBY
E1	7	17	E2
E1	8	18	E2
EXTIN	9	19	XEXTRST
AUX2IN	10	20	NC

5) REGULATOR Board Connector

- **To MOTHER Board**

Circuit No.:	CN105 (to CN111 on MOTHER board)
Model:	171457-1
Part No.:	268069

Connecting Cable:	SC-018R Connecor Cord
Part No.:	372437

+5.1V (8.7A)	1	12	+5.1V (8.7A)
+5VS	2	13	ER2
E2	3	14	E2
+5VB	4	15	E2
PWRCTL	5	16	NC
	6	17	E4
+21V (1.3A)	7	18	E4
–21V (0.15A)	8	19	E1
+8V (0.75A)	9	20	ER1
–8V (0.7A)	10	21	E5
+12V (0.15A)	11		

- **To TRANSFORMER UNIT Board**

Circuit No.:	CN102 (to CN101 on TRANSFORMER UNIT board)
Model:	172034-1
Part No.:	83407

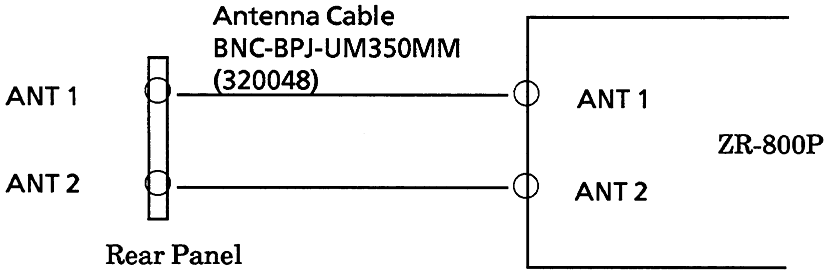
0	7	1	12V (0.9A)
NC	8	2	12V (0.7A)
NC	9	3	21V (3.3A)
		4	21V (0.15A)
0	10	5	0
7.5V (1A)	11	6	7.5V (1A)

6) MEMORY CARD Board Connector

Circuit No.:	CN101 (to CN201 on I/O Board)
Model:	HIF-6-68PA-1.27DS
Part No.:	356767
Connecting cable:	HIF6-68D-1.27R-AA(30)
Part No.:	369147

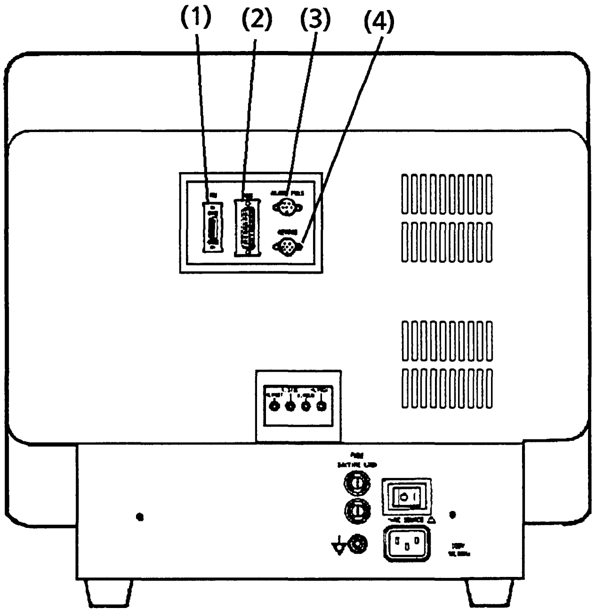
MD3	1A	1B	MCSW
MD5	2A	2B	MD4
MD7	3A	3B	NC
MA10	4A	4B	XCE1
MA11	5A	5B	XOE
MA8	6A	6B	MA9
MA14	7A	7B	MA13
RDY/XBSY	8A	8B	XWE
MCLED	9A	9B	+5V
MA15	10A	10B	MA16
MA7	11A	11B	MA12
MA5	12A	12B	MA6
MA3	13A	13B	MA4
MA1	14A	14B	MA2
MD0	15A	15B	MA0
MD2	16A	16B	MD1
E2	17A	17B	WP
XCD1	18A	18B	E2
MD12	19A	19B	MD11
MD14	20A	20B	MD13
XCE2	21A	21B	MD15
RFU1	22A	22B	XRFSH
MA17	23A	23B	RFU2
MA19	24A	24B	MA18
MA21	25A	25B	MA20
VPP	26A	26B	+5V
MA23	27A	27B	MA22
MA25	28A	28B	MA24
RFU4	29A	29B	RFU3
RFU6	30A	30B	RFU5
BVD2	31A	31B	XREG
MD8	32A	32B	BVD1
MD10	33A	33B	MD9
E2	34A	34B	XCD2

8-1-3 Wiring


Antenna Cable
BNC-BPJ-UM350MM
(320048)
ANT 1
ANT 2
Rear Panel
ANT 1
ANT 2
ZR-800P

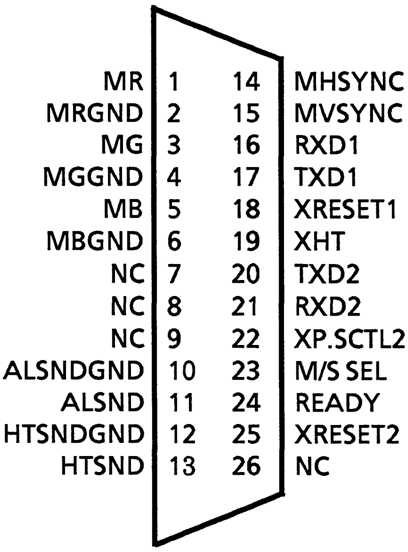
8-2 Display Unit, VD-881R

8-2-1 External Connectors on the Display Unit



1) MU Connector

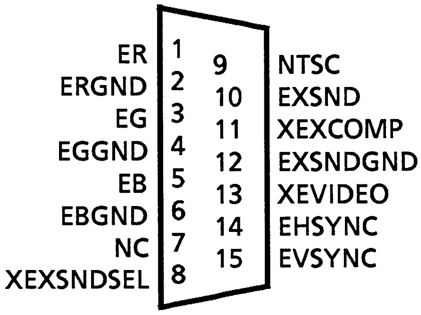
Circuit No. :	CN101
Model :	DX20M-26S
Part No. :	356829
Mating Connector:	VD Connector Cord
Part No.:	YS-0238



MR	1	14	MHSYNC
MRGND	2	15	MVSYNC
MG	3	16	RXD1
MGGND	4	17	TXD1
MB	5	18	XRESET1
MBGND	6	19	XHT
NC	7	20	TXD2
NC	8	21	RXD2
NC	9	22	XP.SCTL2
ALSNDGND	10	23	M/S SEL
ALSND	11	24	READY
HTSNDGND	12	25	XRESET2
HTSND	13	26	NC

2) MU Auxiliary Unit Connector

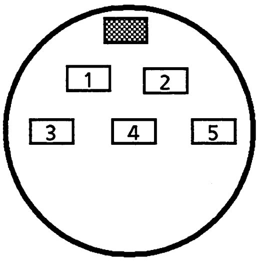
Circuit No.: CN102
Model: SDAB-15SSL-LNK
Part No.: 362724
Mating Type: D Sub 15P Male Connector


ER 1
ERGND 2
EG 3
EGGND 4
EB 5
EBGND 6
NC 7
XEXSNDSEL 8
9 NTSC
10 EXSND
11 XEXCOMP
12 EXSNDGND
13 XEVIDEO
14 EHSYNC
15 EVSYNC

3) Alarm Pole Connector

Circuit No.: CN108
Model: HR212-10R-5SD
Part No.: 356785

XALPLR	1	4	+ 12VA
XALPLY	2	5	+ 12VA
XALPLG	3	S	E2

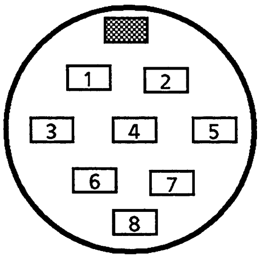


4) Keypad Connector

Circuit No.: CN106
Model: HR212-10RB-8SD
Part No.: 369441

Mating Connector: Keypad Connector Cord
Part No.: 359996

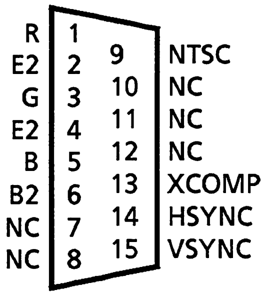
+ 5V	1	5	XRESET2
XREADY	2	6	E2
RXD2	3	7	E2
TXD2	4	8	XP.S CTL2



8-2-2 Internal Connectors in the Display Unit

1) CRT Unit Input Connector

Circuit No. :	CN103
Model :	RDAD-15SE-LNA
Part No. :	081118
Connecting Cable :	CDA-15PP-100
Part No. :	366007



R	1		
E2	2	9	NTSC
G	3	10	NC
E2	4	11	NC
B	5	12	NC
B2	6	13	XCOMP
NC	7	14	HSYNC
NC	8	15	VSYNC

2) OPERATION (VR) Board's CN101 Connector

Circuit No.:	CN104
Model :	HIF3BA-20PA-2.54DSA
Part No. :	085899
Connecting Cable :	HIF3BA-20D-AC-60
Part No. :	357828

SALSND15	1	11	+5V
E1	2	12	E2
HT/EXSND	3	13	+12V
E1	4	14	E1
VHT/EXSND	5	15	NC
E1	6	16	NC
VALSND	7	17	NC
E1	8	18	NC
WSLEEP	9	19	NC
REMOTE	10	20	NC

3) Speaker Connector

Circuit No. :	CN105
Model :	M60-03-30-114P
Part No. :	089663
Connecting Cable:	CN-ASSY M62-03-0018SA L=300
Part No.:	089654

SPKR-	1
SPKR +	2
NC	3

4) SC-019R Power Supply Unit's CN101 Connector

Circuit No. :	CN107
Model :	FFC-14BSM1#02ST
Part No. :	091205A
Connecting Cable :	HKP-14FS02-7BT
Part No. :	099233

+ 5V	1	8	E1
+ 5V	2	9	-12V
E2	3	10	-12V
E2	4	11	XP.SCTL1
+ 12V	5	12	NC
+ 12V	6	13	NC
E1	7	14	NC

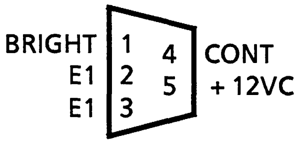
5) LED Board (UP-0806)'s CN101 Connector

Circuit No.:	CN103
Model :	HKP-6ML-3BT
Part No. :	085515
Connecting Cable :	HKP-6FS02-3BT(20)
Part No. :	089119

+ 5V	1	4	E1
E2	2	5	REMOTE
+ 12V	3	6	NC

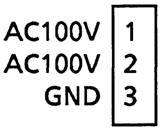
6) CRT Unit Connector

Circuit No.: CN102
Model : B5B-EH
Part No.: 313377


BRIGHT
E1
E1
1
2
3
4
5
CONT
+ 12VC

7) CRT Unit Power Supply Connector

Circuit No. : CN105
Model : 350429-1
Part No.: 083384
Connecting Cable: CRT Connecting Cable
Part No.: 371367


AC100V
AC100V
GND
1
2
3

8-3 Keypad, RY-881PA

8-3-1 External Connectors on the Keypad

1) Main Unit or Display Unit Connector

Circuit No.: CN101
Model: HR212-10RA-8SDL
Part No.: 356811

Mating Connector: Keypad Connector Cord
Part No.: 359996

+ 5V	1	5	XRESET2
XREADY	2	6	E2
RXD2	3	7	E2
TXD2	4	8	XP.S CTL2

Section 9 ELECTRICAL PARTS LIST

CD-130P CHASSIS 1 .... 9.1
CD-131P CHASSIS 1 .... 9.1
CD-137P CHASSIS 2 .... 9.1
CD-157P CHASSIS 2 .... 9.1
SC-018RA POWER TRANSFOMER UNIT 9.1
SC-018RJ POWER TRANSFOMER UNIT 9.1
SC-018RK POWER TRANSFOMER UNIT 9.1
SC-019RA POWER SUPPLY UNIT 9.2
SC-019RJ POWER SUPPLY UNIT 9.2
SC-019RK POWER SUPPLY UNIT 9.2
UP-0272 ECG HEAD AMP BOARD 9.3
UP-0318 CD HEAD AMP BOARD 9.3
UP-0319 TEMP HEAD AMP BOARD 9.4
UP-0369 PRESS HEAD AMP BOARD 9.4
UP-0420 ECG HEAD AMP BOARD 9.5
UP-0421 MAIN BOARD 9.5
UP-0422 SUB BOARD 9.5
UP-0548 TERMISTOR RESP HEAD AMP BOARD 9.5
UP-0563 COM3 BOARD 9.6
UP-0571 MOTOR BOARD 9.7
UP-0588 MAIN BOARD 9.7
UP-0589 SUB BOARD 9.8
UP-0592 O_2 HEAD AMP BOARD 9.8
UP-0629 MAIN BOARD 9.9
UP-0630 SUB BOARD 9.9
UP-0643 NIBP UNIT BOARD 9.9
UP-0670 DPU BOARD (without ROM) 9.10
UP-0795 CRTC (CRT CONTROL) BOARD 9.12
UP-0797 I / O BOARD 9.13
UP-0798 MOTHER BOARD 9.14
UP-0799 MEMORY CARD BOARD 9.14
UP-0801 OPERATION CONTROL BOARD 9.14
UP-0802 ORERATION (VR) BOARD 9.15
UP-0806 LED BOARD 9.15
UP-0807 CONNECTOR BOARD 9.15
UP-0813 REGULATOR BOARD 9.15

UR-3023 **CPU BOARD (with ROM)** **9.16**
UR-3025 **OPERATION RY BOARD** **9.17**
UR-3105 **SpO_2 HEAD AMP MAIN BOARD** **9.17**
UR-3106 **SpO_2 HEAD AMP SUB BOARD** **9.18**
UP-31551 **SpO_2 HEAD AMP BOARD** **9.19**

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION
UP-1234	IC101	146584	1	CMOS TC74HC74AP

- TC74HC74AP: Part name
- CMOS: Part abbreviation
- 1: Quantity used (0 is shown for compatible part)
- 146584: Nihon Kohden part number
- IC101: Circuit No. indicated on the circuit diagram and PCB (* means compatible part)
- UP-1234: Assembly name

ABBREVIATIONS

TRANSISTOR

TR	Transistors other than below
FET	FET
PTR	Phototransistor, photoreflector, and photocoupler

DIODE

D	Diodes other than below
LED	LED
ZD	Zener diode

IC

IC	ICs other than below
ADIC	A/D converter and D/A converter
CRTC	CRT controller
CMOS	CMOS
HIC	Hybrid
OPIC	Operational amplifier
REG	Regulator
RAM	RAM
TTL	TTL

SWITCH

SW	Switches other than below
ATT	Attenuator
RS	Rotary switch

CAPACITOR

C	Titanate, paper block, oil and mica
CEC	Ceramic
CM	Module
EC	Electrolyte
FLC	Film
TAC	Tantalum
VC	Variable capacitor

RESISTOR (Carbon and metal film type are omitted)

R	Mold, solid and cement
RM	Module
WR	Wirewound

VARIABLE RESISTOR

VR	Single rotation
POT	Multi rotation potentiometer
WVR	Wirewound

TRANSFORMER

TF	Transformers other than below
COIL	Choke, rotator, flyback and deflection yoke
PT	Power

CONNECTOR

CN	Connectors other than below
CNA	Harness cord
PCN	Mounted on PC board

MIISCELLANEOUS

ANT	Antenna
BATT	Battery
CLUT	Electromagnetic clutch
CORD	Cord
DISP	CRT, LCD, plasma display, and fluorescent screen
FAN	Fan
FUSE	Fuse, fuse holder and thermal fuse
GAGE	Gauge
HEAD	Thermal head and discharge head
LAMP	Bracket type lamp
MOTOR	Motor
PUMP	Pump
RY	Relay
SP	Speaker, headphone and buzzer
TUBE	Vacuum tube, discharge tube, neon tube and gas arrestor
UNIT	Assembled unit
VALV	Electromagnetic valve
XTAL	Crystal oscillator

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
CD-130P	**CHASSIS 1**				
CD-130P		079772	1	CN	RM12BRD-6S
CD-130P		090224	1	CN	socket M62 M83-02
CD-130P		090233	2	CN	socket contact M62C84-4
CD-130P		320048	2	CNA	antenna cord BNC-BPJ-UM 350MM
CD-130P		320271	2	CN	BNC-J cap
CD-130P		367737	1	FAN	fan motor ASF-84371 12V type
CD-130P		378556	1	CNA	M62-06-0004SA L = 30
CD-131P	**CHASSIS 1**				
CD-131P		089654	1	PCN	M62-03-0018SA (30)
CD-131P	SP001	073662	1	SP	EAS-65P34S 16OHM
CD-137P	**CHASSIS 2**				
CD-137P		088904A	1	PCN	HKP-20FS02-10BT(30) terminal
CD-137P		319157	1	PCN	HIF3BA-40D-AC-10
CD-137P		369147	1	CNA	HIF6-68D-1.27R-AA(30)
CD-157P	**CHASSIS 2**				
CD-157P		089119A	1	PCN	HKP-6FS02-3BT(20)
CD-157P		357828	1	CNA	HIF3BA-20D-AC-60
CD-157P		366007A	1	CNA	CDA-15PP-100A
CD-157P		410325B	1	DISP	QA1465A 14b inch color-CRT unit
SC-018RA	**POWER TRANSFOMER UNIT**				
SC-018RA	F101	103996	1	FUSE	SAU-3A (GDL-3)
SC-018RA	F101	104825	1	FUSE	fuse holder FEU031 1681
SC-018RA	F101	104834	1	FUSE	fuse cap FEK031.1661
SC-018RA	F102	103996	1	FUSE	SAU-3A (GDL-3)
SC-018RA	F102	104825	1	FUSE	fuse holder FEU031 1681
SC-018RA	F102	104834	1	FUSE	fuse cap FEK031.1661
SC-018RA	LF101	024252	1	NFLT	SUP-E3G-E-2 line filter
SC-018RA	SW101	370368	1	SW	JW-M22RKK
SC-018RJ	**POWER TRANSFOMER UNIT**				
SC-018RJ	F101	103996	1	FUSE	SAU-3A (GOL-3)
SC-018RJ	F101	104825	1	FUSE	fuse holder FEU031 1681
SC-018RJ	F101	104834	1	FUSE	fuse cap FEK031.1661
SC-018RJ	F102	103995	1	FUSE	SAU-3A (GDL-3)
SC-018RJ	F102	104825	1	FUSE	fuse holder FEU031.1681
SC-018RJ	F102	104834	1	FUSE	fuse cap FEK031.1661
SC-018RJ	LF101	024252	1	NFLT	SUP-E3G-E-2 line filter
SC-018RJ	SW101	370368	1	SW	JW-M22RkK
SC-018RJ	T101	365823	1	PT	power transformer for SC-018RJ
SC-018RJ	TB101	103131	1	TERM	ULC-505-3P-C
SC-018RK	**POWER TRANSFOMER UNIT**				
SC-018RK	F101	104576	1	FUSE	179 120-2A ELU
SC-018RK	F101	104825	1	FUSE	fuse holder FEU031 1681
SC-018RK	F101	104843	1	FUSE	fuse cap FEK031.1663
SC-018RK	F102	104576	1	FUSE	179 120-2A ELU
SC-018RK	F102	104825	1	FUSE	fuse holder FEU031 1681
SC-018RK	F102	104843	1	FUSE	fuse cap FEK031.1663
SC-018RK	LF101	024252	1	NFLT	SUP-E3G-E-2 line filter
SC-018RK	SW101	370368	1	SW	JW-M22RKK

9. ELECTRICAL PARTS LIST

SC-019RA POWER SUPPLY UNIT

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
SC-019RA		095095	2	CNA	V1.25-4 with cord (250) black
SC-019RA		098252	1	PCN	HKP-14FS02-7BT(40)
SC-019RA	CN102	156876	1	PCN	B3P-VH
SC-019RA	CN105	331981	1	PCN	350429-1 (3P)
SC-019RA	CN106	091205A	1	PCN	FFC-14BSM1#02ST
SC-019RA	C102	040172	1	EC	KME35VB1000 35/1000
SC-019RA	C103-C104	158214	2	EC	KME25VB-220 25V 220UF
SC-019RA	C106-C107	040332	2	EC	KME50VB 1 50V 1MF
SC-019RA	C109	040323	1	EC	KME35VB 220 35V220MF
SC-019RA	D101	004354	1	D	S5VB20
SC-019RA	D103-D104	003649	2	D	1SS81
SC-019RA	D105	004354	1	D	S5VB20
SC-019RA	D106	003943	1	D	V06C (1.1A200V)
SC-019RA	D107-D112	003649	6	D	1SS81
SC-019RA	D113	003943	1	D	V06C (1.1A200V)
SC-019RA	F101	104005	1	FUSE	SAU-4A
SC-019RA	F101	104825	1	FUSE	fuse holder FEU031 1681
SC-019RA	F101	104834	1	FUSE	fuse cap FEK031.1661
SC-019RA	F102	104005	1	FUSE	SAU-4A
SC-019RA	F102	104825	1	FUSE	fuse holder FEU031 1681
SC-019RA	F102	104834	1	FUSE	fuse cap FEK031.1661
SC-019RA	F105-F107	346207	3	FUSE	23902.5 LITTLE
SC-019RA	LF101	024252	1	NFLT	SUP-E3G-E-2 line filter
SC-019RA	Q101	002356	1	TR	2SD717-Y
SC-019RA	Q102	002026	1	TR	2SC2324K
SC-019RA	Q103	002855	1	FET	2SK30A GR
SC-019RA	SW101	370368	1	SW	JW-M22RKK
SC-019RA	VR101	062781	1	VR	GF06P 1 KOHM

SC-019RJ POWER SUPPLY UNIT

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
SC-019RJ		095095	2	CNA	V1.25-4 with cord (250) black
SC-019RJ		098252	1	PCN	HKP-14FS02-7BT(40)
SC-019RJ	CN102	156876	1	PCN	B3P-VH
SC-019RJ	CN105	331981	1	PCN	350429-1 (3P)
SC-019RJ	CN106	091205A	1	PCN	FFC-14BSM1#02ST
SC-019RJ	C102	040172	1	EC	KME35VB1000 35/1000
SC-019RJ	C103-C104	158214	2	EC	KME25VB-220 25V 220UF
SC-019RJ	C106-C107	040332	2	EC	KME50VB 1 50V 1MF
SC-019RJ	C109	040323	1	EC	KME35VB 220 35V220MF
SC-019RJ	D101	004354	1	D	S5VB20
SC-019RJ	D103-D104	003649	2	D	1SS81
SC-019RJ	D105	004354	1	D	S5VB20
SC-019RJ	D106	003943	1	D	V06C (1.1A200V)
SC-019RJ	D107-D112	003649	6	D	1SS81
SC-019RJ	D113	003943	1	D	V06C (1.1A200V)
SC-019RJ	F101	104005	1	FUSE	SAU-4A
SC-019RJ	F101	104825	1	FUSE	fuse holder FEU031 1681
SC-019RJ	F101	104834	1	FUSE	fuse cap FEK031.1661
SC-019RJ	F102	104005	1	FUSE	SAU-4A
SC-019RJ	F102	104825	1	FUSE	fuse holder FEU031 1681
SC-019RJ	F102	104834	1	FUSE	fuse cap FEK031.1661
SC-019RJ	F105-F107	346207	3	FUSE	23902.5 LITTLE
SC-019RJ	LF101	024252	1	NFLT	SUP-E3G-E-2 line filter
SC-019RJ	Q101	002356	1	TR	2SD717-Y
SC-019RJ	Q102	002026	1	TR	2SC2324K
SC-019RJ	Q103	002855	1	FET	2SK30A GR
SC-019RJ	SW101	370368	1	SW	JW-M22RKK
SC-019RJ	VR101	062781	1	VR	GF06P 1 KOHM

SC-019RK POWER SUPPLY UNIT

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
SC-019RK		095095	2	CNA	V1.25-4 with cord (250) black
SC-019RK		098252	1	PCN	HKP-14FS02-7BT(40)
SC-019RK	CN102	156876	1	PCN	B3P-VH
SC-019RK	CN105	331981	1	PCN	350429-1 (3P)
SC-019RK	CN106	091205A	1	PCN	FFC-14BSM1#02ST
SC-019RK	C102	040172	1	EC	KME35VB1000 35/1000
SC-019RK	C103-C104	158214	2	EC	KME25VB-220 25V 220UF
SC-019RK	C106-C107	040332	2	EC	KME50VB 1 50V 1MF
SC-019RK	C109	040323	1	EC	KME35VB 220 35V220MF
SC-019RK	D101	004354	1	D	S5VB20
SC-019RK	D103-D104	003649	2	D	1SS81
SC-019RK	D105	004354	1	D	S5VB20

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
SC-019RK	D106	003943	1	D	V06C (1.1A200V)
SC-019RK	D107-D112	003649	6	D	1SS81
SC-019RK	D113	003943	1	D	V06C (1.1A200V)
SC-019RK	F101	104576	1	FUSE	179 120-2A ELU
SC-019RK	F101	104825	1	FUSE	fuse holder FEU031 1681
SC-019RK	F101	104843	1	FUSE	fuse cap FEK031.1663
SC-019RK	F102	104576	1	FUSE	179 120-2A ELU
SC-019RK	F102	104825	1	FUSE	fuse holder FEU031 1681
SC-019RK	F102	104843	1	FUSE	fuse cap FEK031.1663
SC-019RK	F105-F107	346207	3	FUSE	23902.5 LITTLE
SC-019RK	LF101	024252	1	NFLT	SUP-E3G-E-2 line filter
SC-019RK	Q101	002356	1	TR	2SD717-Y
SC-019RK	Q102	002026	1	TR	2SC2324K
SC-019RK	Q103	002855	1	FET	2SK30A GR
SC-019RK	SW101	370368	1	SW	JW-M22RKK
SC-019RK	VR101	062781	1	VR	GF06P 1 KOHM

UP-0272 ECG HEAD AMP BOARD

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0272	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0272	C001-C002	042357	2	TAC	204M1602 106M4 (10MF/16V)
UP-0272	C003	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0272	C004	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0272	C005	071468	1	CEC	ECB T1H 470J5
UP-0272	C006	071307	1	CEC	DD05-989B101K500 500V 100PF
UP-0272	C007	071138	1	FLC	ECQ-V 1H 224JZ3 (0.22MF)
UP-0272	C008-C013	070834	6	FLC	ECQ-B 1H 102JZ3 0.001MF
UP-0272	C014-C015	046879	2	CEC	DE7090B 102K VA1-KC
UP-0272	D001-D004	071548	4	D	1S2076A RE
UP-0272	D005-D006	071539	2	D	1SS104,TPB2
UP-0272	D007-D008	071548	2	D	1S2076A RE
UP-0272	D011-D012	071539	2	D	1SS104,TPB2
UP-0272	D013-D014	071548	2	D	1S2076A RE
UP-0272	GA001	026811	1	TUBE	Y08-2100B
UP-0272	GA002-GA006	404475	5	TUBE	ceramic arrestor Y06S-100B
UP-0272	IC001	072975	1	REG	u PC78L05J-T
UP-0272	IC002	072984	1	REG	u PC79L05J-T
UP-0272	IC003	016181	1	OPIC	UPC812C
UP-0272	IC004	163262	1	CMOS	MC14051BCP
UP-0272	IC005	163128	1	ADIC	MC14094BCP
UP-0272	IC006	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0272	IC007	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0272	IC008	021736	1	HIC	EHD-HA1272 ECGSEL
UP-0272	IC009-IC012	021727	4	HIC	EHD-HA1271 ECGBUF
UP-0272	PC001-PC003	002739	3	PTR	PC810A
UP-0272	Q001	071904	1	TR	2SA836 CeaD TZ
UP-0272	Q002	072093	1	FET	2SK163 L1eaL2-T
UP-0272	Q003-Q004	072066	2	TR	2SC1213AKDTZ
UP-0272	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0272	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0272	T003	036943A	1	TF	T3772383 EP10IS(red) transformer
UP-0272	VR001	062799	1	VR	GF06P 5 KOHM

UP-0318 CD HEAD AMP BOARD

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0318	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0318	CN002	079558A	1	CN	HR16-18R-10S(01) red
UP-0318	CN003	090215	1	PCN	M60-04-30-114P (4P)
UP-0318	C001-C002	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0318	C003	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0318	C004	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0318	C006	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0318	C007	042357	1	TAC	204M1602 106M4 (10MF/16V)
UP-0318	C008	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0318	C009-C010	071094	2	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0318	C011	071174	1	FLC	ECQ-V 1H 474JZ3 (0.47MF)
UP-0318	C012	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0318	C013-C014	070959	2	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0318	D001-D007	071548	7	D	1S2076A RE
UP-0318	GA001	026811	1	TUBE	Y08-2100B
UP-0318	IC001	072975	1	REG	u PC78L05J-T
UP-0318	IC002	072984	1	REG	u PC79L05J-T
UP-0318	IC003	163289	1	CMOS	MC14053BCP
UP-0318	IC004	015993	1	REG	LT1009CZ 2.5VREF
UP-0318	IC005	016083	1	OPIC	UPC4062C
UP-0318	IC006	016181	1	OPIC	UPC812C
UP-0318	IC007	015779	1	OPIC	LT1001CN8 LOW DRIFT
UP-0318	IC008	010739	1	OPIC	HA17903PS

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0318	IC009	163262	1	CMOS	MC14051BCP
UP-0318	IC010	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0318	IC011	163128	1	ADIC	MC14094BCP
UP-0318	IC012	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0318	IC013	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0318	PC001-PC002	002739	2	PTR	PC810A
UP-0318	Q001-Q003	072066	3	TR	2SC1213AKDTZ
UP-0318	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0318	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0318	VR001	062932	1	VR	GF06P 2 KOHM
UP-0318	VR002-VR003	062781	2	VR	GF06P 1 KOHM
UP-0318	VR004	062807	1	VR	GF06P 10 KOHM
UP-0318	VR005	062781	1	VR	GF06P 1 KOHM

UP-0319 TEMP HEAD AMP BOARD

UP-0319	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0319	CN002	092775	1	CN	jack HLJ0527-01-030 with nut
UP-0319	CN003	090215	1	PCN	M60-04-30-114P (4P)
UP-0319	C001-C002	042357	2	TAC	204M1602 106M4 (10MF/16V)
UP-0319	C003	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0319	C004	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0319	C006	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0319	C007-C008	071094	2	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0319	C009	071343	1	CEC	DD05-989B471K500 500V 470PF
UP-0319	C010	070834	1	FLC	ECQ-B 1H 102JZ3 0.001MF
UP-0319	C011	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0319	C014	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0319	D001-D006	071548	6	D	1S2076A RE
UP-0319	GA001	026811	1	TUBE	Y08-2100B
UP-0319	IC001	072975	1	REG	u PC78L05J-T
UP-0319	IC002	072984	1	REG	u PC79L05J-T
UP-0319	IC003	163289	1	CMOS	MC14053BCP
UP-0319	IC004	015993	1	REG	LT1009CZ 2.5VREF
UP-0319	IC005	016083	1	OPIC	UPC4062C
UP-0319	IC006	015779	1	OPIC	LT1001CN8 LOW DRIFT
UP-0319	IC007	163262	1	CMOS	MC14051BCP
UP-0319	IC008	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0319	IC009	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0319	PC001	002739	1	PTR	PC810A
UP-0319	Q001-Q002	072066	2	TR	2SC1213AKDTZ
UP-0319	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0319	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0319	VR001	062932	1	VR	GF06P 2 KOHM
UP-0319	VR002	062781	1	VR	GF06P 1 KOHM

UP-0369 PRESS HEAD AMP BOARD

UP-0369	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0369	CN002-CN003	079487	2	CN	HR16-13R-5S(02) orange
UP-0369	CN004	089672	1	PCN	M60-06-30-114P (6P)
UP-0369	C001-C002	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0369	C003	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0369	C004	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0369	C006	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0369	C007	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0369	C008-C009	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0369	C010	071058	1	FLC	ECQ-V 1H 473JZ3 (0.047MF)
UP-0369	C011	071031	1	FLC	ECQ-V 1H 333JZ3 (0.033MF)
UP-0369	C012	071058	1	FLC	ECQ-V 1H 473JZ3 (0.047MF)
UP-0369	C013	071031	1	FLC	ECQ-V 1H 333JZ3 (0.033MF)
UP-0369	C016	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0369	C017-C021	071094	5	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0369	D001-D004	071548	4	D	1S2076A RE
UP-0369	D006-D013	071539	8	D	1SS104,TPB2
UP-0369	D014-D015	071548	2	D	1S2076A RE
UP-0369	GA001	026811	1	TUBE	Y08-2100B
UP-0369	IC001	072975	1	REG	u PC78L05J-T
UP-0369	IC002	072984	1	REG	u PC79L05J-T
UP-0369	IC003	163289	1	CMOS	MC14053BCP
UP-0369	IC004	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0369	IC005	015993	1	REG	LT1009CZ 2.5VREF
UP-0369	IC006	016083	1	OPIC	UPC4062C
UP-0369	IC007-IC010	015779	4	OPIC	LT1001CN8 LOW DRIFT
UP-0369	IC011-IC013	016083	3	OPIC	UPC4062C
UP-0369	IC014	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0369	PC001	002739	1	PTR	PC810A
UP-0369	PC002	002695	1	PTR	PC-827

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0369	Q001-Q003	072066	3	TR	2SC1213AKDTZ
UP-0369	Q004	071931	1	TR	2SA673AKCTZ
UP-0369	Q005	072066	1	TR	2SC1213AKDTZ
UP-0369	RA001	072636	1	RM	EXB-F8 V 103JYV
UP-0369	RA002	060916	1	RM	EXB-F5E-105J
UP-0369	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0369	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0369	VR001-VR002	062923	2	VR	GF06P 200 OHM

UP-0420 ECG HEAD AMP BOARD

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0420	CN003	079585A	1	CN	HR16-18R-10S(04) green

UP-0421 MAIN BOARD

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0421	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0421	CN002	089342	1	PCN	HKP-14FDS2-7,8,9T
UP-0421	C001-C002	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0421	C003	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0421	C004	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0421	C005-C006	070959	2	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0421	C007	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0421	C008-C016	070834	9	FLC	ECQ-B 1H 102JZ3 0.001MF
UP-0421	C017	070995	1	FLC	ECQ-B 1H 223JZ3 0.022MF
UP-0421	C018-C019	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0421	D001-D010	071548	10	D	1S2076A RE
UP-0421	D030-D039	071486	10	D	1SS104,TP3
UP-0421	GA001	026811	1	TUBE	Y08-2100B
UP-0421	IC001	072975	1	REG	u PC78L05J-T
UP-0421	IC002	072984	1	REG	u F286F286 PC79L05J-T
UP-0421	IC003	163289	1	CMOS	MC14053BCP
UP-0421	IC004	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0421	IC005	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0421	IC006	016083	1	OPIC	UPC4062C
UP-0421	IC007-IC008	020523	2	OPIC	u PC812C yellow low noise
UP-0421	PC001-PC002	002739	2	PTR	PC810A
UP-0421	Q001-Q003	072066	3	TR	2SC1213AKDTZ
UP-0421	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0421	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0421	VR001	062799	1	VR	GF06P 5 KOHM

UP-0422 SUB BOARD

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0422	CN050	089235	1	PCN	HKP-14M5S-7,8,9T receptacle male
UP-0422	C050-C057	070531	8	TAC	204M2002 106MB(10MF/20V)
UP-0422	C058-C059	070932	2	FLC	ECQ-B 1H 682JZ3 0.0068MF
UP-0422	C060-C061	070914	2	FLC	ECQ-B1H472JZ3 50V 0.0047UF
UP-0422	C062-C063	070995	2	FLC	ECQ-B 1H 223JZ3 0.022MF
UP-0422	C064-C065	070923	2	FLC	ECQ-B 1H 562JZ3 0.0056MF
UP-0422	C066-C071	071058	6	FLC	ECQ-V 1H 473JZ3 (0.047MF)
UP-0422	C072-C073	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0422	C074-C075	071236	2	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0422	D050-D053	071548	4	D	1S2076A RE
UP-0422	IC050	020523	1	OPIC	u PC812C yellow low noise
UP-0422	IC051-IC054	015779	4	OPIC	LT1001CN8 LOW DRIFT
UP-0422	IC055-IC056	016083	2	OPIC	UPC4062C
UP-0422	VR050-VR051	164386	2	POT	ET-6S 20KOHM
UP-0422	VR054-VR055	063031	2	VR	GF06S 500OHM
UP-0548	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)

UP-0548 TERMISTOR RESP HEAD AMP BOARD

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0548	CN002	092035	1	CN	LGY 6501-0101 SMK
UP-0548	CN003	090215	1	PCN	M60-04-30-114P (4P)
UP-0548	C001-C002	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0548	C003-C004	070718	2	TAC	204M3502 105MB (1MF/35V)
UP-0548	C005	070531	1	TAC	204M2002 106MB(10MF/20V)
UP-0548	C006	071174	1	FLC	ECQ-V 1H 474JZ3 (0.47MF)
UP-0548	C007	071031	1	FLC	ECQ-V 1H 333JZ3 (0.033MF)
UP-0548	C008	043873	1	FLC	DH4M2A-105K 100V 1UF
UP-0548	C009	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0548	C010	071031	1	FLC	ECQ-V 1H 333JZ3 (0.033MF)
UP-0548	C011-C012	070959	2	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0548	D001-D006	071548	6	D	1S2076A RE

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0548	D007-D008	071539	2	D	1SS104,TPB2
UP-0548	GA001	026811	1	TUBE	Y08-2100B
UP-0548	IC001	072975	1	REG	u PC78L05J-T
UP-0548	IC002	072984	1	REG	u PC79L05J-T
UP-0548	IC003	015993	1	REG	LT1009CZ 2.5VREF
UP-0548	IC004	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0548	IC005	016163	1	OPIC	UPC811C
UP-0548	IC006	016181	1	OPIC	UPC812C
UP-0548	IC007	016083	1	OPIC	UPC4062C
UP-0548	IC008	163289	1	CMOS	MC14053BCP
UP-0548	PC001	002739	1	PTR	PC810A
UP-0548	Q001-Q002	072066	2	TR	2SC1213AKDTZ
UP-0548	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0548	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0548	VR001	062807	1	VR	GF06P 10 KOHM

UP-0563 COM3 BOARD

UP-0563	CN101	089957	1	PCN	PCN10EA-90P-2.54DS(05)
UP-0563	CN102	089912	1	PCN	PCN10EA-32P-2.54DS(05)
UP-0563	CN103	081092	1	CN	RDCD-37SE-LNA F343
UP-0563	CN104	085934	1	PCN	HIF3BA-40PA-2.54DS
UP-0563	C001-C004	071236	4	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C005-C010	070487	6	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C020-C021	070487	2	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C022	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C023-C024	070487	2	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C025-C047	071236	23	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C048	070487	1	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C048-C051	071236	4	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C052	070487	1	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C053-C066	071236	14	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C067-C068	070487	2	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C101-C102	071245	2	CEC	DD05-989SL100D500 500V 10PF
UP-0563	C103	071343	1	CEC	DD05-989B471K500 500V 470PF
UP-0563	C104-C105	071236	2	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C106	071076	1	FLC	ECQ-V 1H 683JZ3 (0.068MF)
UP-0563	C107	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0563	C108-C111	071236	4	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C112	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0563	C113	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C115	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C116-C117	070487	2	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C118	070879	1	FLC	ECQ-B1H222JZ3 50V 0.0022UF
UP-0563	C119	070487	1	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C120	070834	1	FLC	ECQ-B 1H 102JZ3 0.001MF
UP-0563	C121	070487	1	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	D001-D002	071503	2	D	1S2076ATE
UP-0563	D101	071503	1	D	1S2076ATE
UP-0563	D901-D925	071512	25	D	1SS237(1)-T1
UP-0563	IC101-IC103	019463	3	CMOS	UPD74HCT240C
UP-0563	IC104	019472	1	CMOS	UPD74HCT244C
UP-0563	IC105-IC106	019525	2	CMOS	UPD74HCT640C
UP-0563	IC107-IC111	162771	5	CMOS	HD74HC138P
UP-0563	IC112	163823	1	ADIC	u PD74HC32C
UP-0563	IC113	018758	1	CMOS	UPD74HC30C
UP-0563	IC114	010953	1	TTL	74F04PC
UP-0563	IC115	011881	1	TTL	74F20PC
UP-0563	IC116	011007	1	TTL	74F164PC
UP-0563	IC117	011881	1	TTL	74F20PC
UP-0563	IC118	011319	1	TTL	74F10PC
UP-0563	IC120	008992	1	TTL	SN74LS74AN
UP-0563	IC121	008608	1	TTL	SN74LS04N
UP-0563	IC122	008902	1	TTL	SN74LS38
UP-0563	IC124	008653	1	TTL	SN74LS27N
UP-0563	IC125	008769	1	TTL	SN74LS08N
UP-0563	IC126	367416	1	CPU	MS62256CLL-10PC
UP-0563	IC127-IC130	008698	4	TTL	SN74LS157N
UP-0563	IC131-IC132	010142	2	TTL	SN74LS245N
UP-0563	IC133	018464	1	CPU	u PD8085AHC(AC,AC-2)
UP-0563	IC134	009901	1	TTL	SN74LS373
UP-0563	IC135	009884	1	TTL	SN74LS367AN
UP-0563	IC136	008608	1	TTL	SN74LS04N
UP-0563	IC137	008876	1	TTL	SN74LS32N
UP-0563	IC138	009251	1	TTL	SN74LS139AN
UP-0563	IC139	008876	1	TTL	SN74LS32N
UP-0563	IC140	009251	1	TTL	SN74LS139AN
UP-0563	IC141	011195	1	CPU	HN27C256G20 uPD27C256AD20
UP-0563	IC142	367416	1	CPU	MS62256CLL-10PC
UP-0563	IC143	018615	1	CPU	u PD8251AFC-D USART
UP-0563	IC144	008992	1	TTL	SN74LS74AN

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0563	IC145	008698	1	TTL	SN74LS157N
UP-0563	IC146	009697	1	TTL	SN74LS273
UP-0563	IC147	008992	1	TTL	SN74LS74AN
UP-0563	IC148	008769	1	TTL	SN74LS08N
UP-0563	IC149-IC150	008876	2	TTL	SN74LS32N
UP-0563	IC151	008591	1	TTL	SN74LS02N
UP-0563	IC152	008813	1	TTL	SN74LS14N
UP-0563	IC153	015529	1	CMOS	AM26LS33PC QUAD L.REC.AMD
UP-0563	IC154	012461	1	TTL	SN75174N LINE DRIVER
UP-0563	IC155	007832	1	TTL	SN7406N
UP-0563	IC156	016092	1	ADIC	HA-17012PB 12BIT DA
UP-0563	IC157-IC158	009697	2	TTL	SN74LS273
UP-0563	IC160	009251	1	TTL	SN74LS139AN
UP-0563	IC161	015993	1	REG	LT1009CZ 2.5VREF F418
UP-0563	IC162-IC163	016163	2	OPIC	UPC811C
UP-0563	IC164	009697	1	TTL	SN74LS273
UP-0563	IC165	010062	1	TTL	SN74LS244N
UP-0563	IC166	009991	1	TTL	SN74LS390N
UP-0563	IC167	009376	1	TTL	SN74LS163
UP-0563	IC168	162887	1	CMOS	HD74HC4040P
UP-0563	IC169-IC170	009189	2	TTL	SN74LS123N
UP-0563	IC171	009224	1	TTL	SN74LS132
UP-0563	IC172	072948	1	REG	u PC79L15J-T
UP-0563	IC173	072957	1	REG	u PC78L15J-T
UP-0563	IC176-IC179	367416	4	CPU	MS62256CLL-10PC
UP-0563	IC180	012969	1	RAM	MB8421-12LP
UP-0563	IC181	009919	1	TTL	SN74LS374N
UP-0563	IC182-IC184	010062	3	TTL	SN74LS244N
UP-0563	IC185	010846	1	TTL	SN74LS641
UP-0563	IC186	008608	1	TTL	SN74LS04N
UP-0563	IC187	008902	1	TTL	SN74LS38
UP-0563	LED101-LED109	342497	9	LED	GL3AR8 red
UP-0563	Q101	072066	1	TR	2SC1213AKDTZ
UP-0563	RA101-RA105	072387	5	RM	EXB-F9 E 104JYV
UP-0563	RA106	072369	1	RM	EXB-F9 E 472JYV
UP-0563	RA107	072387	1	RM	EXB-F9 E 104JYV
UP-0563	RA108	072369	1	RM	EXB-F9 E 472JYV
UP-0563	RA109	072173	1	RM	EXB-F5 E 472JYV
UP-0563	RA110	072369	1	RM	EXB-F9 E 472JYV
UP-0563	RA111	072173	1	RM	EXB-F5 E 472JYV
UP-0563	RA112	072369	1	RM	EXB-F9 E 472JYV
UP-0563	RA113	072173	1	RM	EXB-F5 E 472JYV
UP-0563	RA114	072324	1	RM	EXB-F9 E 102JYV
UP-0563	RA901-RA906	072592	6	RM	EXB-F8 V 471JYV
UP-0563	RA907-RA909	072333	3	RM	EXB-F9 E 152JYV
UP-0563	SK133	356606	1	CN	AXS204011(u -IC socket 40pin)
UP-0563	SK141	356598	1	CN	AXS202811(u -IC socket 28pin)
UP-0563	SK174-SK175	356598	2	CN	AXS202811(u -IC socket 28pin)
UP-0563	SW101	030673	1	DSW	B-8A-T
UP-0563	SW102	031039	1	DSW	B-4A-T
UP-0563	SW103	032484	1	SW	SKHCAD (KHC-10904)
UP-0563	VR102-VR103	072672	2	POT	GF06UT2 100 OHM
UP-0563	VR104	072734	1	POT	GF06UT2 10 KOHM
UP-0563	X101	023235	1	XTAL	NC-18C 6.144MHZ

UP-0571 MOTOR BOARD

UP-0571		140278	1	ETC	infrared filter 4.3u
UP-0571		140287	1	ETC	infrared filter 3.7u
UP-0571	C101	042624	1	TAC	ECSZ20MA4R7
UP-0571	C102-C103	047174	2	CEC	ECBA1E104ZF
UP-0571	C104	042633	1	TAC	ECSZ6MA10
UP-0571	C105	047183	1	CEC	ECBA1H221KB5
UP-0571	IC101	016644	1	OPIC	u PC822G2
UP-0571	M101	075366	1	MOTR	1616T012S-72 DC motor mini motor
UP-0571	P101	004675	1	D	PBSE P791-09
UP-0571	VR101	062469	1	POT	ST-4B 500KOHM

UP-0588 MAIN BOARD

UP-0588	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0588	CN002	089342	1	PCN	HKP-14FDS2-7,8,9T
UP-0588	C001-C002	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0588	C003-C007	071236	5	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0588	C008	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0588	C009	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0588	C010-C011	070959	2	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0588	C012	070834	1	FLC	ECQ-B 1H 102JZ3 0.001MF

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0588	C013	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0588	C014	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0588	D001-D004	071548	4	D	1S2076A RE
UP-0588	IC001	163128	1	ADIC	MC14094BCP
UP-0588	IC002	014495	1	ADIC	u F448PC624C
UP-0588	IC003	017973	1	CMOS	HD14538BP
UP-0588	IC004-IC005	017091	2	CMOS	HD14040BP (MC14040BCP)
UP-0588	IC006	015993	1	REG	LT1009CZ 2.5VREF
UP-0588	IC007	016181	1	OPIC	UPC812C
UP-0588	IC008-IC010	016083	3	OPIC	UPC4062C
UP-0588	PC001	002739	1	PTR	PC810A
UP-0588	Q001	071904	1	TR	2SA836 C or D TZ
UP-0588	T001	038068	1	TF	DC-DC converter DC-3826 transformer
UP-0588	VR001	164368	1	POT	ET-6S 5KOHM

UP-0589 SUB BOARD

UP-0589	CN050	089235	1	PCN	HKP-14M5S-7,8,9T
UP-0589	C050-C052	071236	3	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0589	C053	071174	1	FLC	ECQ-V 1H 474JZ3 (0.47MF)
UP-0589	C054	070834	1	FLC	ECQ-B 1H 102JZ3 0.001MF
UP-0589	C055-C056	071094	2	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0589	C057	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0589	C058	070914	1	FLC	ECQ-B1H472JZ3 50V 0.0047UF
UP-0589	C059-C063	071094	5	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0589	C064	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0589	C065	071343	1	CEC	DD05-989B471K500 500V 470PF
UP-0589	D050	071548	1	D	1S2076A RE
UP-0589	D051	071539	1	D	1SS104,TPB2
UP-0589	D052	071548	1	D	1S2076A RE
UP-0589	IC050-IC051	016083	2	OPIC	UPC4062C
UP-0589	IC052	017973	1	CMOS	HD14538BP
UP-0589	IC053	016822	1	CMOS	MC14013BCP
UP-0589	IC054	163066	1	CMOS	MC14001BCP
UP-0589	IC055	163289	1	CMOS	MC14053BCP
UP-0589	IC056	017322	1	CMOS	HD-14066BP
UP-0589	IC057	163262	1	CMOS	MC14051BCP
UP-0589	IC058-IC061	016181	4	OPIC	UPC812C
UP-0589	IC062	010739	1	OPIC	HA17903PS
UP-0589	IC063	016083	1	OPIC	UPC4062C

UP-0592 O_2 HEAD AMP BOARD

UP-0592	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0592	CN002	079504	1	CN	HR16-13R-5S(04) green
UP-0592	CN003	090215	1	PCN	M60-04-30-114P (4P)
UP-0592	C001-C002	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0592	C003	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0592	C004	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0592	C005	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0592	C006	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0592	C007	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0592	C008	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0592	C009	071343	1	CEC	DD05-989B471K500 500V 470PF
UP-0592	C010-C011	070959	2	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0592	D001-D006	071548	6	D	1S2076A RE
UP-0592	D007-D012	071539	6	D	1SS104,TPB2
UP-0592	GA001	026811	1	TUBE	Y08-2100B
UP-0592	IC001	072975	1	REG	u PC78L05J-T
UP-0592	IC002	072984	1	REG	u PC79L05J-T
UP-0592	IC003	163289	1	CMOS	MC14053BCP
UP-0592	IC004	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0592	IC005	015993	1	REG	LT1009CZ 2.5VREF
UP-0592	IC006	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0592	IC007	163262	1	CMOS	MC14051BCP
UP-0592	IC008	016181	1	OPIC	UPC812C
UP-0592	IC009-IC010	016698	2	OPIC	LT1012CN8
UP-0592	PC001-PC002	002739	2	PTR	PC810A
UP-0592	Q001-Q002	072066	2	TR	2SC1213AKDTZ
UP-0592	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0592	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0592	VR001-VR002	062799	2	VR	GF06P 5 KOHM

UP-0629 MAIN BOARD

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION
UP-0629	CNJ102	090215	1	PCN M60-04-30-114P (4P)
UP-0629	CNJ103	339884	1	PCN M60-09-30-114P
UP-0629	CN101	089895	1	PCN PCN10EA-20P-2.54DS(05)
UP-0629	CN104	092302	1	PCN FSN-21.5A-9 flexible jumper
UP-0629	C101	159695	1	TAC 267M3502 106MR720 10MF35V
UP-0629	C102	368905	1	CEC ECU V1H 104ZFX
UP-0629	C103	331107	1	FLC ECW-U1H223JA5 50V 0.022UF
UP-0629	C104	161513	1	CEC C4532X7R1H 334KT 0.33MF
UP-0629	C105	159695	1	TAC 267M3502 106MR720 10MF35V
UP-0629	C106	159775	1	CEC GRM39SL 221K50PT 220PF50V
UP-0629	C107-C108	161513	2	CEC C4532X7R1H 334KT 0.33MF
UP-0629	C109	331107	1	FLC ECW-U1H223JA5 50V 0.022UF
UP-0629	C110	159695	1	TAC 267M3502 106MR720 10MF35V
UP-0629	C111	040591	1	EC ECEAICGE471 470MF 16V
UP-0629	C112-C118	368905	7	CEC ECU V1H 104ZFX
UP-0629	C119	159775	1	CEC GRM39SL 221K50PT 220PF50V
UP-0629	C120	040591	1	EC ECEAICGE471 470MF 16V
UP-0629	D101-D109	160078	9	D HSK120TR
UP-0629	IC101-IC103	160309	3	ADIC HA17903FP
UP-0629	IC104	160523	1	CMOS MC14040BF
UP-0629	IC105	161558	1	CMOS MC14094BF
UP-0629	IC106	160595	1	CMOS MC14066BF
UP-0629	IC107	160817	1	CMOS MC14538BF
UP-0629	IC108	160595	1	CMOS MC14066BF
UP-0629	IC109	160523	1	CMOS MC14040BF
UP-0629	IC110	160505	1	CMOS MC14027BF
UP-0629	IC111-IC113	160452	3	CMOS MC14011BF
UP-0629	IC114	160844	1	CMOS MC14584BF
UP-0629	IC115	160603	1	CMOS MC14068BF
UP-0629	IC116	160817	1	CMOS MC14538BF
UP-0629	IC117	160497	1	CMOS MC14025BF
UP-0629	Q101	161487	1	TR 2SC4181-T2
UP-0629	Q102	160149	1	TR 2SC2618 D TR
UP-0629	Q103-Q107	161496	5	TR 2SD1950-T1
UP-0629	Q108	160149	1	TR 2SC2618 D TR
UP-0629	RY101	033073	1	RY G6A-274P 6V mini relay

UP-0630 SUB BOARD

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION
UP-0630	C201	368905	1	CEC ECU V1H 104ZFX
UP-0630	C202	159695	1	TAC 267M3502 106MR720 10MF35V
UP-0630	C203-C204	331134	2	FLC ECW-U1H103JA5 50V 0.01UF
UP-0630	C205	341471	1	FLC ECW-U1H473JA5 50V 0.047UF
UP-0630	C206	357801	1	FLC ECW-U1H104JB9 50V 0.1UF
UP-0630	C207	161513	1	CEC C4532X7R1H 334KT 0.33MF
UP-0630	C208	331134	1	FLC ECW-U1H103JA5 50V 0.01UF
UP-0630	C209	161513	1	CEC C4532X7R1H 334KT 0.33MF
UP-0630	C210	331134	1	FLC ECW-U1H103JA5 50V 0.01UF
UP-0630	C211-C212	368905	2	CEC ECU V1H 104ZFX
UP-0630	C213	159775	1	CEC GRM39SL 221K50PT 220PF50V
UP-0630	IC201	160407	1	REG LT1009S8
UP-0630	IC202-IC204	160202	3	OPIC LT1001CS8
UP-0630	IC205-IC206	160274A	2	OPIC u PC4062G2-E2
UP-0630	IC207	160595	1	CMOS MC14066BF
UP-0630	IC208	160568	1	CMOS MC14051BF
UP-0630	IC209	160256	1	OPIC u PC811G2
UP-0630	T201	366738	1	TD FPM-07PG-NK1(red)
UP-0630	VR201	159828	1	POT G4AT 200 OHM
UP-0630	VR202	161567	1	POT ST-5TP 1 KOHM

UP-0643 NIBP UNIT BOARD

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION
UP-0643	DCC501	038077	1	TF EX-7202B DC/DC converter

9. ELECTRICAL PARTS LIST

UP-0670 DPU BOARD (without ROM)

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0670		092614	2	CN	RDBD
UP-0670	CN101	089957	1	PCN	PCN10EA-90P-2.54DS(05)
UP-0670	CN102	089912	1	PCN	PCN10EA-32P-2.54DS(05)
UP-0670	CN103	081092	1	CN	RDCD-37SE-LNA
UP-0670	CN104	084356	1	PCN	DF11-16DP-2DS receptacle male
UP-0670	C001-C010	070487	10	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0670	C021-C022	070959	2	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0670	C031-C050	368905	20	CEC	ECU V1H 104ZFX
UP-0670	C052-C075	368905	24	CEC	ECU V1H 104ZFX
UP-0670	C201	159668	1	TAC	267M3502 225MR533 2.2MF35
UP-0670	C202	368905	1	CEC	ECU V1H 104ZFX
UP-0670	C701-C702	070834	2	FLC	ECQ-B 1H 102JZ3 0.001MF
UP-0670	C703	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0670	C704-C715	070959	12	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0670	C716-C719	368905	4	CEC	ECU V1H 104ZFX
UP-0670	C721-C724	070959	4	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0670	C731	159784	1	CEC	GRM39SL 331K50PT 330PF50V
UP-0670	C732	368905	1	CEC	ECU V1H 104ZFX
UP-0670	C733	043543	1	FLC	ECQP1H102JZ 1000PF
UP-0670	C734-C737	368905	4	CEC	ECU V1H 104ZFX
UP-0670	C801-C802	368905	2	CEC	ECU V1H 104ZFX
UP-0670	C803	159748	1	CEC	GRM39SL 470K50PT 50V 47PF
UP-0670	C804	071138	1	FLC	ECQ-V 1H 224JZ3 (0.22MF)
UP-0670	C812	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0670	C813-C816	070977	4	FLC	ECQ-B 1H 153JZ3 0.015MF
UP-0670	C817	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0670	C818-C819	070977	2	FLC	ECQ-B 1H 153JZ3 0.015MF
UP-0670	C822	070879	1	FLC	ECQ-B1H222JZ3 50V 0.0022UF
UP-0670	C823-C826	070923	4	FLC	ECQ-B 1H 562JZ3 0.0056MF
UP-0670	C827	070879	1	FLC	ECQ-B1H222JZ3 50V 0.0022UF
UP-0670	C828-C829	070923	2	FLC	ECQ-B 1H 562JZ3 0.0056MF
UP-0670	C831-C832	071138	2	FLC	ECQ-V 1H 224JZ3 (0.22MF)
UP-0670	C833	071058	1	FLC	ECQ-V 1H 473JZ3 (0.047MF)
UP-0670	C834-C837	071138	4	FLC	ECQ-V 1H 224JZ3 (0.22MF)
UP-0670	C838	071058	1	FLC	ECQ-V 1H 473JZ3 (0.047MF)
UP-0670	C901	070879	1	FLC	ECQ-B1H222JZ3 50V 0.0022UF
UP-0670	C902-C905	159632	4	TAC	267M2002 106MR533 10MF20V
UP-0670	C906	071174	1	FLC	ECQ-V 1H 474JZ3 (0.47MF)
UP-0670	C907	070834	1	FLC	ECQ-B 1H 102JZ3 0.001MF
UP-0670	C908-C910	071058	3	FLC	ECQ-V 1H 473JZ3 (0.047MF)
UP-0670	C911	070977	1	FLC	ECQ-B 1H 153JZ3 0.015MF
UP-0670	C912	070923	1	FLC	ECQ-B 1H 562JZ3 0.0056MF
UP-0670	C913	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0670	C914	070834	1	FLC	ECQ-B 1H 102JZ3 0.001MF
UP-0670	C915-C917	071058	3	FLC	ECQ-V 1H 473JZ3 (0.047MF)
UP-0670	C918	070977	1	FLC	ECQ-B 1H 153JZ3 0.015MF
UP-0670	C919	070923	1	FLC	ECQ-B 1H 562JZ3 0.0056MF
UP-0670	C920	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0670	C921	070879	1	FLC	ECQ-B1H222JZ3 50V 0.0022UF
UP-0670	C922-C925	159632	4	TAC	267M2002 106MR533 10MF20V
UP-0670	C926	071174	1	FLC	ECQ-V 1H 474JZ3 (0.47MF)
UP-0670	C927	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0670	C928-C929	159632	2	TAC	267M2002 106MR533 10MF20V
UP-0670	C930	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0670	DA921	003613	1	D	DAN401
UP-0670	DA922	003604	1	D	DAP401
UP-0670	D001-D002	071548	2	D	1S2076A RE
UP-0670	D201	071548	1	D	1S2076A RE
UP-0670	D711-D714	071539	4	D	1SS104,TPB2
UP-0670	D901-D902	071557	2	D	1SS106RE schottky
UP-0670	D903-D904	071539	2	D	1SS104,TPB2
UP-0670	D905-D906	071557	2	D	1SS106RE schottky
UP-0670	D907-D908	071539	2	D	1SS104,TPB2
UP-0670	IC101	013941	1	CPU	TMP68HC000N-16
UP-0670	IC102	013718	1	CPU	HN27C1024HG-85 1MBIT(X16)
UP-0670	IC103-IC104	448089	2	RAM	HM62256BLFP-8TZ
UP-0670	IC105	161317	1	TTL	74F04SJ
UP-0670	IC106	161326	1	TTL	74F32SJ
UP-0670	IC111-IC112	161353	2	TTL	74F138SJ
UP-0670	IC113	161772	1	CMOS	HD74HCT138FP
UP-0670	IC114	161371	1	TTL	SN74LS09NS
UP-0670	IC116	161433	1	TTL	SN74LS01 NS
UP-0670	IC117	161398	1	TTL	74F74SJ
UP-0670	IC118	161353	1	TTL	74F138SJ
UP-0670	IC131	161638	1	TTL	74F00SJ
UP-0670	IC132	323018	1	TTL	SN74LS11NS

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0670	IC133	161736	1	TTL	74F27SJ
UP-0670	IC134	161326	1	TTL	74F32SJ
UP-0670	IC135-IC136	161406	2	TTL	74F08SJ
UP-0670	IC201	161317	1	TTL	74F04SJ
UP-0670	IC202-IC204	161736	3	TTL	74F27SJ
UP-0670	IC205	161406	1	TTL	74F08SJ
UP-0670	IC206	161389	1	TTL	74F164SJ
UP-0670	IC207	161629	1	TTL	74F158SJ
UP-0670	IC208	161389	1	TTL	74F164SJ
UP-0670	IC209	161638	1	TTL	74F00SJ
UP-0670	IC210	161398	1	TTL	74F74SJ
UP-0670	IC221-IC222	161647	2	CMOS	HD74HCT244FP
UP-0670	IC223-IC224	161415	2	CMOS	HD74HCT240FP
UP-0670	IC225-IC226	161745	2	CPU	HM6264ALFP-15
UP-0670	IC227-IC228	161656	2	TTL	SN74LS245NS
UP-0670	IC229-IC230	161665	2	TTL	SN74LS640NS
UP-0670	IC301	161772	1	CMOS	HD74HCT138FP
UP-0670	IC302	160889	1	CMOS	HD74HC08FP
UP-0670	IC303	160978	1	CMOS	HD74HC74FP
UP-0670	IC304	161273	1	CMOS	HD74HC148FP
UP-0670	IC305	160898	1	CMOS	HD74HC10FP
UP-0670	IC401	161398	1	TTL	74F74SJ
UP-0670	IC402	161674	1	TTL	SN74LS393NS
UP-0670	IC403-IC404	161683	2	TTL	SN74LS390NS
UP-0670	IC405	160871	1	CMOS	HD74HC04FP
UP-0670	IC406	161264	1	CMOS	HD74HC4040FP
UP-0670	IC407	160978	1	CMOS	HD74HC74FP
UP-0670	IC409	160862	1	CMOS	HD74HC02FP
UP-0670	IC410	160853	1	CMOS	HD74HC00FP
UP-0670	IC421	161095	1	CMOS	HD74HC164FP
UP-0670	IC422-IC423	160978	2	CMOS	HD74HC74FP
UP-0670	IC424	160871	1	CMOS	HD74HC04FP
UP-0670	IC425	160889	1	CMOS	HD74HC08FP
UP-0670	IC426	160951	1	CMOS	HD74HC32FP
UP-0670	IC428	161282	1	CMOS	MC14504BF
UP-0670	IC429	160978	1	CMOS	HD74HC74FP
UP-0670	IC430	160951	1	CMOS	HD74HC32FP
UP-0670	IC501	160862	1	CMOS	HD74HC02FP
UP-0670	IC502-IC505	161291	4	CMOS	u PD74HC4094GS
UP-0670	IC507-IC510	161754	4	CMOS	HD74HC597FP
UP-0670	IC601-IC602	161647	2	CMOS	HD74HCT244FP
UP-0670	IC603-IC605	161219	3	CMOS	HD74HC374FP
UP-0670	IC606	161442	1	CPU	FRAMSYNC1208631
UP-0670	IC607	160951	1	CMOS	HD74HC32FP
UP-0670	IC608	161371	1	TTL	SN74LS09NS
UP-0670	IC609	161647	1	CMOS	HD74HCT244FP
UP-0670	IC701-IC704	323099	4	OPIC	u PC458G2
UP-0670	IC705-IC706	161763	2	CMOS	JLC1133F (MC14051 inspected)
UP-0670	IC711-IC715	160265	5	OPIC	u PC812G2
UP-0670	IC716-IC717	161763	2	CMOS	JLC1133F (MC14051 inspected)
UP-0670	IC721	160265	1	OPIC	u PC812G2
UP-0670	IC722	160407	1	REG	LT1009S8
UP-0670	IC723	161763	1	CMOS	JLC1133F (MC14051 inspected)
UP-0670	IC724	015886	1	IC	UPC-649C (sample hold)
UP-0670	IC725	016653	1	ADIC	ADC574AJH 12BITADC BB
UP-0670	IC726	323152	1	RAM	MB8421-90LPFQ-G 2port RAM
UP-0670	IC801-IC802	161219	2	CMOS	HD74HC374FP
UP-0670	IC803	016092	1	ADIC	HA-17012PB 12BIT DA
UP-0670	IC804	160265	1	OPIC	u PC812G2
UP-0670	IC805	161282	1	CMOS	MC14504BF
UP-0670	IC806	161763	1	CMOS	JLC1133F (MC14051 inspected)
UP-0670	IC807-IC810	160265	4	OPIC	u PC812G2
UP-0670	IC811	161291	1	CMOS	u PD74HC4094GS
UP-0670	IC812-IC813	160265	2	OPIC	u PC812G2
UP-0670	IC814	160586	1	CMOS	MC14053BF
UP-0670	IC815	160265	1	OPIC	u PC812G2
UP-0670	IC901	160586	1	CMOS	MC14053BF
UP-0670	IC902-IC903	160265	2	OPIC	u PC812G2
UP-0670	IC904-IC905	160586	2	CMOS	MC14053BF
UP-0670	IC906-IC907	160256	2	OPIC	u PC811G2
UP-0670	IC908-IC909	160265	2	OPIC	u PC812G2
UP-0670	IC910	160586	1	CMOS	MC14053BF
UP-0670	IC911	160265	1	OPIC	u PC812G2
UP-0670	IC912	010071	1	TR	TD62004P
UP-0670	IC913	160265	1	OPIC	u PC812G2
UP-0670	IC921	161193	1	CMOS	HD74HC367FP
UP-0670	IC922	160354	1	REG	HA178L15UATR
UP-0670	IC923	160399A	1	REG	HA179L15UTR
UP-0670	LED601-LED608	342497	8	LED	GL3AR8 red
UP-0670	L101	316882	1	NFLT	ferrite beads BL02RN2-R62
UP-0670	SKT102	356606	1	CN	AXS204011(u -IC socket 40pin)
UP-0670	SW101	032484	1	SW	SKHCAD (KHC-10904)
UP-0670	SW601	031039	1	DSW	B-4A-T

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0670	SW602	317319	1	SW	ATE1D-6M3-10
UP-0670	VR101	159873	1	POT	G4AT F76010 KOHM
UP-0670	VR102	159846	1	POT	G4AT 1 KOHM
UP-0670	VR103	159828	1	POT	G4AT 200 OHM
UP-0670	VR104-VR105	159819	2	POT	G4AT 100 OHM
UP-0670	VR106-VR107	159873	2	POT	G4AT 10 KOHM
UP-0670	VR108-VR109	159882	2	POT	G4AT 20 KOHM
UP-0670	VR110	159837	1	POT	G4AT 500 OHM
UP-0670	X101	024297	1	XTAL	TD308C 32MHZ CRISTAL

UP-0795 CRTC (CRT CONTROL) BOARD

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0795	CN101	089957	1	PCN	PCN10EA-90P-2.54DS(05)
UP-0795	CN102	354359	1	CN	DX10M-26SE
UP-0795	CN103	081118	1	CN	RDAD-15SE-LNA
UP-0795	CN104	089912	1	PCN	PCN10EA-32P-2.54DS(05)
UP-0795	C001-C004	159641	4	TAC	267M2002 226MR533 22MF20V
UP-0795	C005-C107	368905	103	CEC	ECU V1H 104ZFX
UP-0795	C201-C202	159659	2	TAC	267M3502 105MR 1MF35V
UP-0795	C701-C702	368905	2	CEC	ECU V1H 104ZFX
UP-0795	C703-C704	159632	2	TAC	267M2002 106MR533 10MF20V
UP-0795	C705	368905	1	CEC	ECU V1H 104ZFX
UP-0795	C706	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0795	D703	160078	1	D	HSK120TR
UP-0795	FIL601	367381	1	NFLT	NFM61R30T472T1
UP-0795	FIL700-FIL702	367381	3	NFLT	NFM61R30T472T1
UP-0795	FIL703-FIL713	334149	11	NFLT	NFM52R20P506
UP-0795	FIL720	367381	1	NFLT	NFM61R30T472T1
UP-0795	FIL721-FIL736	341489	16	NFLT	BLM21A05PT
UP-0795	IC101-IC102	334096	2	CMOS	TD74BC640F
UP-0795	IC103-IC104	334087	2	CMOS	TD74BC240F
UP-0795	IC105-IC106	357445	2	CMOS	TC74AC175F
UP-0795	IC107	357409	1	CMOS	74ACT138SJ
UP-0795	IC109	334042	1	CMOS	HD74AC125FP
UP-0795	IC110	333836	1	CMOS	74AC04SJ
UP-0795	IC201	333916	1	CRTC	HD63484CP98
UP-0795	IC202-IC203	149937A	2	CMOS	74AC373SJ(CD74AC373M) SOP
UP-0795	IC206-IC207	149901A	2	CMOS	74AC74SJ(CD74AC74M) (SOP)
UP-0795	IC208	333836	1	CMOS	74AC04SJ
UP-0795	IC209, 211, 213, 215	334158A	4	RAM	TC528257J-80
UP-0795	IC217	357418	1	CMOS	HD74AC164FP
UP-0795	IC301-IC302	333854	2	CMOS	74AC244SJ
UP-0795	IC303-IC310	448089	8	RAM	HM62256BLFP-8TZ
UP-0795	IC311-IC318	357454	8	CMOS	TC74AC245F
UP-0795	IC319-IC322	013745A	4	CPU	gate array DCW
UP-0795	IC323-IC328	357463	6	CMOS	TC74AC374F
UP-0795	IC333	013754A	1	CPU	gate array ACW
UP-0795	IC334-IC336	357463	3	CMOS	TC74AC374F
UP-0795	IC338	333845	1	CMOS	74AC139SJ
UP-0795	IC339	333854	1	CMOS	74AC244SJ
UP-0795	IC344	149901A	1	CMOS	74AC74SJ(CD74AC74M) (SOP)
UP-0795	IC345	357418	1	CMOS	HD74AC164FP
UP-0795	IC346	149901A	1	CMOS	74AC74SJ(CD74AC74M) (SOP)
UP-0795	IC347	333863	1	CMOS	74AC08SJ
UP-0795	IC348-IC395	333907	48	RAM	HM53461JP-12
UP-0795	IC396-IC407	334069	12	CMOS	TC74AC299F
UP-0795	IC408	333854	1	CMOS	74AC244SJ
UP-0795	IC409	149901A	1	CMOS	74AC74SJ(CD74AC74M) (SOP)
UP-0795	IC502-IC503	333952	2	RAM	MB8441-55 QFP
UP-0795	IC504-IC505	149937A	2	CMOS	74AC373SJ(CD74AC373M) SOP
UP-0795	IC506-IC507	357436	2	CMOS	74AC174SJ
UP-0795	IC508-IC509	161264	2	CMOS	HD74HC4040FP
UP-0795	IC510	161237	1	CMOS	HD74HC390FP
UP-0795	IC514	334015	1	CMOS	HD74AC166FP
UP-0795	IC516	357418	1	CMOS	HD74AC164FP
UP-0795	IC520	161264	1	CMOS	HD74HC4040FP
UP-0795	IC521	357418	1	CMOS	HD74AC164FP
UP-0795	IC601	161317	1	TTL	74F04SJ
UP-0795	IC602	333997	1	TTL	74F163SJ
UP-0795	IC603	333988	1	TTL	74F175SJ
UP-0795	IC604	161398	1	TTL	74F74SJ
UP-0795	IC605	333702	1	CMOS	HD74HC273FP
UP-0795	IC606	161193	1	CMOS	HD74HC367FP
UP-0795	IC701	333925	1	CRTC	ADV471KP66
UP-0795	IC704	161469	1	TTL	SN74LS06 NS
UP-0795	IC705	334078	1	CMOS	TD74BC244F
UP-0795	IC707	160363	1	REG	HA179L05UTR
UP-0795	IC708	334113A	1	REG	LT1004CS8-1.2
UP-0795	Q701-Q707	334122A	7	TR	2SC3735-T2B
UP-0795	SK513	356598	1	CN	AXS202811(u-IC socket 28pin)
UP-0795	VC601	047637	1	VC	TZ03R 300ER 5.2-30PF

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0795	X601	354368	1	XTAL	1349-M1 64MHZ

UP-0797 I / O BOARD

UP-0797	CN101	089957	1	PCN	PCN10EA-90P-2.54DS(05)
UP-0797	CN102	089912	1	PCN	PCN10EA-32P-2.54DS(05)
UP-0797	CN103	089725	1	PCN	M60-06-30-134P (6P)
UP-0797	CN104	085934	1	PCN	HIF3BA-40PA-2.54DS
UP-0797	CN105	081092	1	CN	RDCD-37SE-LNA
UP-0797	CN106	089672	1	PCN	M60-06-30-114P (6P)
UP-0797	CN201	356767	1	PCN	HIF-6-68PA-1.27DS
UP-0797	CN401	091072	1	PCN	TCS7587-01-401
UP-0797	C101-C104	331134	4	FLC	ECW-U1H103JA5 50V 0.01UF
UP-0797	C105-C106	159632	2	TAC	267M2002 106MR533 10MF20V
UP-0797	C151-C160	368905	10	CEC	ECU V1H 104ZFX
UP-0797	C301-C304	331107	4	FLC	ECW-U1H223JA5 50V 0.022UF
UP-0797	C305	159641	1	TAC	267M2002 226MR533 22MF20V
UP-0797	C306	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0797	C307	159677	1	TAC	267M3502 475MR 4.7MF35V
UP-0797	C308	159748	1	CEC	GRM39SL 470K50PT 50V 47PF
UP-0797	C309	159677	1	TAC	267M3502 475MR 4.7MF35V
UP-0797	C310	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0797	C311-C312	357801	2	FLC	ECW-U1H104JB9 50V 0.1UF
UP-0797	C313	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UP-0797	C314-C315	341471	2	FLC	ECW-U1H473JA5 50V 0.047UF
UP-0797	C316-C319	357801	4	FLC	ECW-U1H104JB9 50V 0.1UF
UP-0797	C320-C322	159784	3	CEC	GRM39SL 331K50PT 330PF50V
UP-0797	C323-C324	159739	2	CEC	GRM39SL 330K50PT 50V 33PF
UP-0797	C325	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0797	C401-C408	159695	8	TAC	267M3502 106MR720 10MF35V
UP-0797	C409	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0797	C410-C411	159739	2	CEC	GRM39SL 330K50PT 50V 33PF
UP-0797	C412	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0797	C413	368905	1	CEC	ECU V1H 104ZFX
UP-0797	C414	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UP-0797	C415	357801	1	FLC	ECW-U1H104JB9 50V 0.1UF
UP-0797	C416	159659	1	TAC	267M3502 105MR 1MF35V
UP-0797	C417	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0797	C451-C454	368905	4	CEC	ECU V1H 104ZFX
UP-0797	C601-C602	159632	2	TAC	267M2002 106MR533 10MF20V
UP-0797	C603-C642	368905	40	CEC	ECU V1H 104ZFX
UP-0797	D301	160078	1	D	HSK120TR
UP-0797	D302	005389	1	ZD	HZ2C1
UP-0797	D401-D402	160104	2	D	HSM123 TR
UP-0797	D403-D410	357597	8	LED	LT1L51A
UP-0797	D411-D412	160096	2	D	1SS294 TE85R
UP-0797	FIL101-FIL104	323223	4	NFLT	BLA81A01T1
UP-0797	FIL105-FIL107	323232	3	NFLT	NFM61T20T472T1
UP-0797	FIL201-FIL207	323223	7	NFLT	BLA81A01T1
UP-0797	FIL208	323232	1	NFLT	NFM61T20T472T1
UP-0797	FIL401	323223	1	NFLT	BLA81A01T1
UP-0797	FIL402-FIL403	323232	2	NFLT	NFM61T20T472T1
UP-0797	IC101	160256	1	OPIC	u PC811G2
UP-0797	IC102	160238	1	OPIC	u PC1458G2
UP-0797	IC103	160256	1	OPIC	u PC811G2
UP-0797	IC104	161469	1	TTL	SN74LS06
UP-0797	IC201-IC202	161424	2	CMOS	u PD74HCT640GS
UP-0797	IC203-IC205	161415	3	CMOS	HD74HCT240FP
UP-0797	IC206	161023	1	CMOS	HD74HC138FP
UP-0797	IC208	161647	1	CMOS	HD74HCT244FP
UP-0797	IC209-IC210	357507	2	CMOS	HD74HCT245FP
UP-0797	IC211-IC214	161219	4	CMOS	HD74HC374FP
UP-0797	IC301-IC302	323036	2	CMOS	HD74HC 14FP
UP-0797	IC303	160871	1	CMOS	HD74HC04FP
UP-0797	IC304-IC308	161112	5	CMOS	HD74HC174FP
UP-0797	IC309	160853	1	CMOS	HD74HC00FP
UP-0797	IC310	160817	1	CMOS	MC14538BF
UP-0797	IC311	370225	1	CPU	u PD75004GB-777-3B4
UP-0797	IC312	160817	1	CMOS	MC14538BF
UP-0797	IC313	160229A	1	OPIC	u PC358G2-E2
UP-0797	IC314	160586	1	CMOS	MC14053BF
UP-0797	IC315	015431	1	CMOS	melody IC 7910I
UP-0797	IC316	160265	1	OPIC	u PC812G2
UP-0797	IC317	160586	1	CMOS	MC14053BF
UP-0797	IC318	160265	1	OPIC	u PC812G2
UP-0797	IC319	160586	1	CMOS	MC14053BF
UP-0797	IC320	160265	1	OPIC	u PC812G2
UP-0797	IC401	160978	1	CMOS	HD74HC74FP
UP-0797	IC403	161095	1	CMOS	HD74HC164FP
UP-0797	IC404	323205	1	CPU	u PD72001GC-3B6
UP-0797	IC405	161469	1	TTL	SN74LS06 NS

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0797	IC406-IC407	161023	2	CMOS	HD74HC138FP
UP-0797	IC408	323205	1	CPU	u PD72001GC-3B6
UP-0797	IC409	161647	1	CMOS	HD74HCT244FP
UP-0797	IC410-IC411	334202	2	ADIC	MAX232CWE-T
UP-0797	IC412	160871	1	CMOS	HD74HC04FP
UP-0797	IC413	370225	1	CPU	u PD75004GB-777-3B4
UP-0797	IC414	161692	1	ADIC	TL7705ACPS
UP-0797	IC415	161219	1	CMOS	HD74HC374FP
UP-0797	IC417	161469	1	TTL	SN74LS06 NS
UP-0797	IC418	323036	1	CMOS	HD74HC 14FP
UP-0797	IC419	161264	1	CMOS	HD74HC4040FP
UP-0797	IC420	160978	1	CMOS	HD74HC74FP
UP-0797	IC421	160817	1	CMOS	MC14538BF
UP-0797	IC422	161219	1	CMOS	HD74HC374FP
UP-0797	IC501-IC503	160951	3	CMOS	HD74HC32FP
UP-0797	IC504	160889	1	CMOS	HD74HC08FP
UP-0797	IC505-IC508	334185	4	CMOS	HD74HC595FP
UP-0797	IC511-IC512	161166	2	CMOS	HD74HC244FP
UP-0797	Q301	160149	1	TR	2SC2618 D TR
UP-0797	Q302	160122	1	TR	2SA1122 CORD TR
UP-0797	VR101	159873	1	POT	G4AT 10 KOHM
UP-0797	VR102	159837	1	POT	G4AT 500 OHM
UP-0797	VR103	159873	1	POT	G4AT 10 KOHM
UP-0797	VR104	159837	1	POT	G4AT 500 OHM
UP-0797	X301	357552	1	XTAL	CSAC 4.19MGCM-TC ceramic oscillator
UP-0797	X401	357552	1	XTAL	CSAC 4.19MGCM-TC ceramic oscillator

UP-0798 MOTHER BOARD

UP-0798	CN101-CN105	089966	5	PCN	PCN10EA-90S-2.54DSA(05)
UP-0798	CN106-CN110	089921	5	PCN	PCN10EA-32S-2.54DSA(05)
UP-0798	CN111	268069	1	PCN	171457-1
UP-0798	CN112	090206	1	PCN	M60-02-30-114P (2P)
UP-0798	CN113	091232A	1	PCN	FFC-20BSM1#02ST
UP-0798	C101-C102	046861	2	C	EECF5R5U105 1F/5.5V
UP-0798	D101	160078	1	D	HSK120TR
UP-0798	FIL001	341489	1	NFLT	BLM21A05PT
UP-0798	FIL002	367381	1	NFLT	NFM61R30T472T1
UP-0798	FIL003-FIL007	341489	5	NFLT	BLM21A05PT

UP-0799 MEMORY CARD BOARD

UP-0799	CN101	356767	1	PCN	HIF-6-68PA-1.27DS
UP-0799	CN102	352628	1	PCN	JC20EA-J68P-V4LT-A1
UP-0799	D101	356838	1	LED	HLMP-5050 green
UP-0799	FIL101-FIL108	341489	8	NFLT	BLM21A05PT
UP-0799	FIL109-FIL110	367381	2	NFLT	NFM61R30T472T1
UP-0799	FIL111-FIL164	341489	54	NFLT	BLM21A05PT

UP-0801 OPERATION CONTROL BOARD

UP-0801	CN101	356829	1	CN	DX20M-26S
UP-0801	CN102	081083	1	CN	HD-LNA D sub lock fitting
UP-0801	CN102	362724	1	CN	SDAB-15S-SL-LNK(02)
UP-0801	CN103	081118	1	CN	RDAD-15SE-LNA
UP-0801	CN104	085899	1	PCN	HIF3BA-20PA-2.54DSA
UP-0801	CN105	089663	1	PCN	M60-03-30-114P (3P)
UP-0801	CN106	369441	1	PCN	HR212-10RB-8SD
UP-0801	CN107	091205A	1	PCN	FFC-14BSM1#02ST
UP-0801	CN108	356785	1	PCN	HR212-10R-5SD(02)
UP-0801	C201-C202	159695	2	TAC	267M3502 106MR720 10MF35V
UP-0801	C203	368905	1	CEC	ECU V1H 104ZFX
UP-0801	C204	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0801	C205-C206	159695	2	TAC	267M3502 106MR720 10MF35V
UP-0801	C207	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0801	C208-C211	159739	4	CEC	GRM39SL 330K50PT 50V 33PF
UP-0801	C301	159766	1	CEC	GRM39SL 101K50PT 100PF50V
UP-0801	C302	159748	1	CEC	GRM39SL 470K50PT 50V 47PF
UP-0801	C303	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0801	C304	350728	1	EC	ECEA1VU101 35V100M
UP-0801	C305	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0801	C306	159695	1	TAC	267M3502 106MR720 10MF35V
UP-0801	C307	368905	1	CEC	ECU V1H 104ZFX
UP-0801	C308	350728	1	EC	ECEA1VU101 35V100M
UP-0801	C309	159739	1	CEC	GRM39SL 330K50PT 50V 33PF
UP-0801	C310	350728	1	EC	ECEA1VU101 35V100M

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0801	C311	159739	1	CEC	GRM39SL 330K50PT 50V 33PF
UP-0801	C312-C313	331107	2	FLC	ECW-U1H223JA5 50V 0.022UF
UP-0801	C314-C315	159632	2	TAC	267M2002 106MR533 10MF20V
UP-0801	C316-C317	159695	2	TAC	267M3502 106MR720 10MF35V
UP-0801	C318-C327	368905	10	CEC	ECU V1H 104ZFX
UP-0801	C328	159766	1	CEC	GRM39SL 101K50PT 100PF50V
UP-0801	C330	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0801	C331-C333	368905	3	CEC	ECU V1H 104ZFX
UP-0801	C401	368905	1	CEC	ECU V1H 104ZFX
UP-0801	C402	159695	1	TAC	267M3502 106MR720 10MF35V
UP-0801	D101-D108	334461	8	D	HSK83 TR
UP-0801	D109-D116	160078	8	D	HSK120TR
UP-0801	D119-D120	160078	2	D	HSK120TR
UP-0801	D121-D122	160096	2	D	1SS294 TE85R
UP-0801	D401-D402	160078	2	D	HSK120TR
UP-0801	FIL101-FIL112	334149	12	NFLT	NFM52R20P506
UP-0801	FIL120-FIL127	341489	8	NFLT	BLM21A05PT
UP-0801	FIL136	334149	1	NFLT	NFM52R20P506
UP-0801	IC101	161469	1	TTL	SN74LS06 NS
UP-0801	IC104	160586	1	CMOS	MC14053BF
UP-0801	IC201	370243A	1	CPU	u PD78214GC-414-AB8
UP-0801	IC202	334202	1	ADIC	MAX232CWE-T
UP-0801	IC203	161469	1	TTL	SN74LS06 NS
UP-0801	IC204	374168	1	CPU	u PD75402AGB-543-3B4
UP-0801	IC205	161692	1	ADIC	TL7705ACPS
UP-0801	IC301	160265	1	OPIC	u PC812G2
UP-0801	IC302	010801	1	ADIC	u PC1316C AUDIO AMP
UP-0801	IC303	160265	1	OPIC	u PC812G2
UP-0801	IC402	160336	1	REG	HA178L08UATR
UP-0801	IC403	160372	1	REG	HA179L08UATR
UP-0801	IC404	160265	1	OPIC	u PC812G2
UP-0801	Q101-Q106	334443	6	TR	2SA1213-Y TE12R
UP-0801	Q107	160122	1	TR	2SA1122 CORD TR
UP-0801	RY101-RY103	356847	3	RY	G6A-274P-ST-US 5V
UP-0801	SW201	357605	1	DSW	CHS-04TB
UP-0801	X102	357552	1	XTAL	CSAC 4.19MGCM-TCceramic oscillator

UP-0802 ORERATION (VR) BOARD

UP-0802	CN101	085899	1	PCN	HIF3BA-20PA-2.54DSA
UP-0802	CN102	313377	1	PCN	B5B-EH
UP-0802	CN103	085515	1	PCN	HKP-6ML-3BT
UP-0802	D101	160078	1	D	HSK120TR
UP-0802	IC105	160336	1	REG	HA178L08UATR
UP-0802	Q101-Q102	160149	2	TR	2SC2618 D TR
UP-0802	VR101-VR102	357819	2	VR	EVJ-02AF15B14 10K OHM
UP-0802	VR103	359942	1	VR	RA12S 10K OHM
UP-0802	VR105	359951	1	VR	EVJ-02AF15B53 5K OHM

UP-0806 LED BOARD

UP-0806	CN101	085515	1	PCN	HKP-6ML-3BT
UP-0806	C101	368905	1	CEC	ECU V1H 104ZFX
UP-0806	C102	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0806	IC101	357837	1	IC	SBX1610-52
UP-0806	LED101-LED102	006245	2	LED	LT-9000N (yellow-green)

UP-0807 CONNECTOR BOARD

UP-0807	CN101	091232A	1	PCN	FFC-20BSM1#02ST
UP-0807	CN102	092775	1	CN	jackHLJ0527-01-030 with nut
UP-0807	CN103	094497	1	CN	HLJ2308-01-3030
UP-0807	CN104	356811	1	PCN	HR212-10RA-8SDL(03)
UP-0807	D101-D102	007075	2	LED	GL3KG8 3 green
UP-0807	SW101	360004	1	PSW	SKHHLR
UP-0807		105147	2	LAMP	PC PCL-490

UP-0813 REGULATOR BOARD

UP-0813	CN102	083401	1	PCN	172034-1
UP-0813	CN103	090206	1	PCN	M60-02-30-114P (2P)
UP-0813	CN105	268069	1	PCN	171457-1
UP-0813	C109	243069	1	FLC	ECQ-V1H104JZ 50V 0.1UF
UP-0813	C111	325702	1	EC	ECEA1HGE010

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0813	C112	044818	1	FLC	ECQ-V1H224JZ 50V 0.22UF
UP-0813	C120-C121	325702	2	EC	ECEA1HGE010
UP-0813	D103-D105	003649	3	D	1SS81
UP-0813	D106	005362	1	ZD	HZ6LB1
UP-0813	D109-D110	003649	2	D	1SS81
UP-0813	D112	003943	1	D	V06C (1.1A200V)
UP-0813	D113-D117	003649	5	D	1SS81
UP-0813	D120-D121	003649	2	D	1SS81
UP-0813	F103-F106	346207	4	FUSE	23902.5 LITTLE
UP-0813	IC101	021674	1	HIC	SWC-01
UP-0813	IC102	195245	1	REG	UPC7808H
UP-0813	IC103	015788	1	REG	UPC7908H
UP-0813	L101	035891	1	COIL	SKP-5-50 5A 150UH
UP-0813	L103-L104	037791	2	COIL	2643-000301
UP-0813	Q103	071922	1	TR	2SA1015-Y,TPE2 (2SA495)
UP-0813	Q105	002356	1	TR	2SD717-Y
UP-0813	Q107	002026	1	TR	2SC2324K
UP-0813	Q109-Q110	072003	2	TR	2SC1815-Y,TPE2 (2SC372)
UP-0813	Q114-Q115	072003	2	TR	2SC1815-Y,TPE2 (2SC372)
UP-0813	R103	156573	1	R	ERG-1SJ 470
UP-0813	VR101	062781	1	VR	GF06P 1 KOHM
UP-0813	VR102	062923	1	VR	GF06P 200 OHM
UP-0813	VR103	062781	1	VR	GF06P 1 KOHM

UR-3023 CPU BOARD (with ROM)

UR-3023	BAT101	105842	1	BATT	CR17335SE-T-C7 lithium battery 3V
UR-3023	CN101	089957	1	PCN	PCN10EA-90P-2.54DS(05)
UR-3023	CN102	089912	1	PCN	PCN10EA-32P-2.54DS(05)
UR-3023	CN103	081109	1	CN	RDBD-25SE-LNA
UR-3023	CN104	092864	1	PCN	IL-2P-S3FP2-1
UR-3023	C101	159641	1	TAC	267M2002 226MR533 22MF20V
UR-3023	C102	368905	1	CEC	ECU V1H 104ZFX
UR-3023	C103	159632	1	TAC	267M2002 106MR533 10MF20V
UR-3023	C104	357801	1	FLC	ECW-U1H104JB9 50V 0.1UF
UR-3023	C105	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UR-3023	C106	159632	1	TAC	267M2002 106MR533 10MF20V
UR-3023	C107	159721	1	CEC	GRM39SL 220K50PT 50V 22PF
UR-3023	C109	159632	1	TAC	267M2002 106MR533 10MF20V
UR-3023	C110-C119	368905	10	CEC	ECU V1H 104ZFX
UR-3023	C122-C124	159632	3	TAC	267M2002 106MR533 10MF20V
UR-3023	C125-C141	368905	17	CEC	ECU V1H 104ZFX
UR-3023	C142-C149	159695	8	TAC	267M3502 106MR720 10MF35V
UR-3023	D101	160087	1	D	1SS307 TE85R
UR-3023	D102	160096	1	D	1SS294 TE85R
UR-3023	D103	071637	1	ZD	HZ3C3TE (3.3-3.5V)
UR-3023	D104	003667	1	D	HP5082-2835
UR-3023	D107-D108	160087	2	D	1SS307 TE85R
UR-3023	FIL101-FIL104	334149	4	NFLT	NFM52R20P506
UR-3023	IC101	013941	1	CPU	TMP68HC000N-16
UR-3023	IC102	161398	1	TTL	74F74SJ
UR-3023	IC104	357427	1	CMOS	TC74ACT164F
UR-3023	IC105	357472	1	CMOS	HD74AC393FP
UR-3023	IC111	357409	1	CMOS	74ACT138SJ
UR-3023	IC112	161709	1	CMOS	74AC138SJ
UR-3023	IC113	357409	1	CMOS	74ACT138SJ
UR-3023	IC114	333863	1	CMOS	74AC08SJ
UR-3023	IC115	161594	1	TTL	SN74LS27NS
UR-3023	IC116	161692	1	ADIC	TL7705ACPS
UR-3023	IC117	323027	1	CMOS	HD74HC123AFP
UR-3023	IC118	160978	1	CMOS	HD74HC74FP
UR-3023	IC119	160889	1	CMOS	HD74HC08FP
UR-3023	IC120	357525	1	TTL	74F14SJ
UR-3023	IC121	352192	1	CMOS	HD74HC01FP
UR-3023	IC122	357499	1	CMOS	HD74HC21FP
UR-3023	IC123	161772	1	CMOS	HD74HCT138FP
UR-3023	IC124	160889	1	CMOS	HD74HC08FP
UR-3023	IC125-IC126	160978	2	CMOS	HD74HC74FP
UR-3023	IC127	161273	1	CMOS	HD74HC148FP
UR-3023	IC128	160889	1	CMOS	HD74HC08FP
UR-3023	IC129	160978	1	CMOS	HD74HC74FP
UR-3023	IC130	359906	1	CMOS	HD74HCT534FP
UR-3023	IC131	161273	1	CMOS	HD74HC148FP
UR-3023	IC132	161415	1	CMOS	HD74HCT240FP
UR-3023	IC133	161772	1	CMOS	HD74HCT138FP
UR-3023	IC134-IC135	160889	2	CMOS	HD74HC08FP
UR-3023	IC136-IC139	160978	4	CMOS	HD74HC74FP
UR-3023	IC140	357516	1	CMOS	HD74HCT374FP
UR-3023	IC141	161273	1	CMOS	HD74HC148FP
UR-3023	IC142	161415	1	CMOS	HD74HCT240FP
UR-3023	IC143	161772	1	CMOS	HD74HCT138FP

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UR-3023	IC148	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC150	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC152	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC154	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC156	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC158	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC160	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC162	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC168	323045	1	CMOS	HD74HC132FP
UR-3023	IC169	323179A	1	CPU	MSM6242GS-VKR2
UR-3023	IC170	323188A	1	CPU	HM58C65FP-25 TZ
UR-3023	IC172	365302	1	CPU	TMP82C51AM-10(CELZ
UR-3023	IC173	323197	1	CPU	u PD71054GB-3B4
UR-3023	IC174-IC175	334202	2	ADIC	MAX232CWE-T
UR-3023	IC176	357623	1	CPU	TMP82C79M-2
UR-3023	IC177	333827	1	CMOS	74AC32SJ
UR-3023	IC178	160309	1	ADIC	HA17903FP
UR-3023	IC179-IC180	161415	2	CMOS	HD74HCT240FP
UR-3023	IC181	161255	1	CMOS	HD74HC534FP
UR-3023	IC182-IC184	357481	3	CMOS	TD74BC533F
UR-3023	IC185-IC186	334096	2	CMOS	TD74BC640F
UR-3023	IC187-IC188	161415	2	CMOS	HD74HCT240FP
UR-3023	IC191	333836	1	CMOS	74AC04SJ
UR-3023	IC192-IC193	149901A	2	CMOS	74AC74SJ(CD74AC74M) (SOP)
UR-3023	IC197-IC198	357418	2	CMOS	HD74AC164FP
UR-3023	IC199	365231	1	CMOS	74AC158SJ
UR-3023	IC200	161469	1	TTL	SN74LS06 NS
UR-3023	IC202	149901A	1	CMOS	74AC74SJ(CD74AC74M) (SOP)
UR-3023	IC203	323036	1	CMOS	HD74HC 14FP
UR-3023	IC204	333854	1	CMOS	74AC244SJ
UR-3023	LED101-LED110	357597	10	LED	LT1L51A
UR-3023	Q101	160149	1	TR	2SC2618 D TR
UR-3023	SKT144	356606	1	CN	AXS204011(u -IC socket 40pin)
UR-3023	SKT146	356606	1	CN	AXS204011(u -IC socket 40pin)
UR-3023	SW102-SW104	357605	3	DSW	CHS-04TB
UR-3023	VC101	047637	1	VC	TZ03R 300ER 5.2-30PF
UR-3023	X101	369887	1	XTAL	1343-M1 32MHZ
UR-3023	X102	022931	1	XTAL	KF-38G

UR-3025 OPERATION RY BOARD

UR-3025	CN101	356811	1	PCN	HR212-10RA-8SDL(03)
UR-3025	C001	159632	1	TAC	267M2002 106MR533 10MF20V
UR-3025	C002-C003	368905	2	CEC	ECU V1H 104ZFX
UR-3025	C005-C006	368905	2	CEC	ECU V1H 104ZFX
UR-3025	C101-C104	159695	4	TAC	267M3502 106MR720 10MF35V
UR-3025	C105	368905	1	CEC	ECU V1H 104ZFX
UR-3025	C106	159632	1	TAC	267M2002 106MR533 10MF20V
UR-3025	C401-C402	159739	2	CEC	GRM39SL 330K50PT 50V 33PF
UR-3025	D101-D108	160078	8	D	HSK120TR
UR-3025	D201-D207	160078	7	D	HSK120TR
UR-3025	D301-D308	160078	8	D	HSK120TR
UR-3025	D401-D403	160078	3	D	HSK120TR
UR-3025	D501-D502	160078	2	D	HSK120TR
UR-3025	D504-D505	160078	2	D	HSK120TR
UR-3025	FIL101-FIL105	341489	5	NFLT	BLM21A05PT
UR-3025	IC101	370243A	1	CPU	u PD78214GC-414-AB8
UR-3025	IC102	334202	1	ADIC	MAX232CWE-T
UR-3025	IC103	161469	1	TTL	SN74LS06 NS
UR-3025	IC104	161692	1	ADIC	TL7705ACPS
UR-3025	LED101-LED102	006593	2	LED	LD101YY
UR-3025	L101	037559	1	COIL	SF-T8-50D 125MH 2A
UR-3025	Q301	334443	1	TR	2SA1213-Y TE12R
UR-3025	SP101	073671	1	SP	EFB-RD24C411
UR-3025	SW101-SW108	032484	8	SW	SKHCAD (KHC-10904)
UR-3025	SW201-SW207	032484	7	SW	SKHCAD (KHC-10904)
UR-3025	SW301-SW308	032484	8	SW	SKHCAD (KHC-10904)
UR-3025	SW401-SW403	032484	3	SW	SKHCAD (KHC-10904)
UR-3025	SW501	357605	1	DSW	CHS-04TB

UR-3105 SpO$_2$ HEAD AMP MAIN BOARD

UR-3105	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UR-3105	CN003	088512	1	PCN	HKP-20FDS2
UR-3105	CN005	319576	1	PCN	HKP-6FD2-3BT
UR-3105	C001	331179A	1	FLC	ECW-U1H472JA5 50V 0.0047UF
UR-3105	C002	159748	1	CEC	GRM39SL 470K50PT 50V 47PF
UR-3105	C003	331179A	1	FLC	ECW-U1H472JA5 50V 0.0047UF

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UR-3105	C004	159748	1	CEC	GRM39SL 470K50PT 50V 47PF
UR-3105	C005	331197A	1	FLC	ECW-U1H332JA5 50V 0.0033UF
UR-3105	C006	339607A	1	FLC	ECW-U1H222JA5 50V 0.0022UF
UR-3105	C008-C009	357801	2	FLC	ECW-U1H104JB9 50V 0.1UF
UR-3105	C010	159712	1	CEC	GRM39SL 100D50PT 50V10PF
UR-3105	C013-C015	368905	3	CEC	ECU V1H 104ZFX
UR-3105	C016-C017	159632	2	TAC	267M2002 106MR533 10MF20V
UR-3105	C018	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UR-3105	C019	331072	1	FLC	ECW-U1H102JA5 50V 0.001UF
UR-3105	C020	331179A	1	FLC	ECW-U1H472JA5 50V 0.0047UF
UR-3105	C021-C022	368905	2	CEC	ECU V1H 104ZFX
UR-3105	C023	070148	1	EC	ECEA1CU101B 16V 100UF
UR-3105	C024	372544	1	CEC	ECKDNS101MBX 100PF
UR-3105	C101-C104	368905	4	CEC	ECU V1H 104ZFX
UR-3105	D001-D004	160078	4	D	HSK120TR
UR-3105	D005-D006	071548	2	D	1S2076A RE
UR-3105	D007-D009	160078	3	D	HSK120TR
UR-3105	FIL001-FIL003	316882	3	NFLT	ferrite beads BL02RN2-R62
UR-3105	GA001	026811	1	TUBE	Y08-2100B
UR-3105	IC001-IC005	160265	5	OPIC	u PC812G2
UR-3105	IC006	160568	1	CMOS	MC14051BF
UR-3105	IC007	160407	1	REG	LT1009S8
UR-3105	IC008	160327	1	REG	HA178L05UATR
UR-3105	IC009	160363	1	REG	HA179L05UTR
UR-3105	IC010	160586	1	CMOS	MC14053BF
UR-3105	IC011	021718	1	HIC	EHD-HA1270 ISOLATE
UR-3105	PC001	002739	1	PTR	PC810A
UR-3105	Q001-Q002	160185	2	TR	2SD1418 DB OR DC TR
UR-3105	Q003-Q004	072066	2	TR	2SC1213AKDTZ
UR-3105	T001	036925	1	TF	T3772365 EP10PS transformer
UR-3105	T002	036916	1	TF	T3772356 EP10IS transformer

UR-3106 SpO_2 HEAD AMP SUB BOARD

UR-3106	CN004	088441	1	PCN	HKP-20M5S
UR-3106	CN006	262075	1	PCN	HKP-6M2-3BT
UR-3106	C030-C032	368905	3	CEC	ECU V1H 104ZFX
UR-3106	C051	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UR-3106	C052	341471	1	FLC	ECW-U1H473JA5 50V 0.047UF
UR-3106	C054	331107	1	FLC	ECW-U1H223JA5 50V 0.022UF
UR-3106	C055	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UR-3106	C056	341471	1	FLC	ECW-U1H473JA5 50V 0.047UF
UR-3106	C058	331107	1	FLC	ECW-U1H223JA5 50V 0.022UF
UR-3106	C059	341471	1	FLC	ECW-U1H473JA5 50V 0.047UF
UR-3106	C060	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UR-3106	C061	341462A	1	FLC	ECW-U1H333JA5 50V 0.033UF
UR-3106	C062	341471	1	FLC	ECW-U1H473JA5 50V 0.047UF
UR-3106	C063	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UR-3106	C064	341462A	1	FLC	ECW-U1H333JA5 50V 0.033UF
UR-3106	C065-C066	331107	2	FLC	ECW-U1H223JA5 50V 0.022UF
UR-3106	C067-C070	159632	4	TAC	267M2002 106MR533 10MF20V
UR-3106	C071-C072	331107	2	FLC	ECW-U1H223JA5 50V 0.022UF
UR-3106	C075-C076	161522	2	CEC	C3216JB1H 103KT 0.01MF
UR-3106	C078	159632	1	TAC	267M2002 106MR533 10MF20V
UR-3106	C079-C080	368905	2	CEC	ECU V1H 104ZFX
UR-3106	C081-C082	159739	2	CEC	GRM39SL 330K50PT 50V 33PF
UR-3106	C083	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UR-3106	C151-C176	368905	26	CEC	ECU V1H 104ZFX
UR-3106	D051-D055	160087	5	D	1SS307 TE85R
UR-3106	D056	160078	1	D	HSK120TR
UR-3106	IC050	160577	1	CMOS	MC14052BF
UR-3106	IC051-IC053	386289	3	OPIC	TLC27M7CPS power sourse
UR-3106	IC054	160265	1	OPIC	u PC812G2
UR-3106	IC056	160595	1	CMOS	MC14066BF
UR-3106	IC057-IC058	160265	2	OPIC	u PC812G2
UR-3106	IC059	160568	1	CMOS	MC14051BF
UR-3106	IC060	160523	1	CMOS	MC14040BF
UR-3106	IC061	160318	1	ADIC	HA17901FP
UR-3106	IC062-IC064	381222	3	CMOS	MC14520BF
UR-3106	IC065-IC066	160568	2	CMOS	MC14051BF
UR-3106	IC067	160844	1	CMOS	MC14584BF
UR-3106	IC068	160701	1	CMOS	MC14081BF
UR-3106	IC069	160452	1	CMOS	MC14011BF
UR-3106	IC070	160416	1	CMOS	MC14001BF
UR-3106	IC071	161264	1	CMOS	HD74HC4040FP
UR-3106	IC072	160889	1	CMOS	HD74HC08FP
UR-3106	IC073	351032A	1	CMOS	TC74HCU04AF
UR-3106	IC075	160327	1	REG	HA178L05UATR
UR-3106	PC050	002739	1	PTR	PC810A
UR-3106	Q050	160149	1	TR	2SC2618 D TR
UR-3106	SW050	380651	1	SW	SW SSSS2-12-11

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UR-3106	X050	381213	1	XTAL	DS-HC-49U3H 4.032MHZ

UP-31551 SpO_2 HEAD AMP BOARD

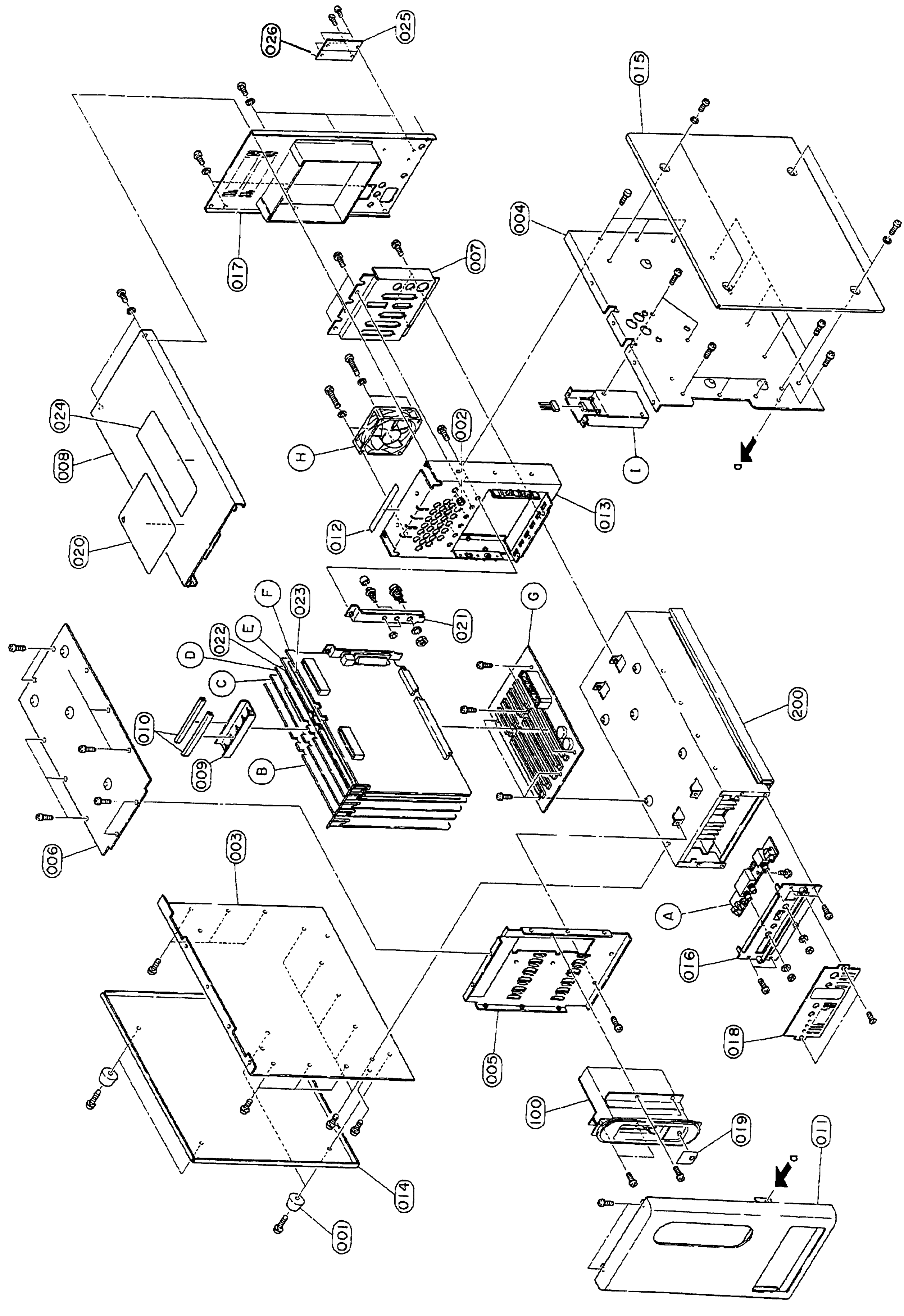
ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UR-31551		079594A	1	CN	HR16-18R-10S(05) blue

Section 10 MECHANICAL PARTS LIST

10-1 Main Unit 10.C2
10-2 Power Transformer Unit 10.4
10-3 Display Unit 10.6
10-4 Power Supply Unit 10.8
10-5 Keypad 10.10
10-6 Head Amplifiers 10.12
  10-6-1 ECG/Respiration Head Amplifier, AC-800P 10.12
  10-6-2 Blood Pressure Head Amplifier, AP-800PA 10.14
  10-6-3 Cardiac Output Head Amplifier, AH-800PA 10.16
  10-6-4 Temperature Head Amplifier, AW-800PA 10.18
  10-6-5 Respiration Head Amplifier, AR-800PA 10.20
  10-6-6 SpO_2 Head Amplifier, AL-800PA 10.22
  10-6-7 EEG Head Amplifier, AE-800PA 10.24
  10-6-8 CO_2 Head Amplifier, AG-800PA 10.26
  10-6-9 CO_2 Sensor, TG-706P 10.28
  10-6-10 O_2 Head Amplifier, AG-820PA 10.30
  10-6-11 Blank Module, EK-800P 10.32
  10-6-12 NIBP Head Amplifier, AP-860PA 10.34
10-7 Transmitter 10.38
  10-7-1 ZB-810PK/ZB-820PK/ZB-821PK 10.38

10-1 Main Unit

No.	Code No.	Description	
001	111345	Rubber foot	ゴム足 K-30(ワツシャ入り)
002	297839	Grommet bush.G84	グロメツトゴムブツシュ G84
003	1112-021275B	Left side chassis	サイド シャーシ(L)
004	1112-021284B	Right side chassis	サイド シャーシ(R)
005	1112-021604B	Front chassis	フロント シャーシ
006	1113-063798A	Shield board	シールド板
007	1113-064128D	Rear holder	リア ホルダ
008	1113-064137B	Top cover	トツプ カバ
009	1114-234139	Circuit board holder	P板 押え
010	1114-234166	U-type rubber	Uガタ ゴム
011	1123-020736B	Front frame (6)	フロントフレーム
012	1124-052165A	Color display nameplate	カラー表示銘板
013	1143-008178B	Rear chassis ASSY	リア シャーシASSY
014	6113-002199A	Left side cover	サイド カバ(L)
015	6113-002207A	Right side cover	サイド カバ(R)
016	1114-234148A	Jack holder	ジャック ホルダ
017	1122-007976B	Rear panel	リア パネル
	6122-000879	Rear panel A	リア パネル A
018	6123-001653A	Front panel A	フロント パネル A
020	6123-001751	BSM warning panel	BSM注意パネル
021	6114-006522	Antenna connector holder	コネクタ ホルダ(ANT)
022	1113-064155A	CRTC shield cover.2	CRTCシールド カバ.2
023	1113-064173A	CRTC shield cover.1	CRTCシールド カバ.1
25	1124-036441	BSM System nameplate	BSM システム銘板
26	1124-036432	BSM Main Unit nameplate	BSM 本体銘板
100	UP-0799	MEMORY CARD Board	
200	SC-018R	Power Transformer Unit	
A	UP-0807	CONNECTOR Board	コネクタ ボード
B	UP-0670	DPU Board	DPU ボード
C	UP-0563	COM3 Board	COM3 ボード
D	UR-3027	CPU Board	CPU ボード
E	UP-0795	CRTC Board	CRTC ボード
F	UP-0797	I/O Board	I/O ボード
G	UP-0798	MOTHER Board	マザー ボード
H	367737	Fan, ASF-84371	ファン,ASF-84371
I	ZR-800P	Receiver Unit	レシーバーユニット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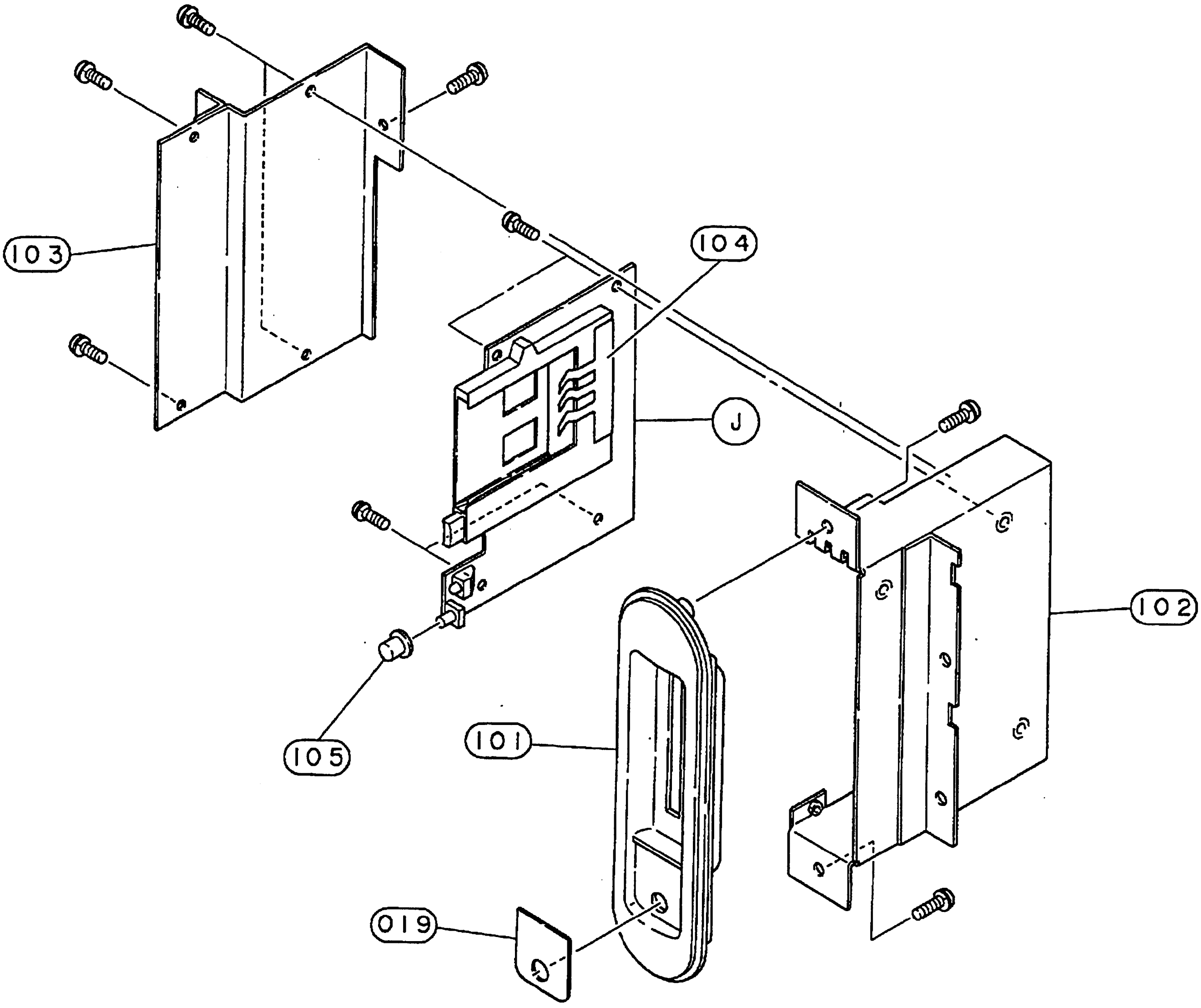
10. MECHANICAL PARTS LIST

No.	Code No.	Description	
019	6124-004051A	MC panel A	MCパネルA
101	1112-021622C	MC front panel	MCフロントパネル
102	1113-064164C	MC shield case.2	MCシールドケース.2
103	1114-234184C	MC shield case.1	MCシールドケース.1
104	6114-002161	MC shield spring	MCシールドバネ
105	6114-002179	Memory SW key top	メモリーSWキートップ
J	UP-0799	MEMORY CARD Board	メモリカードボード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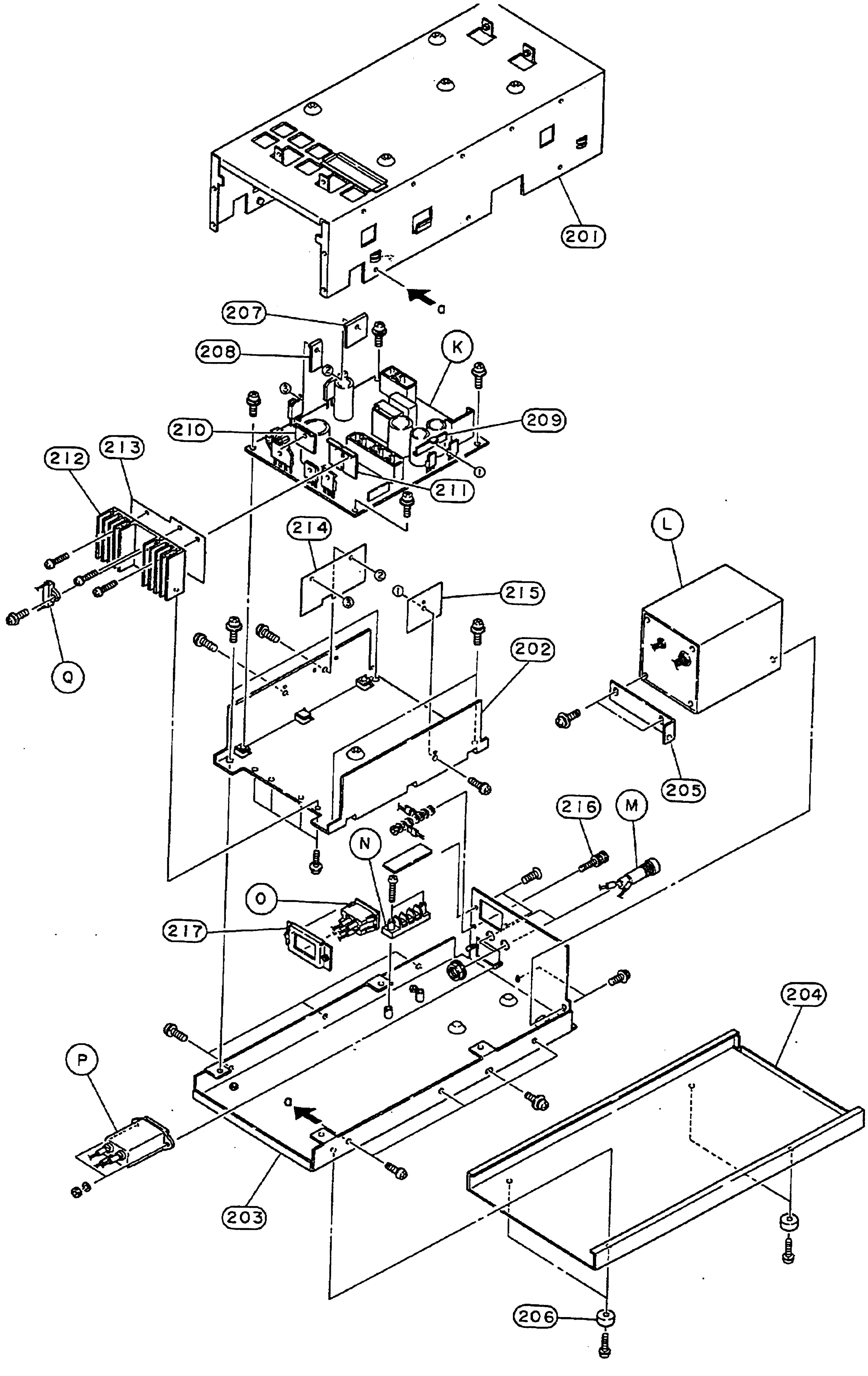
10-2 Power Transformer Unit

No.	Code No.	Description	
201	1112-021266A	Internal chassis	内部シャーシ
202	1113-063789A	Chassis.2	電源シャーシ.2
203	113-063771A	Chassis.1	電源シャーシ.1
204	6113-002956	Bottom cover	ボトム カバ
205	1114-233434A	Transformer holder	トランス ホ·ルダ
206	367835	Flat type rubber foot CK-17	平型ゴム足 CK-17
207	6114-000395	D fixing plate	D 取付け板
208	6114-000484	TR fixing plate (2)	TR 取付け板 (2)
209	1114-151175	Transistor fixing plate 2A	トランジスタ固定金具 2A
210	6114-000395	D fixing plate	D 取付け板
211	6114-000475	TR fixing plate (1)	TR 取付け板 (1)
212	6114-000038	Radiator	放熱器
213	6114-000493	Radiation sheet.1	放熱シート.1
214	6114-000564	Radiation sheet.2	放熱シート.2
215	6114-000617	Radiation sheet.3	放熱シート.3
216	1144-010734A	Equipotential terminal ASSY	アースターミナル ASSY
217	1114-234157A	Switch holder	スイッチ ホ·ルダ
K	UP-0813	Regulator Board	レギュレータユニット ボード
L	365828 365837	Power Transformer for SC-018RJ Power Transformer for SC-018RK	トランス
M	104825	Fuse holder	ヒューズ ホルダFEU031-1681
N	103131	Power terminal	端子台 ULC-505-3P-C
O	370368	Power switch	電源 スイッチ, JW-M22-RKK
P	024252	AC inlet	AC インレット, SUP-E3G-E2
Q	325854	Thermal switch	サーマルスイッチ,OHD3-90MU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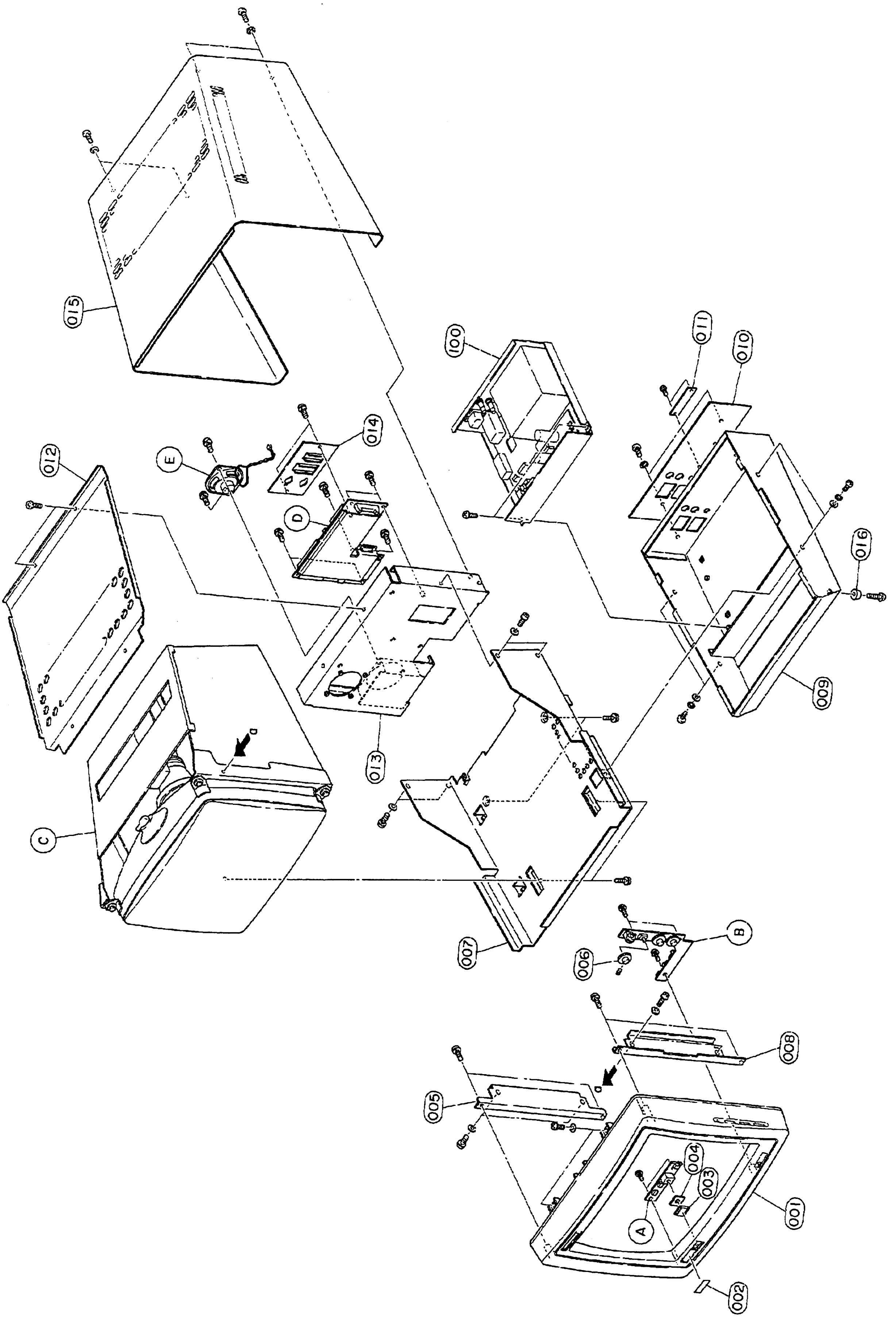
10-3 Display Unit

No.	Code No.	Description	
001	6142-000191A	Front panel ASSY	フロント パネル ASSY
002	6124-004006	LED panel A	LED パネル.A
003	6114-007111A	Filter	フィルタ
004	6114-007352A	Fixed sponge	固定 スポンジ
005	6113-002457B	CRT unit fixing plate	CRT 取付け金具
006	6114-005559	VR knob	VR ツマミ
007	6112-001103B	Bottom chassis	ボトム シャーシ
008	6113-002457B	CRT unit fixing plate	CRT 取付け金具
009	6112-001095A	Bottom cover	ボトム カバ
010	6123-001395	Power supply panel	電源 パネル
011	1124-024632	Display unit nameplate	本体銘板
012	6113-002448	Reinforcement plate	補強板
013	6112-001121	Rear chassis	リヤ シャーシ
014	6124-003239	Connector panel	コネクタ パネル
015	6112-001112A	Display unit cover	カバ
016	111345	Rubber foot with washer	ゴム足 K-30(ワッシャイリ)
100	SC-019R	Power Supply Unit	
A	UP-0806	LED Board	
B	UP-0802	OPERATION (VR) Board	
C	410325	CRT unit, QA1465	
D	UP-0801	OPERATION CONTROL Board	
E	073662	Speaker EAS-65P34S 160Ω	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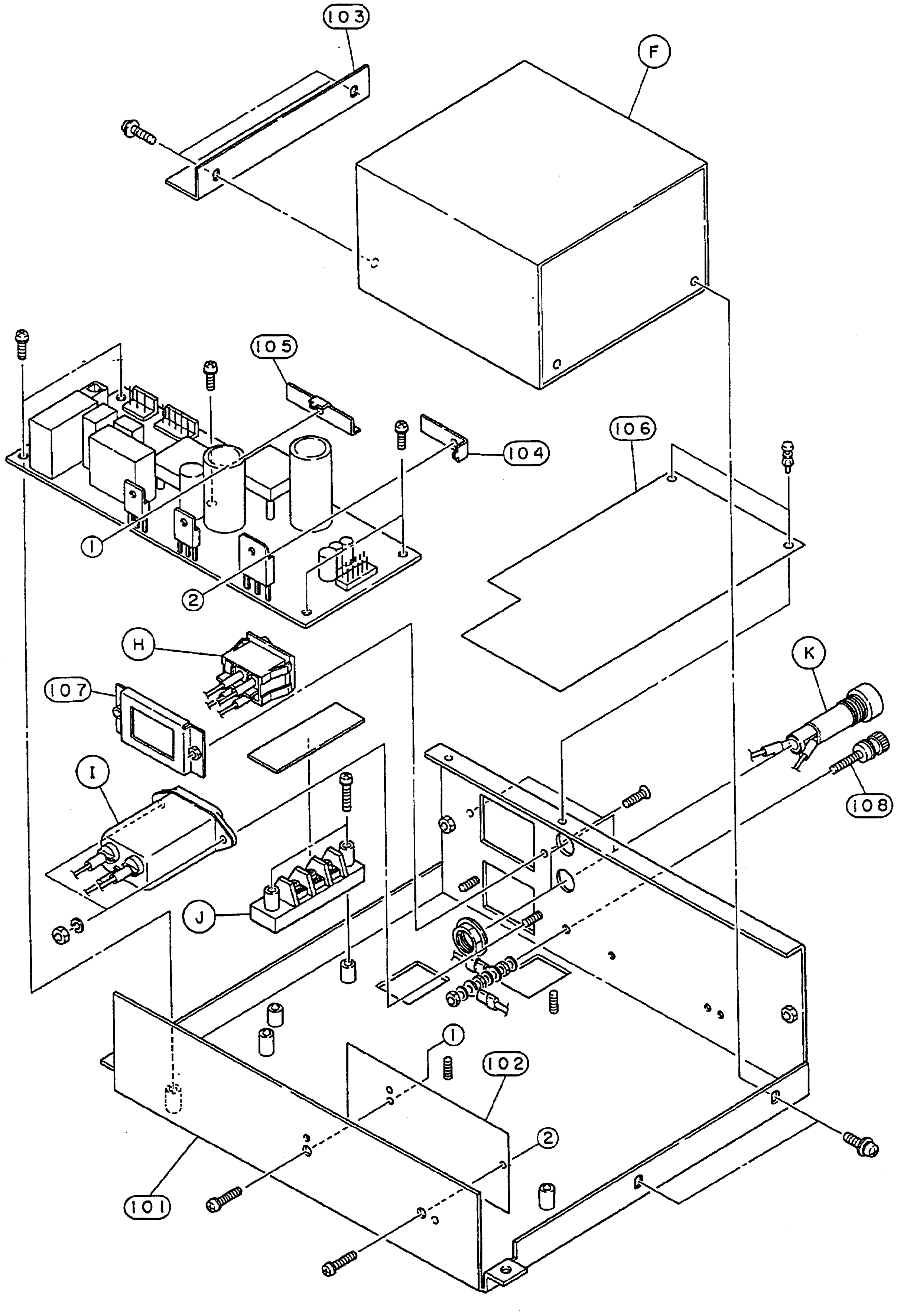
10-4 Power Supply Unit

No.	Code No.	Description	
101	6112-000541	Chassis	シャーシ
102	6114-002562	Heat insulation sheet	放熱シート
103	6114-002312	Transformer fixing plate	トランス金具
104	6114-002116	TR fixing plate	TR取付け板
105	1114-151175	Transistor fixing plate.2A	トランジスタ固定金具.2A
106	6114-003196	Insulation sheet	絶縁 シート
107	1114-234157A	Switch holder	スイッチ ホルダ
108	1114-010734A	Equipotential terminal ASSY	アースタミナル ASSY
F	365864	Power Transformer for SC-019RJ	トランス
	365873	Power Transformer for SC-019RK	
H	370368	Power switch	JW-M22RKK
I	024252	Line filter	ラインフィルタ SUP-E3G-E-2
J	103131	Power terminal	端子台コウワ ULC-505-3P-C
K	104825	Fuse holder	ヒューズホルダ FEU031 1681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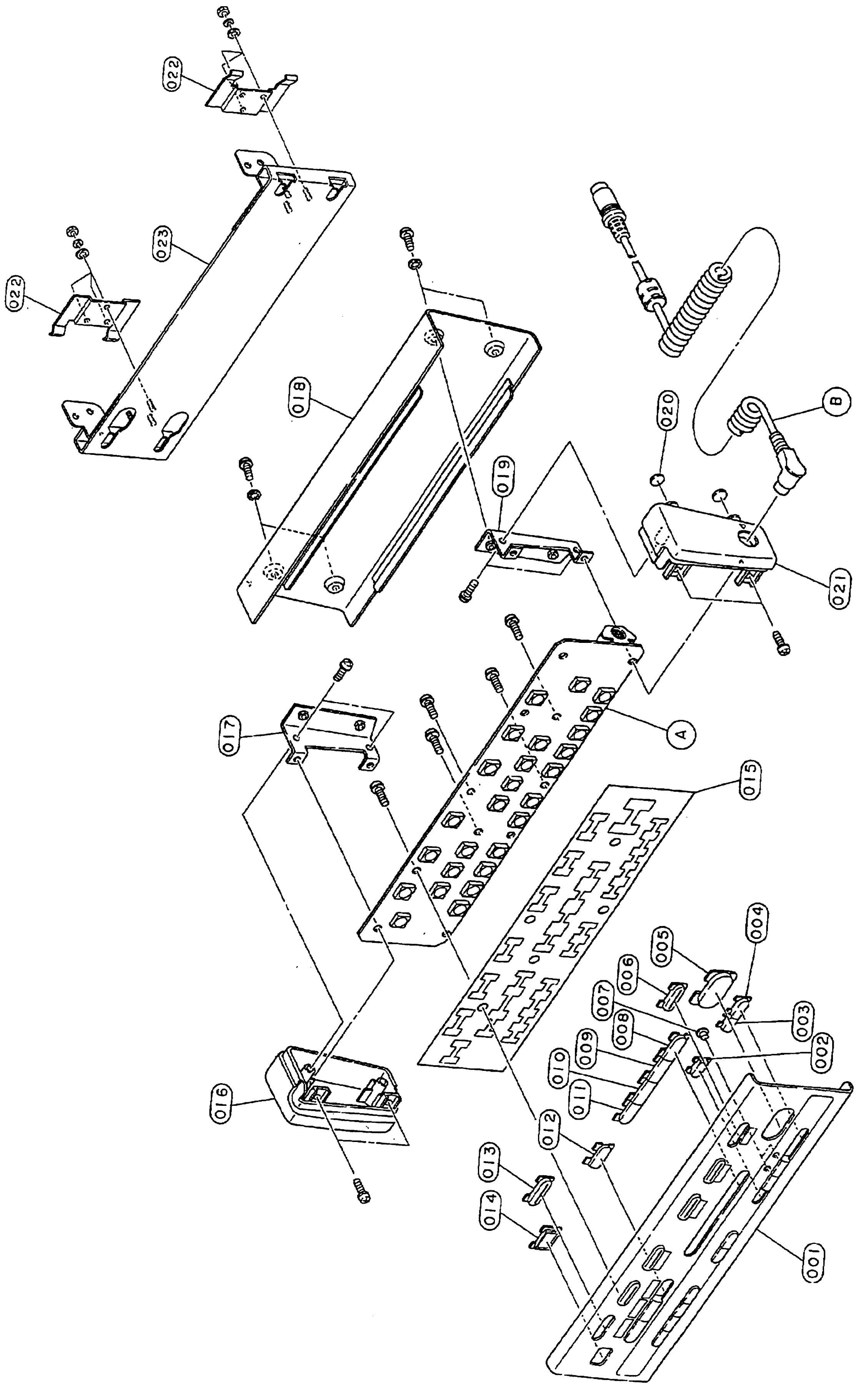
10-5 Keypad

No.	Code No.	Description	
001	6122-000389A	Operation panel	操作部 本体シルク図
002	6114-003124B	Key top 4	キートップ 4
003	2114-081268	Key top 5×15 (L.Gray)	キートップ5×15(ライトグレー)
004	6114-003124B	Key top 4	キートップ 4
005	6124-002276	Key top 2	キートップ 2 シルク図
006	6124-003702A	Key top 6A.2	キートップ 6Aシルク図.2
007	6114-003151	LED spacer	LED スペーサ
008	6124-002267B	Key top 3	キートップ 3 シルク図
009	6114-006879	Key top 8×20 (XL.Gray)	キートップ8×20(エキストライトグレー)
010	6124-002294A	Key top 5	キートップ 5シルク図
011	6114-003098B	Key top 3	キートップ 3
012		Instruction label (6-2A)	取り説パネル。(6-2A)
013	6124-003694A	Key top 6A.1	キートップ 6Aシルク図.1
014	6124-002285A	Key top 1	キートップ 1 シルク図
015	6112-000461B	Key top positioning sheet	位置決めシート
016	6112-000514C	Left side cover	サイド カバ (左)
017	6113-001101D	Operation board holder.2	操作部固定板.2
018	6112-000523B	Keypad bottom frame	操作部ソコイタ
019	6113-001093C	Operation board holder.1	操作部固定板.1
020	6114-008805	Rubber foot	ゴムパット
021	6112-000505C	Right side cover	サイド カバ (右)
022	6114-009377	Click spring	クリックバネ
023	6112-000488B	Keypad holder	操作部結合金具
A	UR-3025	OPERATION RY Board	
B	359996	Keypad connecting cable	キーパット接続ケーブル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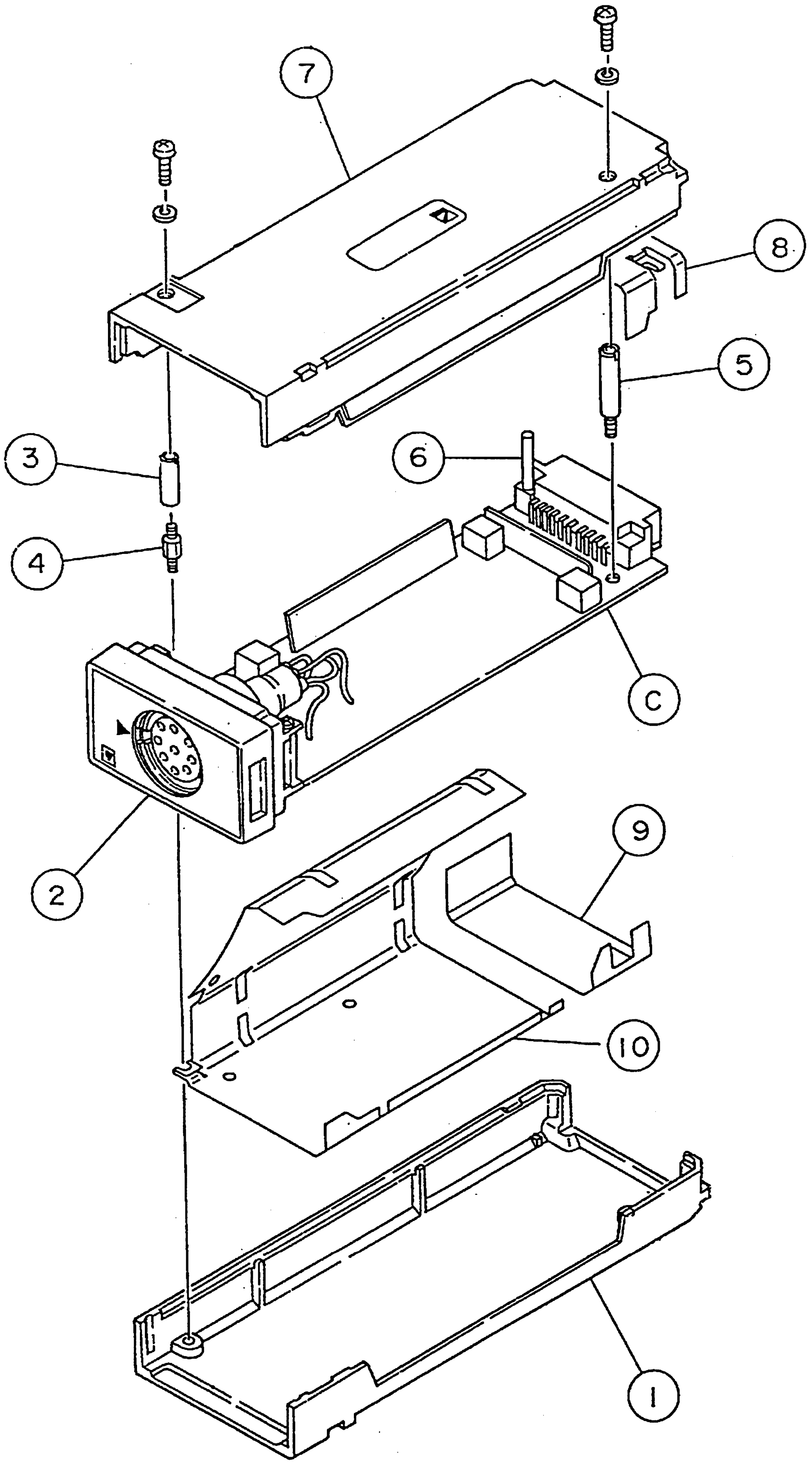
10-6 Head Amplifiers

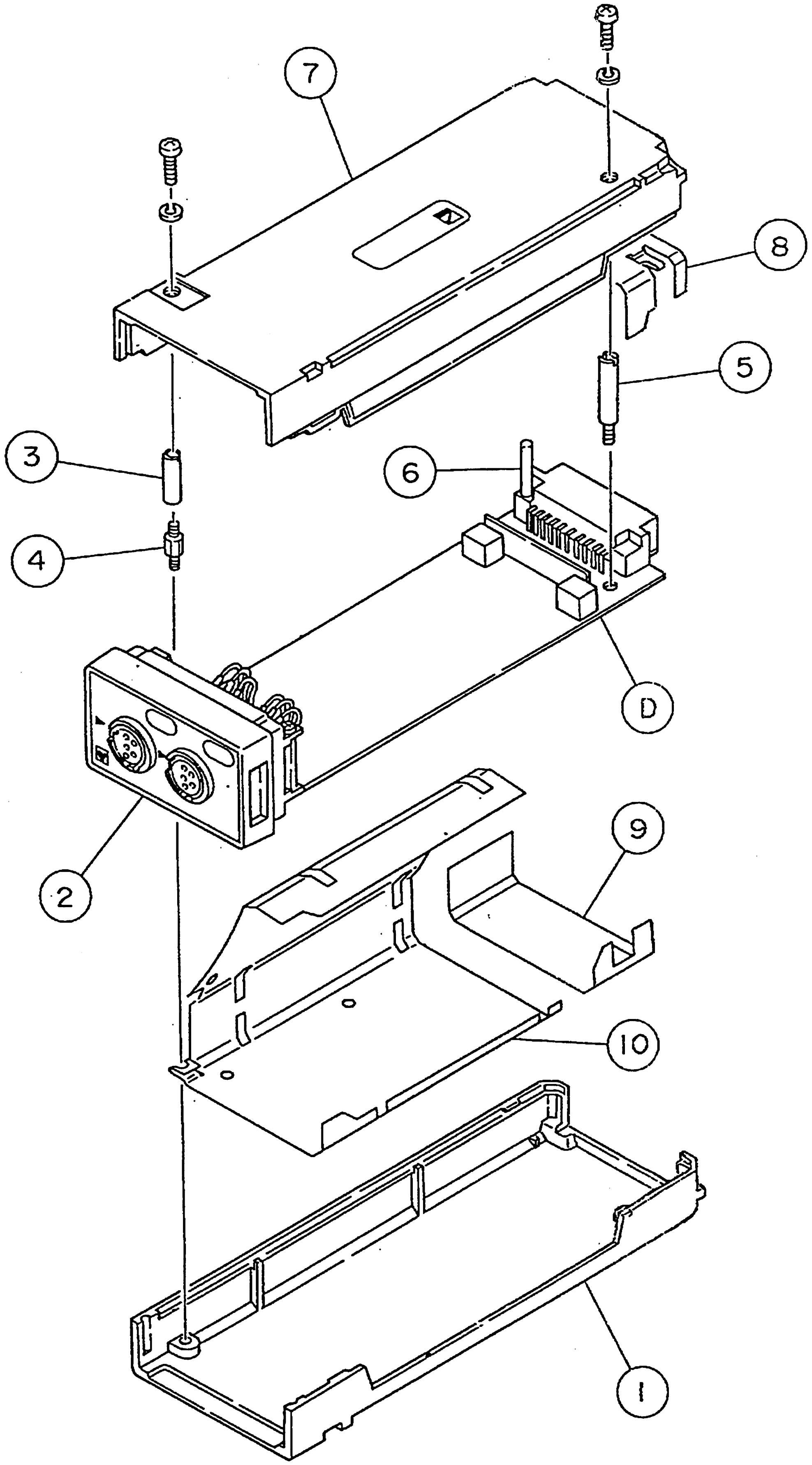
10-6-1 ECG/Respiration Head Amplifier, AC-800P

Index	Code No.	Description	
1	1112-013569	Head amp housing (right)	アンプユニットケース(右)
2	1112-013542A	ECG Input connector case	ECG アンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱2
4	1114-190052	PCB Support-1	P板支柱1
5	1114-169397	PCB Support	
6	1114-177281	Spacer	反り防止スペーサ
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
8	1114-171055B	Shielding cover DDG	
9	1114-179448B	Shielding cover DMG	
10	1113-049831A	Shielding cover F	
C	UP-0272	ECG Head Amp board	


C

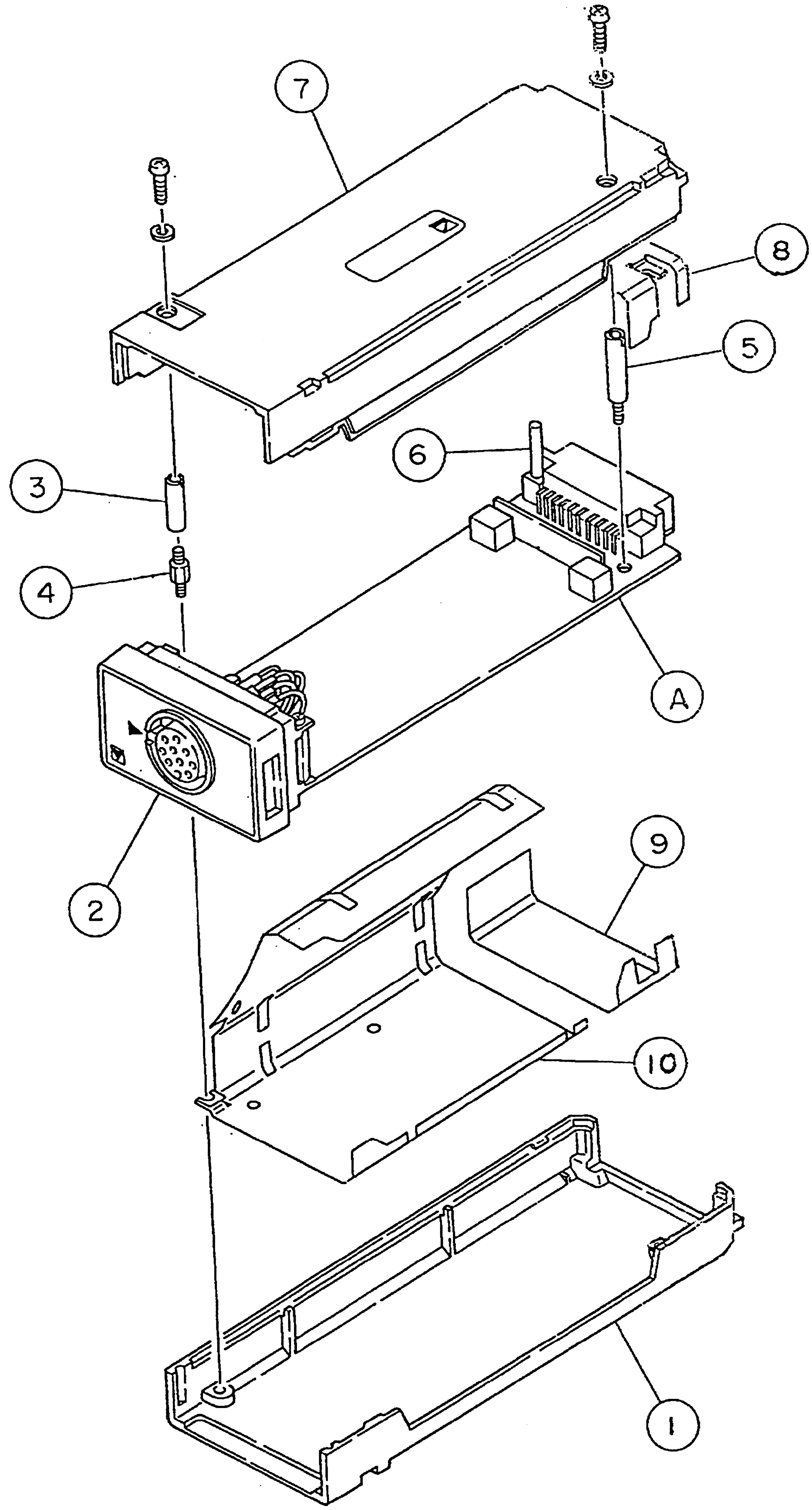
10-6-2 Blood Pressure Head Amplifier, AP-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-014238A	BP Input connector case	5Px2 アンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-169397	PCB Support	
6	1114-177281	Spacer	反り防止スペーサ
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
8	1114-171055B	Shielding cover DDG	
9	1114-179448B	Shielding cover DMG	
10	1113-049831A	Shielding cover F	
D	UP-0369	Blood Pressure Head Amp board	


D

10-6-3 Cardiac Output Head Amplifier, AH-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニトケース(右)
2	1112-014211A	CO Input connector case	10P, 15P アンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-169397	PCB Support	
6	1114-177281	Spacer	反り防止スペーサ
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
8	1114-171055B	Shielding cover DDG	
9	1114-179448B	Shielding cover DMG	
10	1113-049831A	Shielding cover F	
A	UP-0318	Cardiac Output Head Amp board	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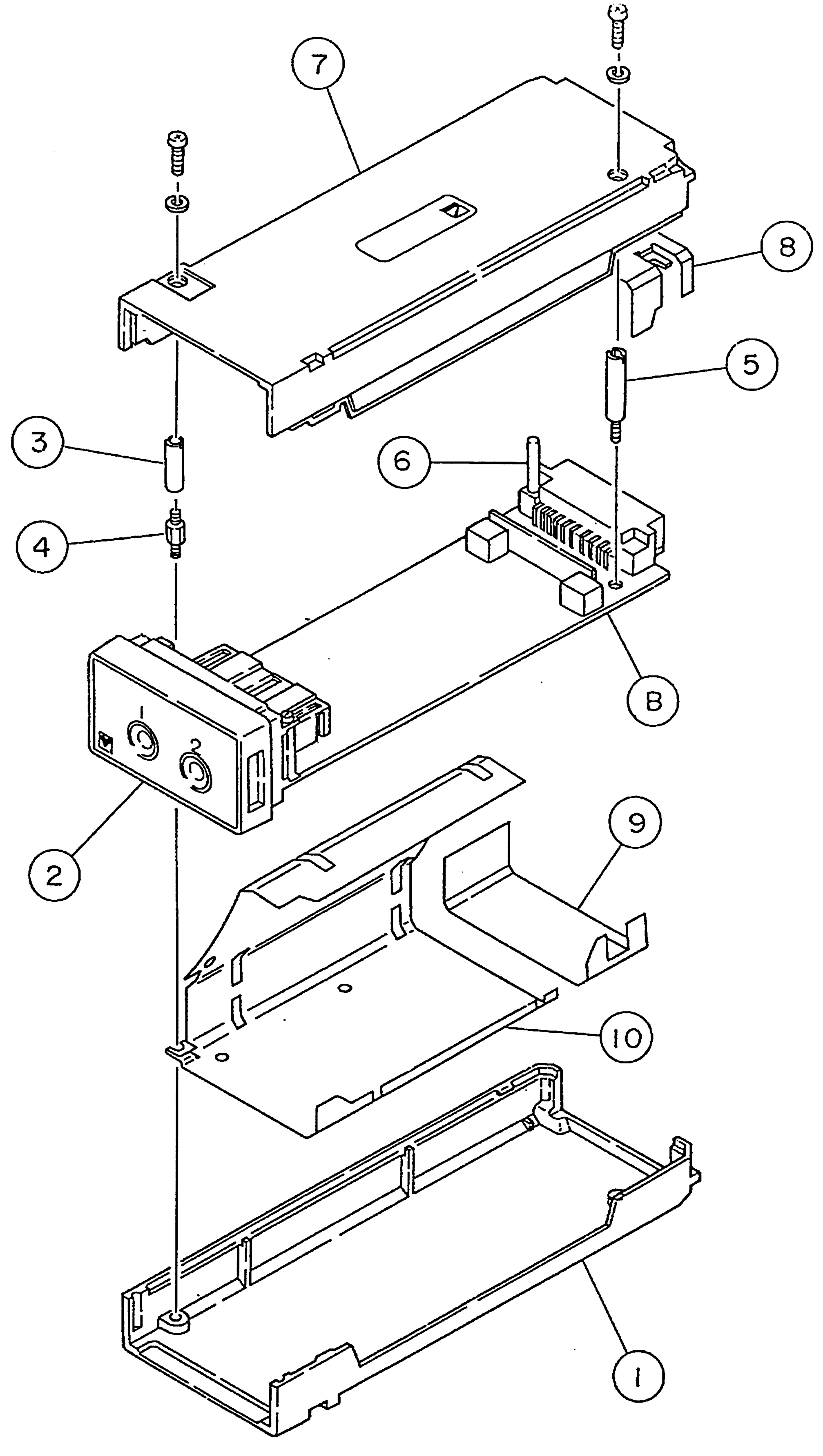
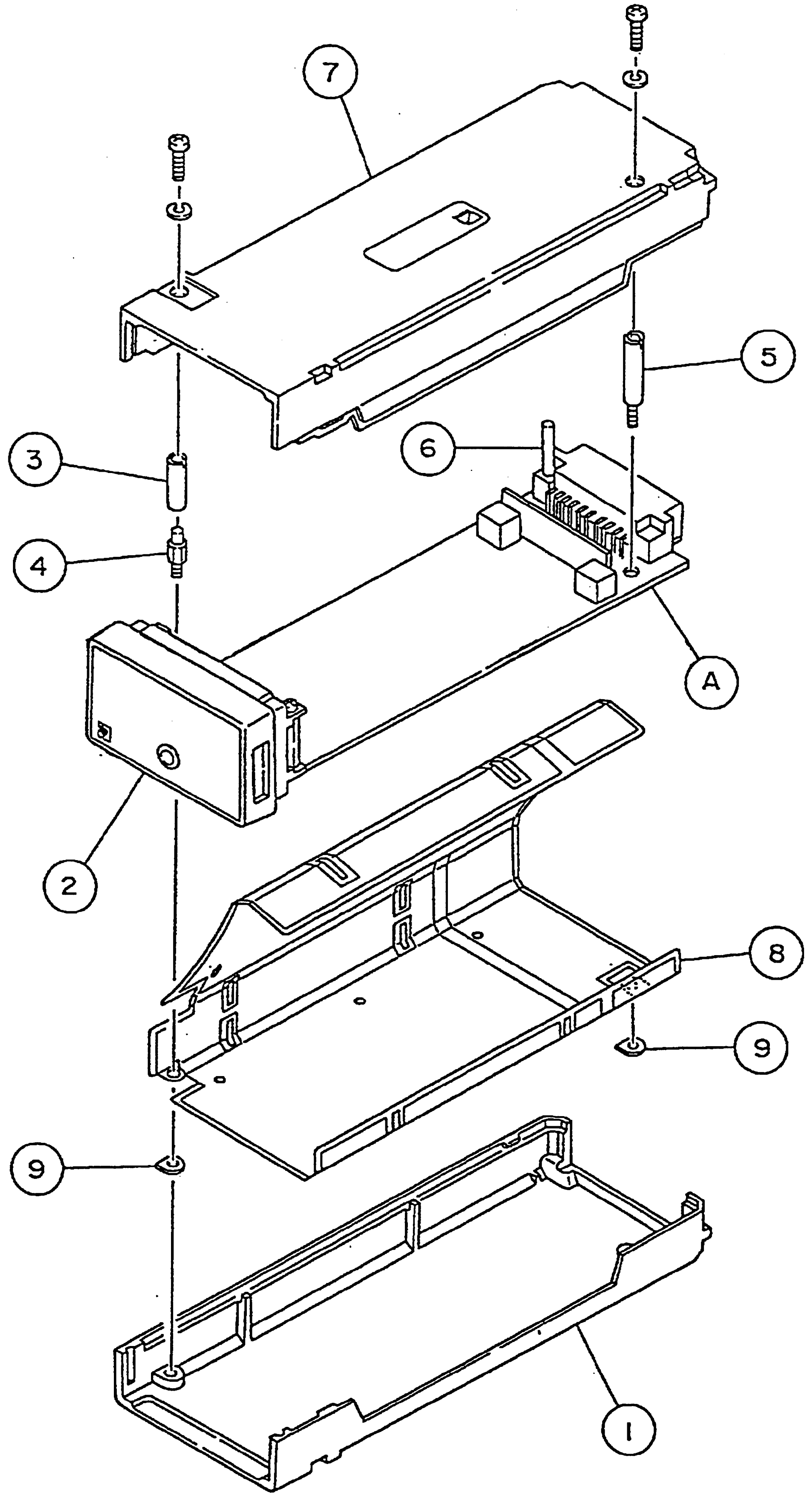
10-6-4 Temperature Head Amplifier, AW-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-013587	TEMP Input connector case	TEMP アンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱 2
4	1114-190052	PCB Support-1	P板支柱 1
5	1114-169397	PCB Support	
6	1114-177281	Spacer	反り防止スペーサ
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
8	1114-171055B	Shielding cover DDG	
9	1114-179448B	Shielding cover DMG	
10	1113-049831A	Shielding cover F	
B	UP-0319	Temp Head Amp board	


B

10-6-5 Respiration Head Amplifier, AR-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-014211A	10P, 15P amp main unit	10P, 15P アンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-169397	PCB Support	
6	1114-177281	Spacer	反り防止スペーサ
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
8	1113-047299	Laminated shielding plate	ラミネート シールド板
9	1114-205946	Spacer	スペーサ
10	1124-038778B	AR-800PA front panel	AR-800PA 表パネル
A	UP-0548	Respiration Head Amp board	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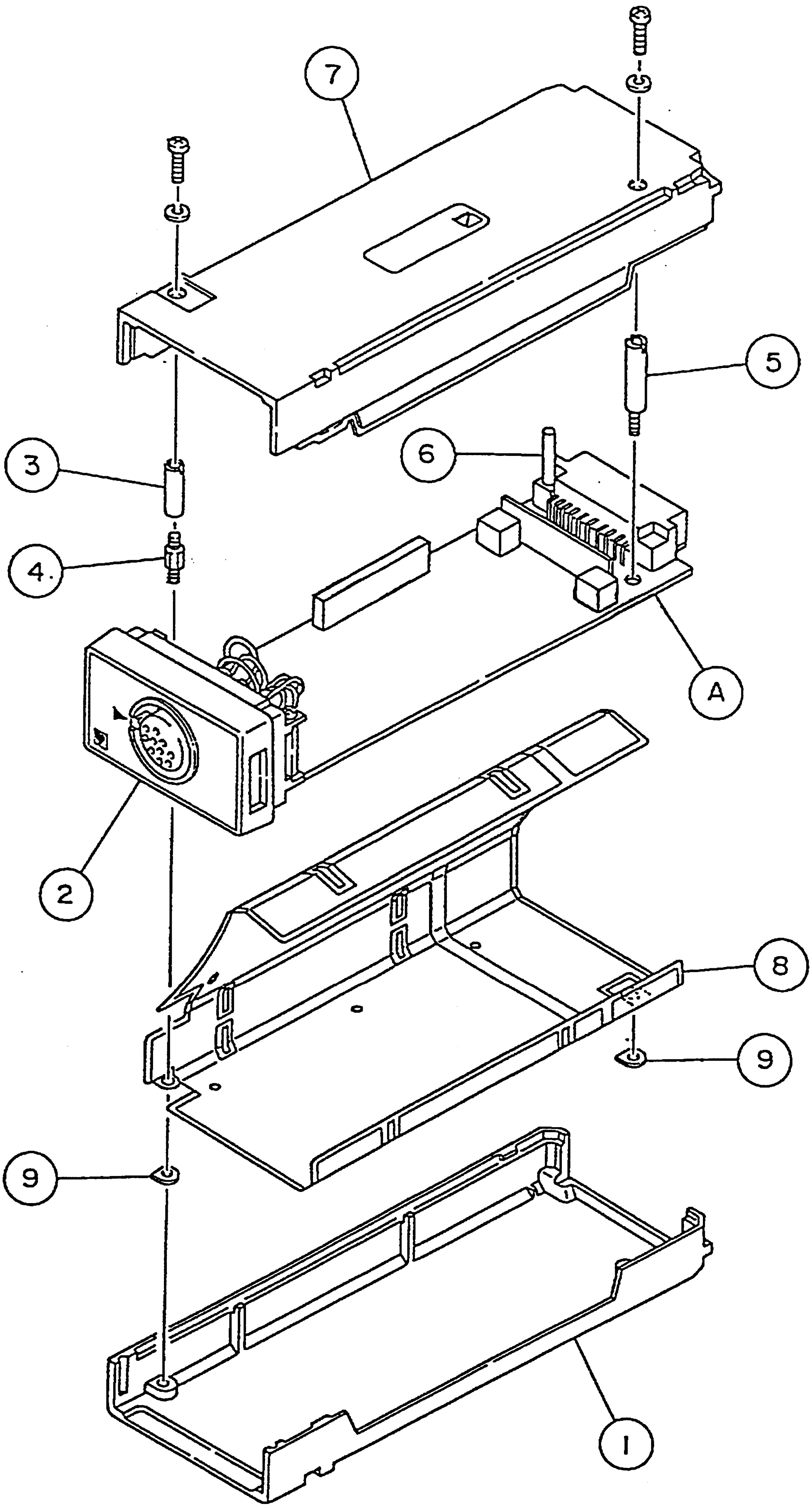
10-6-6 SpO$_2$ Head Amplifier, AL-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-014211A	10P, 15P amp main unit	10P,15Pアンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-169397	PCB Support	
6	1114-199738	Spacer	反り防止 スペーサ.B
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
8	1113-047299	Laminated shielding plate	ラミネートシールド板
9	1114-205946	Spacer	スペーサ
10	1124-038537A	AL-800PA front panel	AL-800PA 表パネル
A	UP-0551	SpO$_2$ Main board	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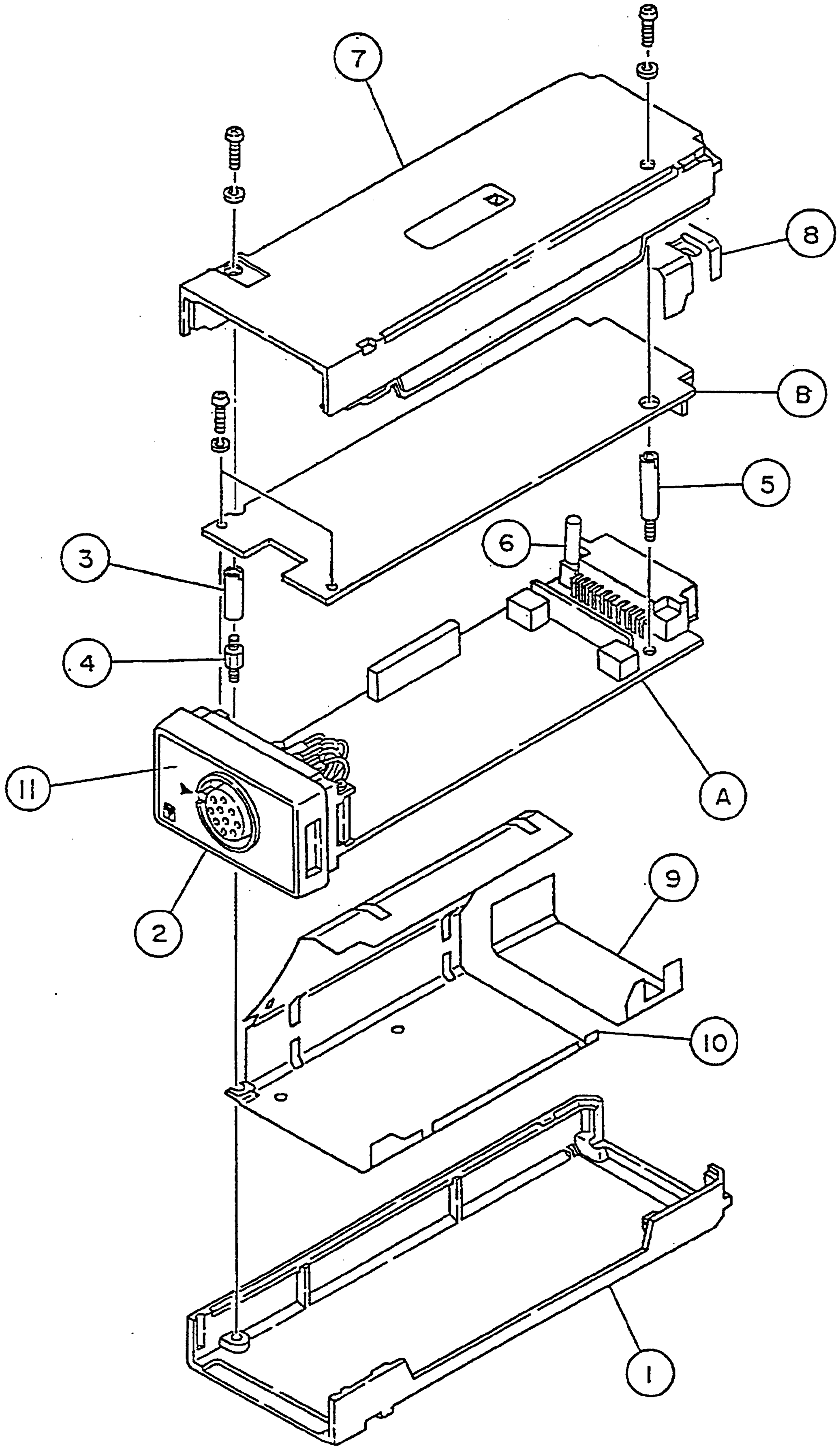
10-6-7 EEG Head Amplifier, AE-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-014211A	EEG input connector case	10P, 15P アンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-169397	PCB Support	
6	1114-199738	Spacer	反り防止スペーサ.B
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左))
8	1114-171055B	Shielding cover DDG	
9	1114-179448B	Shielding cover DMG	
10	1113-049831A	Shielding cover F	
11	1124-033132A	AE-800PA front panel	AE-800PA表パネル
A	UP-0421	EEG main board	
B	UP-0422	EEG sub board	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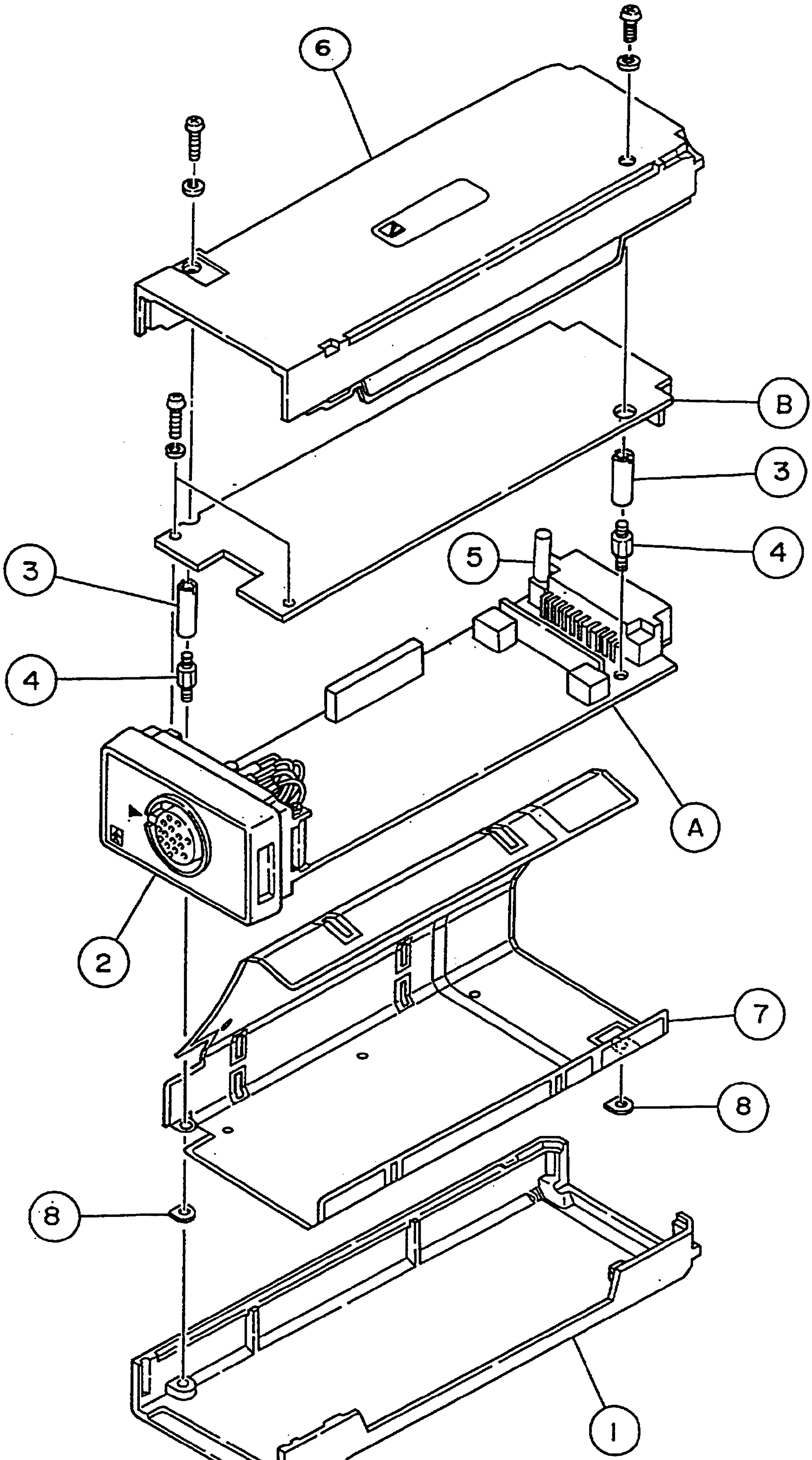
10-6-8 CO_2 Head Amplifier, AG-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-014211A 1124-038796A	Amp. unit front frame (10P, 14P) AG-800PA front panel	10P,15P アンプユニット本体 AG-800PA 表パネル
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-199738	Spacer	反り防止 スペーサ.B
6	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
7	1113-047299	Laminated shielding plate	ラミネート シールド板
8	1114-205946	Spacer	スペーサ
A	UP-0588	CO_2 main board	
B	UP-0589	CO_2 sub board	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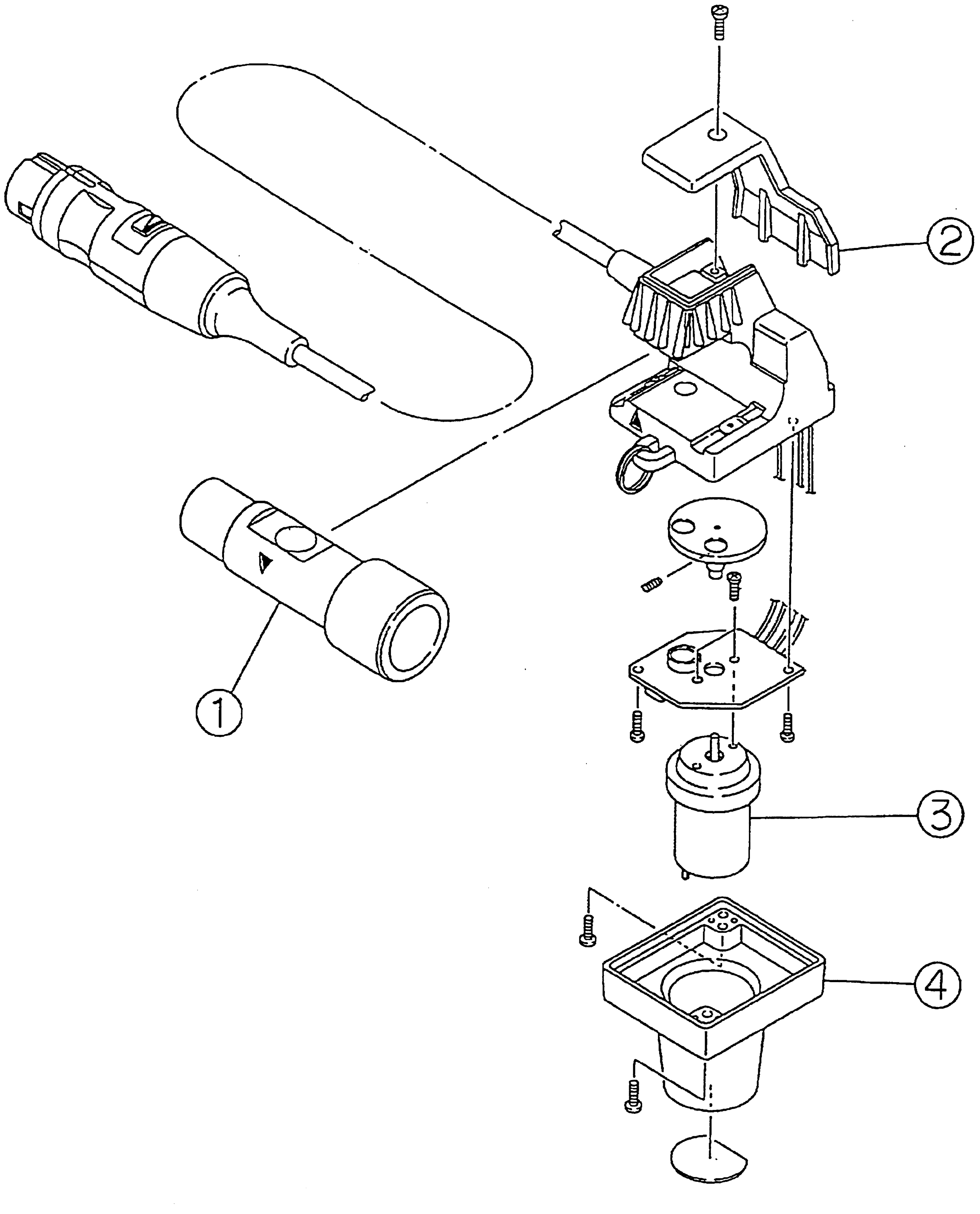
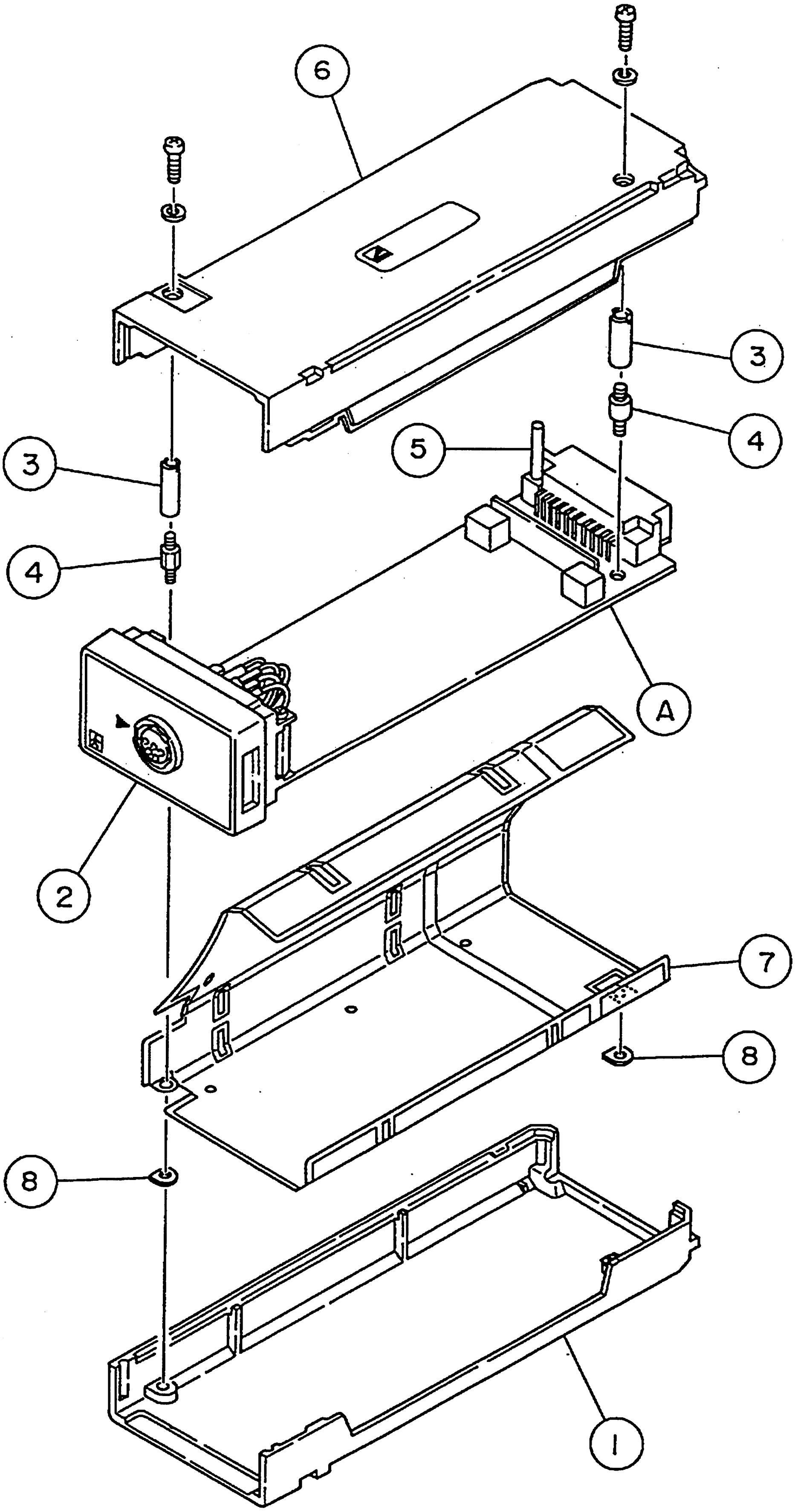
10-6-9 CO_2 Sensor, TG-706P

Index	Code No.	Description
1	YG-706P	CO_2 cell
2	1113-043588C	RG-706P housing TC
3	YS-017P4	RG-706P motor Assy
4	1113-052943	RG-706P housing TA.2



10-6-10 O_2 Head Amplifier, AG-820PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-014238A	Amplifier unit front frame (5P×2)	5Px2 アンプユニット本体
	1124-039206B	AG-820PA front panel	AG-800PA 表パネル
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-177281	Spacer	反り防止スペーサ
6	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
7	1113-047299	Laminated shielding panel	ラミネート シールド板
8	1114-205946	Spacer	スペーサ
A	UP-0592	O_2 Head Amp board	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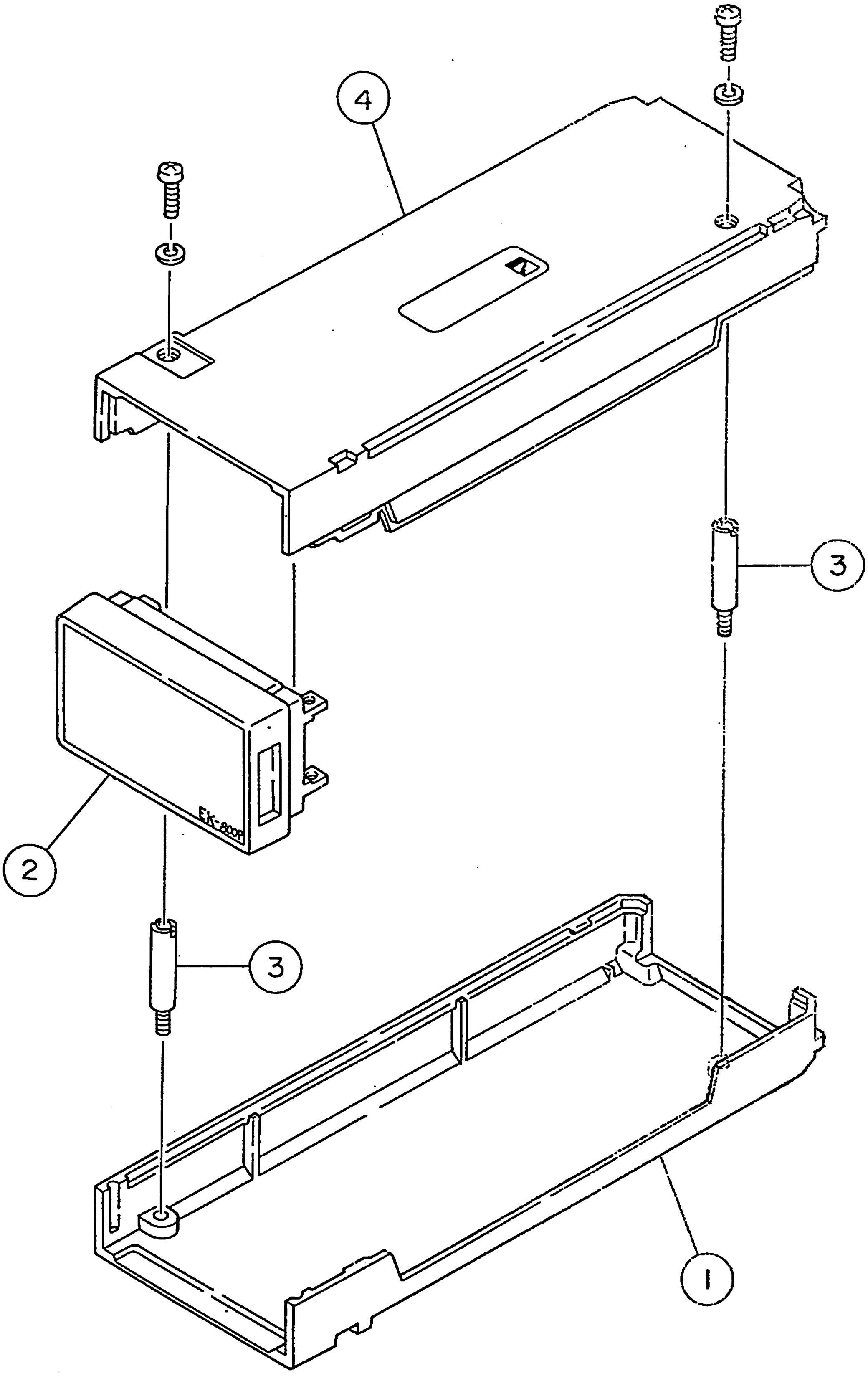
10-6-11 Blank Module, EK-800P

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-013587	TEMP Input connector case	
3	1114-171376	Housing spacer	
4	1112-013533A	Head amp housing (left)	アンプユニットケース(左)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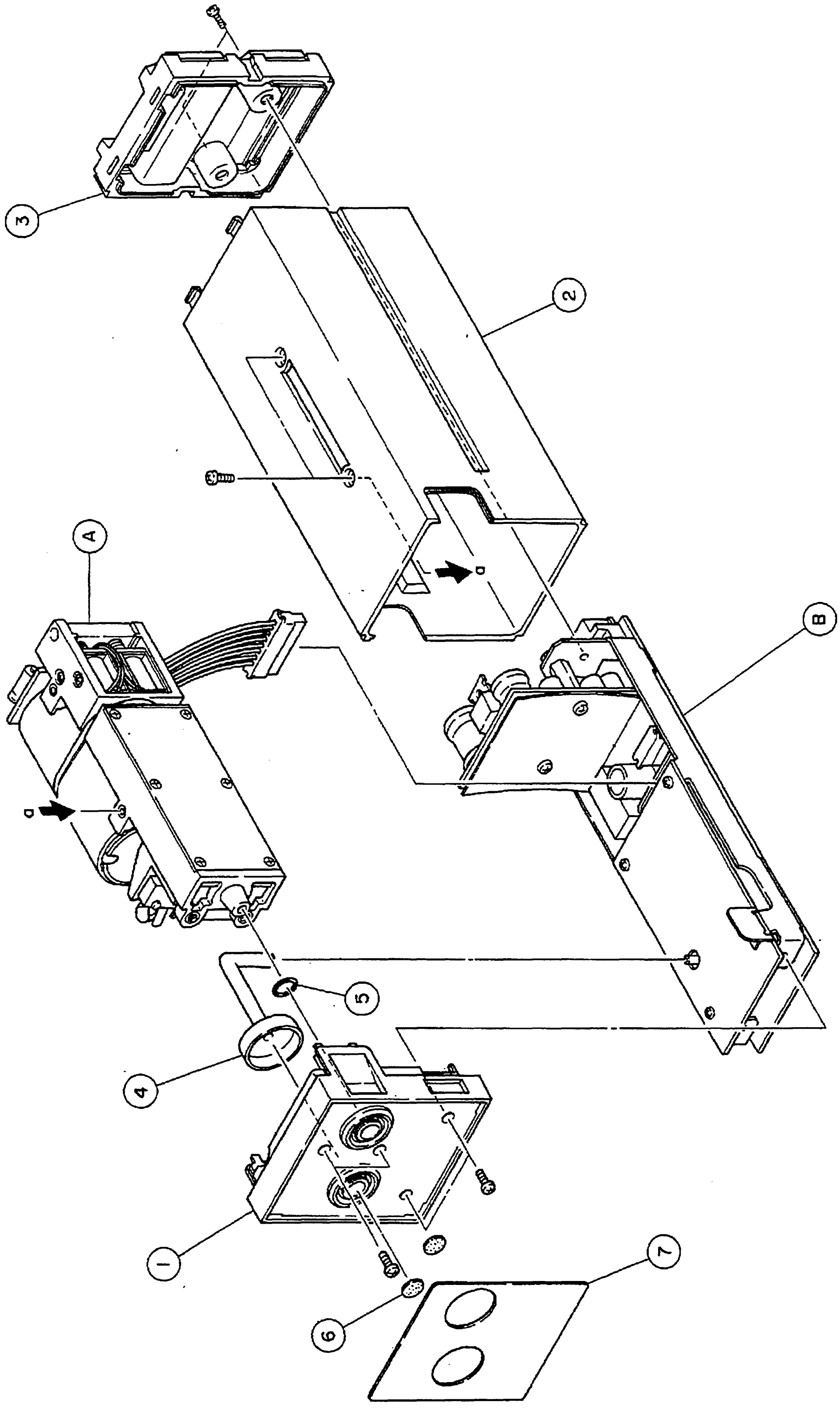
10-6-12 NIBP Head Amplifier, AP-860PA

Index	Code No.	Description	
1	6112-000122A	NIBP main unit	NIBPユニット本体
2	1112-018243B	NIBP case	NIBPケース
3	1112-018297D	NIBP unit cover	NIBPユニットカバ
4	6114-000546	L-shaped tube (sensor)	L形チューブ(センサ)
5	108893	O Ring P-5	Oリング P-5
6	1114-210316	Filter.4	フィルタ.4
7	1124-042229B	Panel for AP-860PA	AP-860PA表パネル
A	SG-001P	AIR unit	空気系ユニット
B		NIBP Head Amplifier's chassis	NIBPユニットアンプシャーシ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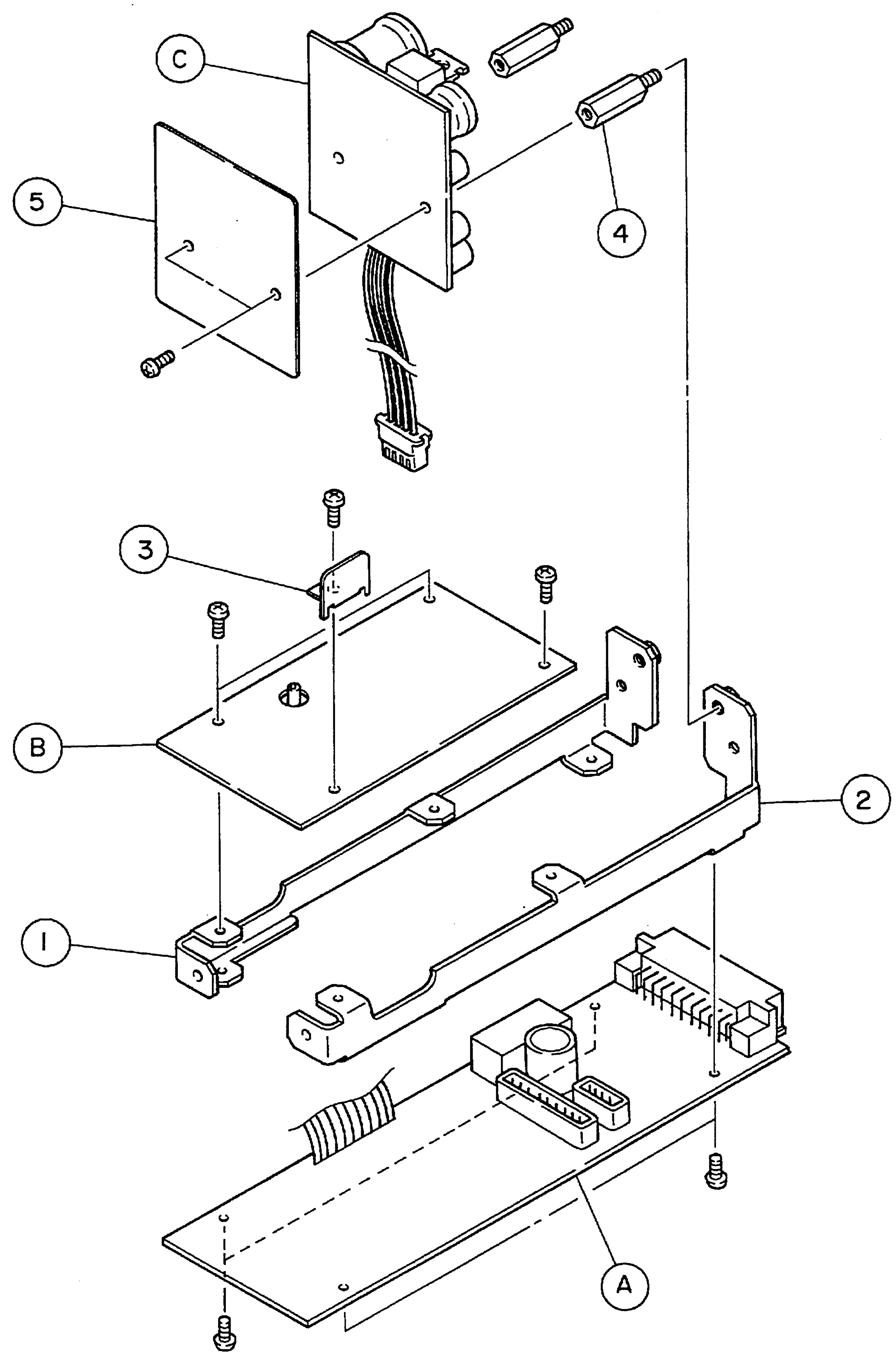
NIBP Head Amplifier's Chassis

Index	Code No.	Description	
1	1114-219896A	PCB board holder.1	P板ホルダ.1
2	1114-219904A	PCB board holder.2	P板ホルダ.2
3	1114-222482	Suspension spring	導通バネ
4	128176	Spacer Bolt (L=14)	間隔ボルド(L=14)
5	1114-221474	Converter Insulation sheet	コンバータ絶縁シート
A	UP-0629	Main board	メイン ボード
B	UP-0630	Sub board	サブ ボード
C	038077	DC/DC Converter	DC/DC コンバータ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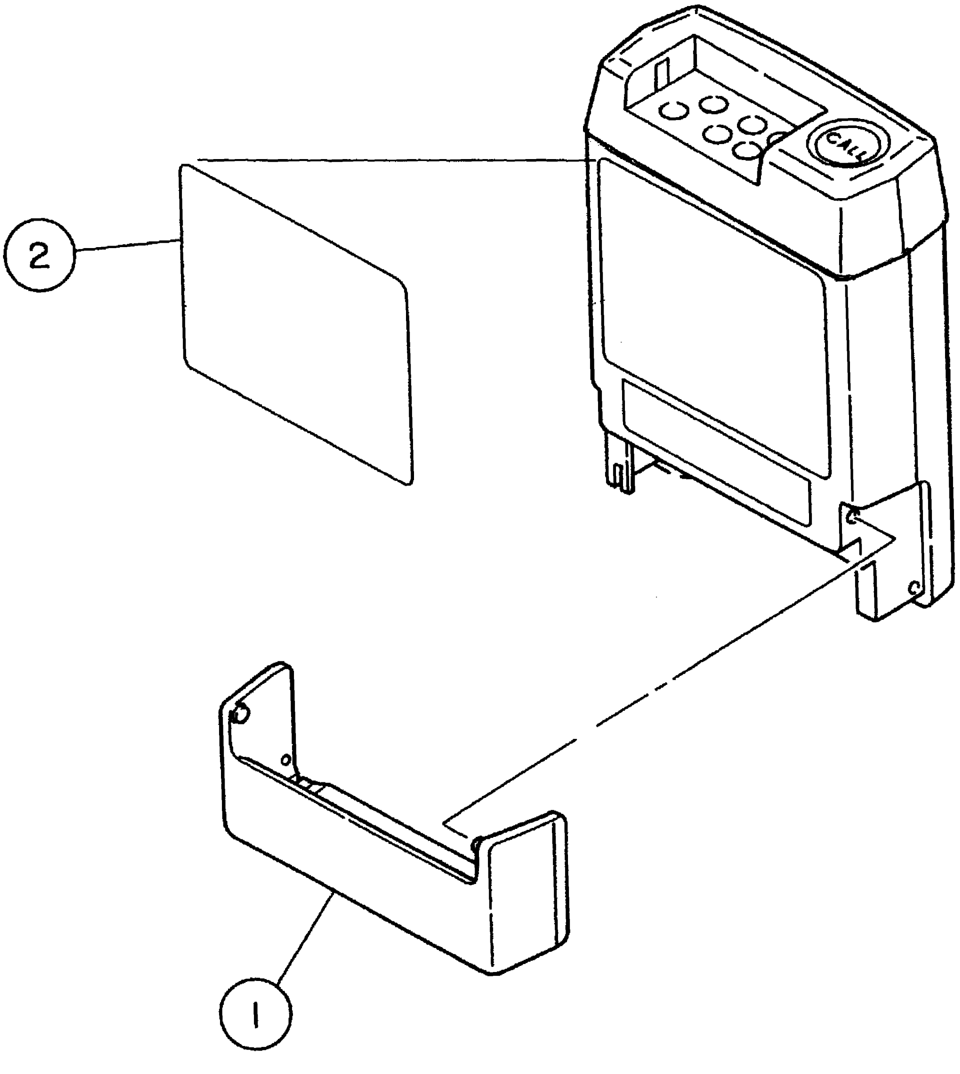
10-7 Transmitter

10-7-1 ZB-810PK/ZB-820PK/ZB-821PK

Index	Code No.	Description	
1	1112-020222	Battery cover	バッテリカバ
2	1124-051585A	ZB-810PK Label	ZB-810PK メイバン
	1124-051834	ZB-820PK Label	ZB-820PK メイバン
	6124-011907	ZB-821PK Label	ZB-821PK メイバン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Section 11 BLOCK DIAGRAM

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11-6 Display Unit, VD-881R

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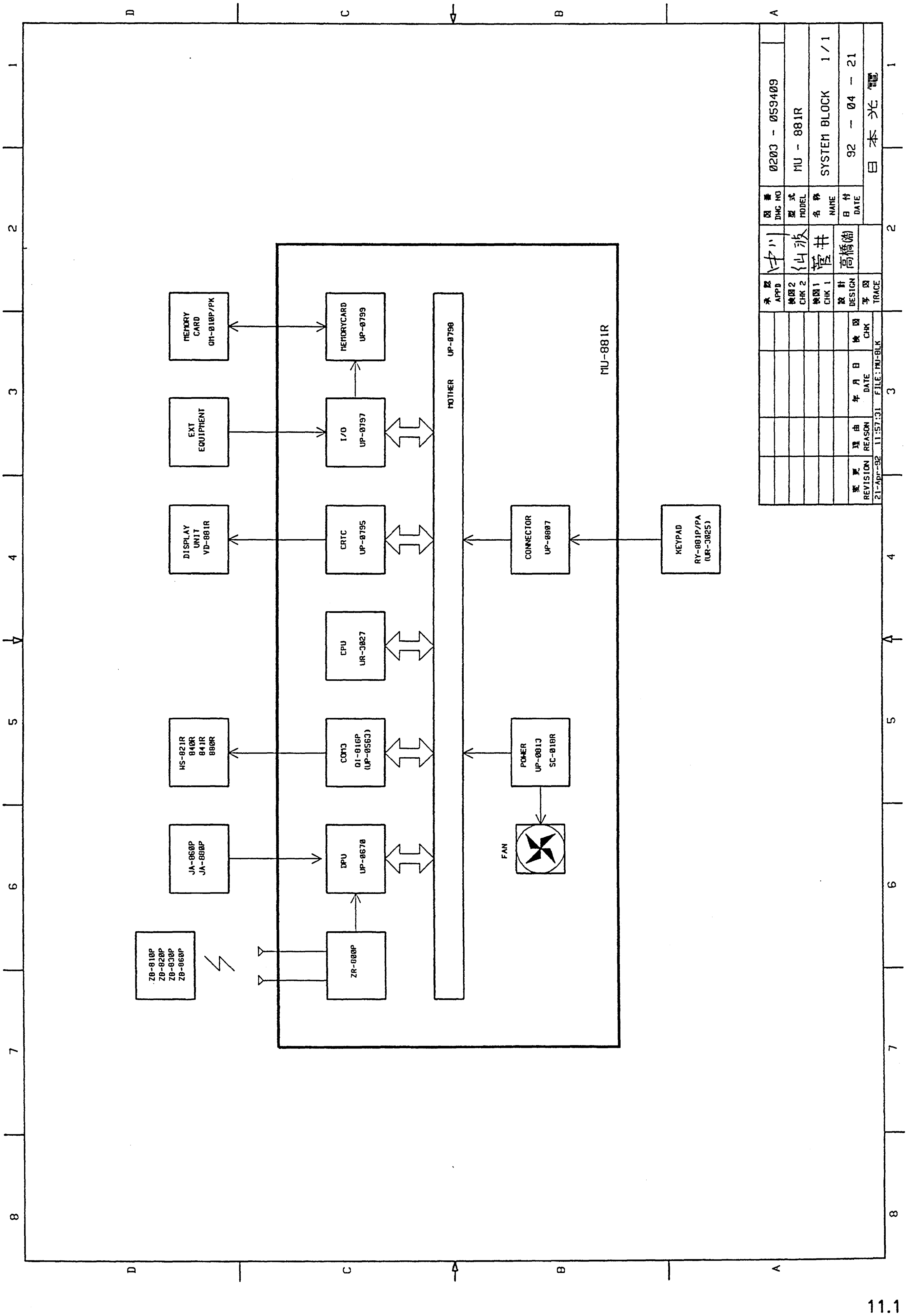
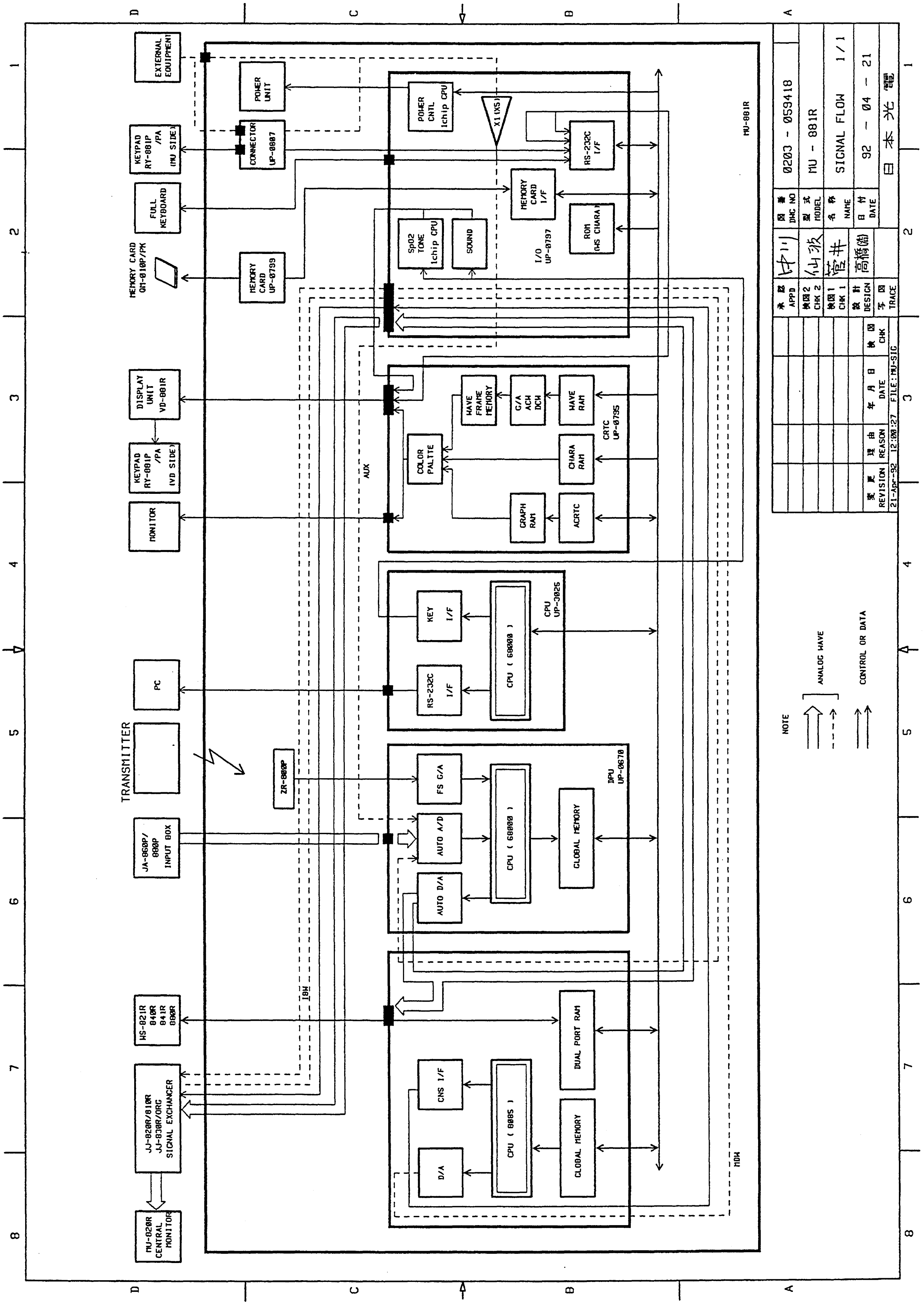
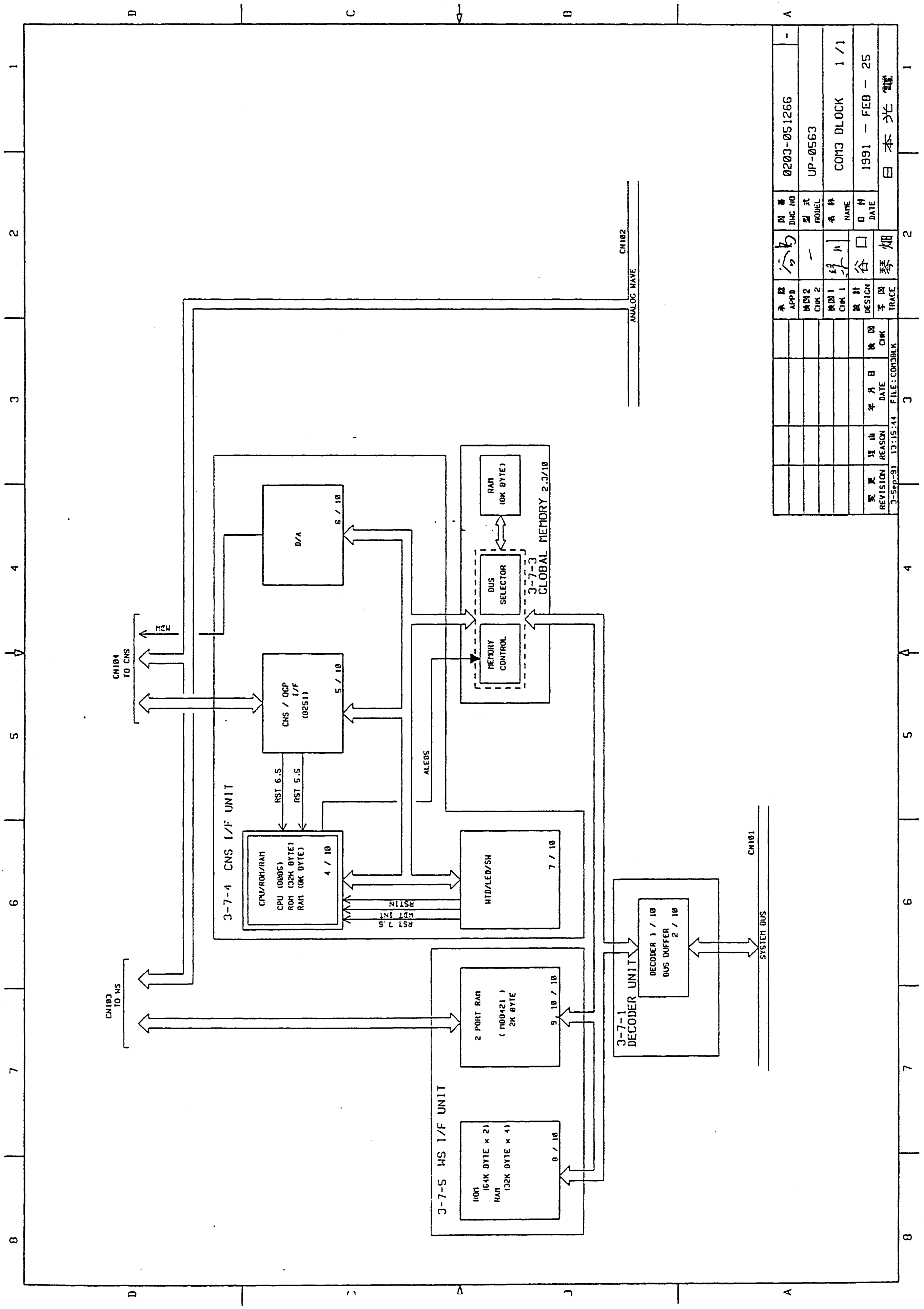
11. BLOCK DIAGRAM


MEMORY CARD QM-010P/PK
MEMORYCARD UP-0799
MOTHER UP-0798
MU-881R
EXT EQUIPMENT
I/O UP-0797
DISPLAY UNIT VD-881R
CRTC UP-0795
CONNECTOR UP-0807
KEYPAD RY-881P/PA (UR-3025)
CPU UR-3027
WS-821R 840R 841R 880R
COMM QI-016P (UP-0563)
POWER UP-0813 SC-010R
FAN
JA-060P JA-080P
DPU UP-0670
ZB-010P ZB-020P ZB-030P ZB-060P
ZR-080P
A B C D
1 2 3 4 5 6 7 8
図番 DWG NO 0203 - 059409
型式 MODEL MU - 881R
名称 NAME SYSTEM BLOCK 1/1
日付 DATE 92 - 04 - 21
日本光電
承認 APP'D 中川
検図2 CHK 2 仙波
検図1 CHK 1 菅井
設計 DESIGN 高橋
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
21-Apr-92 11:57:31 FILE:MU-BLK

11. BLOCK DIAGRAM

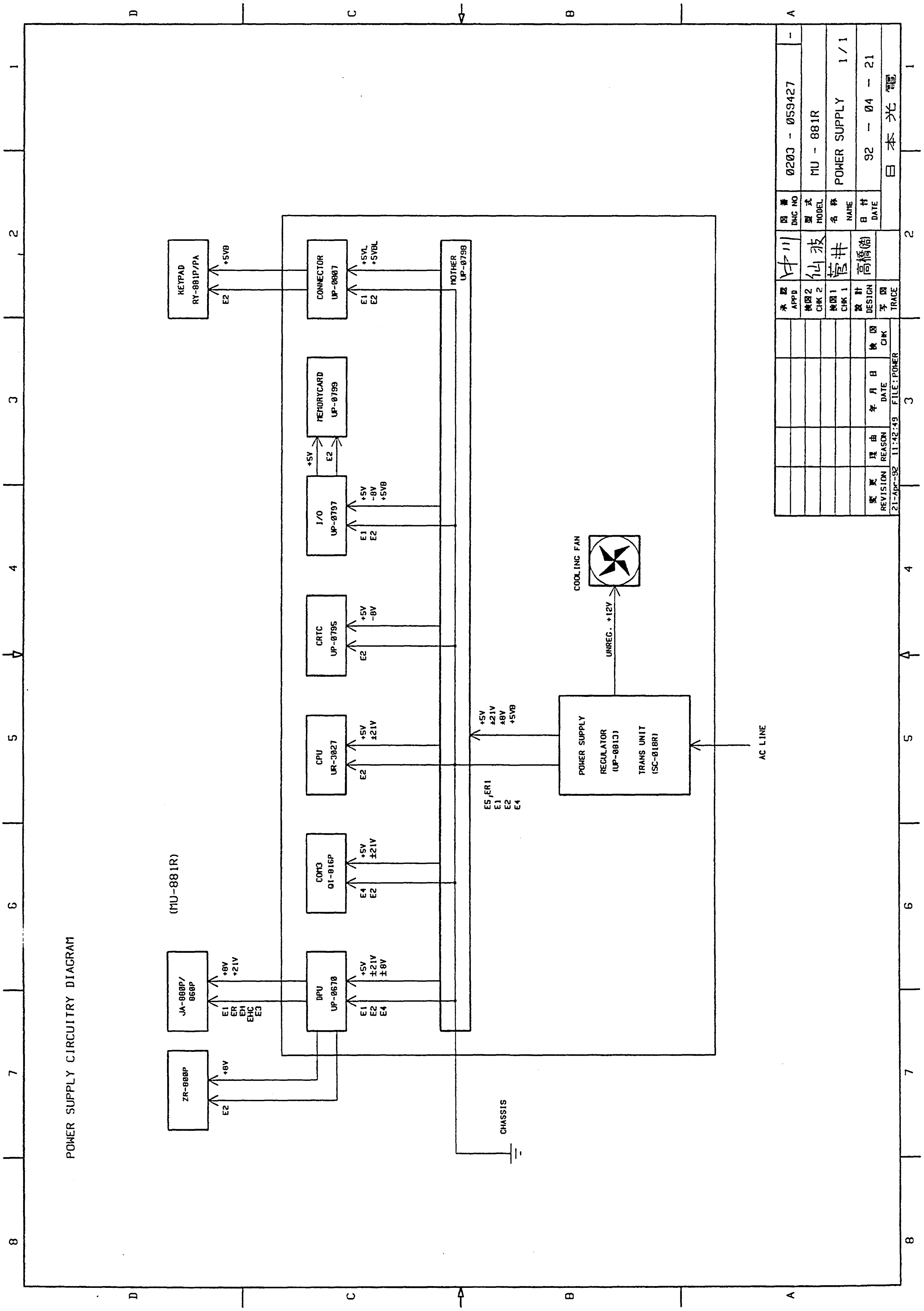

EXTERNAL EQUIPMENT
KEYPAD RY-001P /PA (MU SIDE)
FULL KEYBOARD
MEMORY CARD QM-010P/PK
DISPLAY UNIT VD-001R
KEYPAD RY-001P /PA (VD SIDE)
MONITOR
PC
TRANSMITTER
JA-060P/ 080P INPUT BOX
WS-021R 040R 041R 080R
JJ-020R/010R JJ-030R/ORG SIGNAL EXCHANGER
MU-020R CENTRAL MONITOR
POWER UNIT
CONNECTOR UP-0007
MEMORY CARD UP-0799
POWER CNTL 1chip CPU
X1(XS)
RS-232C I/F
MEMORY CARD I/F
ROM (HS CHARA)
Sp02 TONE 1chip CPU
SOUND
I/O UP-0797
MU-001R
WAVE FRAME MEMORY
G/A ACH DCH
WAVE RAM
CRTC UP-0795
COLOR PALTTE
CHARA RAM
GRAPH RAM
ACRTC
AUX
KEY I/F
CPU (68000)
CPU UP-3025
RS-232C I/F
ZR-000P
FS G/A
AUTO A/D
AUTO D/A
CPU (68000)
GLOBAL MEMORY
DPU UP-0670
IBH
CNS I/F
CPU (8085)
DUAL PORT RAM
GLOBAL MEMORY
D/A
NOH
NOTE
ANALOG WAVE
CONTROL OR DATA
A
B
C
D
1
2
3
4
5
6
7
8
図番 DWG NO
0203 - 059418
型式 MODEL
MU - 001R
名称 NAME
SIGNAL FLOW 1/1
日付 DATE
92 - 04 - 21
日本光電
承認 APPD
中川
検図2 CHK 2
仙波
検図1 CHK 1
笹井
設計 DESIGN
高橋
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
21-APR-92 12:00:27 FILE:MU-SIG

11. BLOCK DIAGRAM

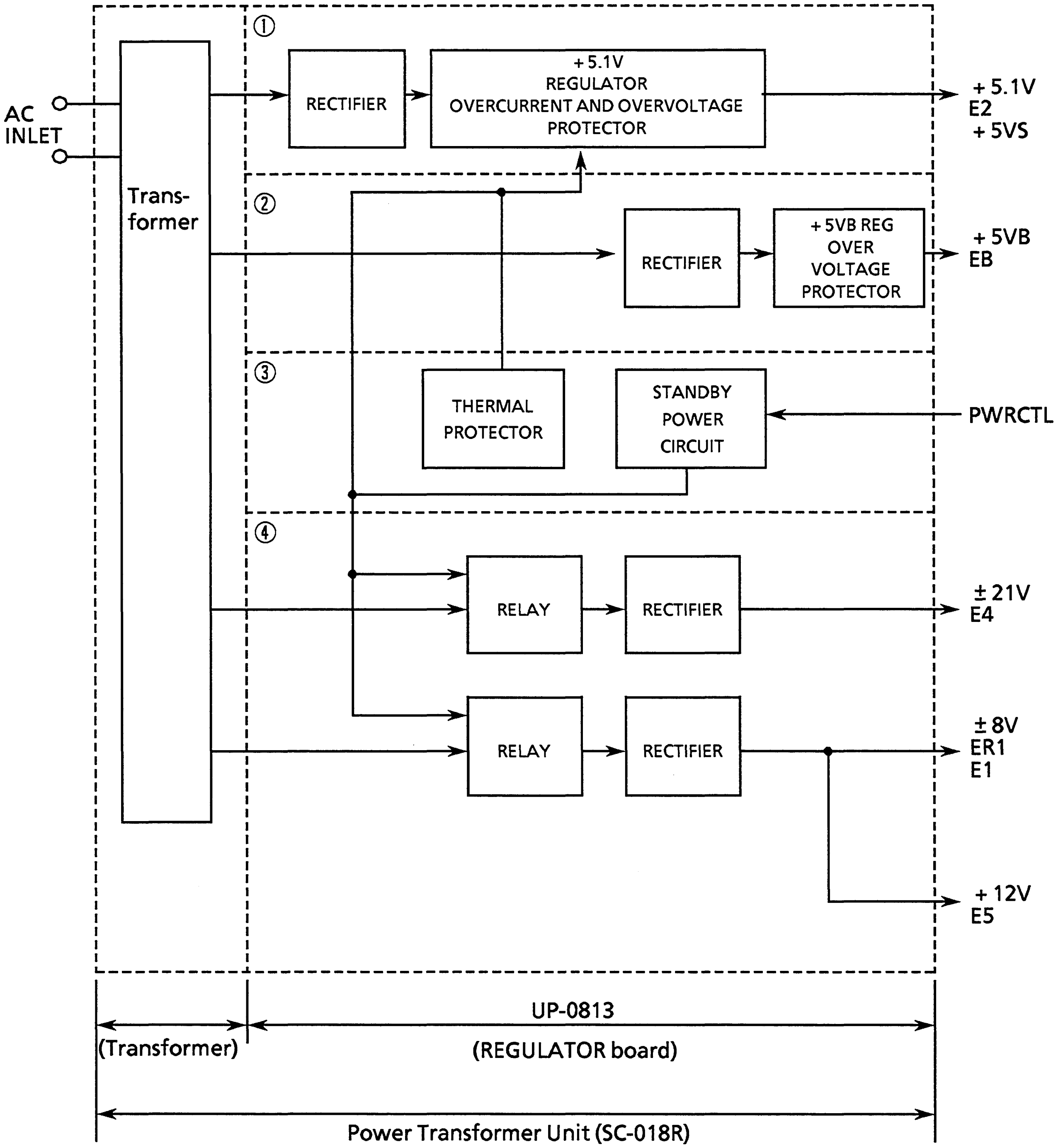


3-7-4 CNS I/F UNIT
D/A
6 / 10
CNS / OCP I/F (8251)
5 / 10
RST 6.5
RST 5.5
CPU/ROM/RAM
CPU (8085)
ROM (32K BYTE)
RAM (8K BYTE)
4 / 10
RSTIN
KEY INT
RST 7.5
WTD/LED/SW
7 / 10
ALE8S
3-7-3 GLOBAL MEMORY 2.3/10
RAM (8K BYTE)
BUS SELECTOR
MEMORY CONTROL
CN104 TO CNS
CN103 TO WS
CN102
ANALOG WAVE
CN101
SYSTEM BUS
3-7-1 DECODER UNIT
DECODER 1 / 10
BUS BUFFER 2 / 10
3-7-5 WS I/F UNIT
2 PORT RAM (MB8421) 2K BYTE
9, 10 / 10
ROM (64K BYTE × 2)
RAM (32K BYTE × 4)
8 / 10
1
2
3
4
5
6
7
8
A
B
C
D
0203-051266
-
図番 DWG NO
型式 MODEL
UP-0563
名称 NAME
COM3 BLOCK 1 / 1
日付 DATE
1991 - FEB - 25
日本光電
承認 APP'D
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
谷口
琴畑
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
3-Sep-91 13:15:44 FILE:COM3BLK

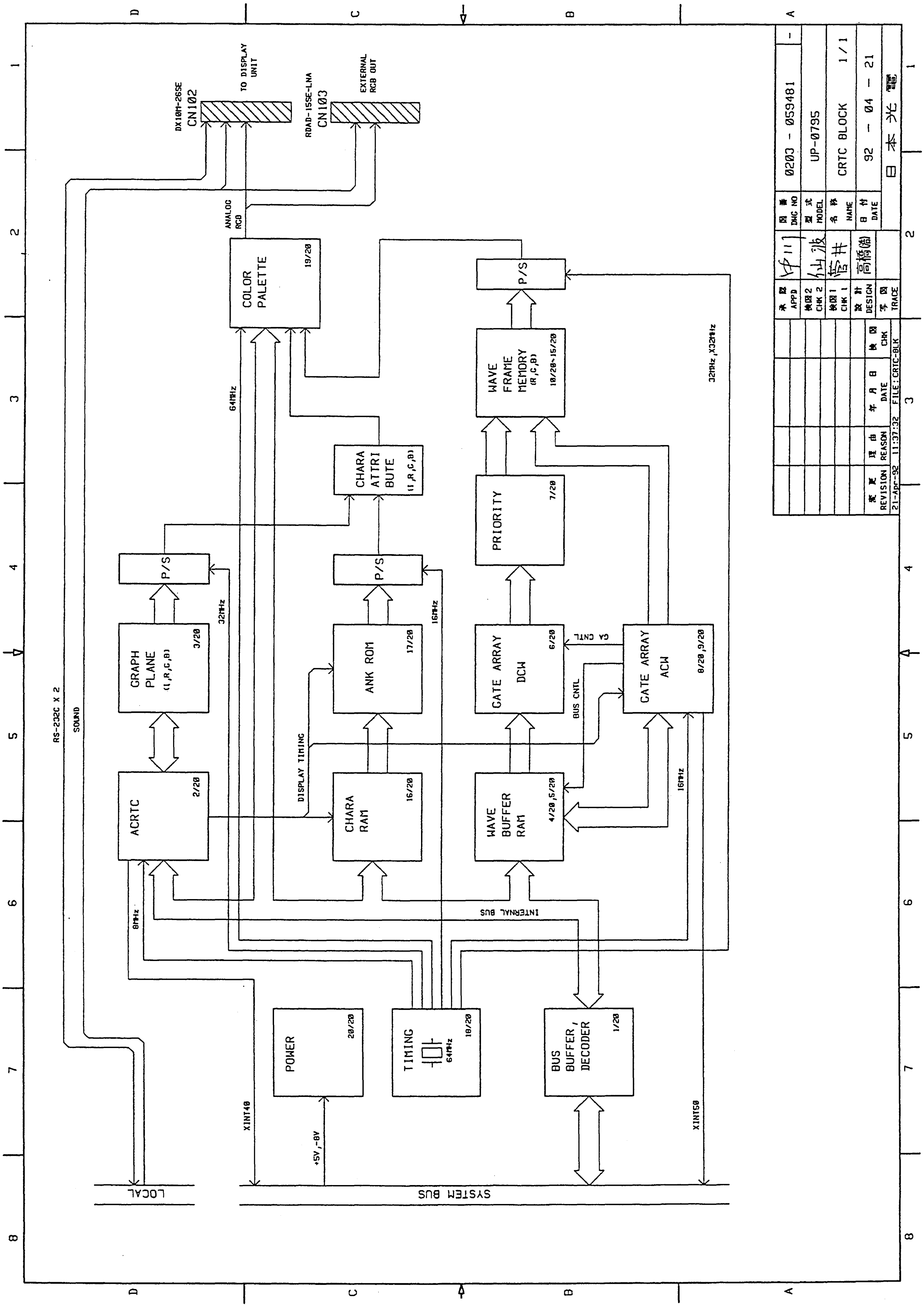
11. BLOCK DIAGRAM

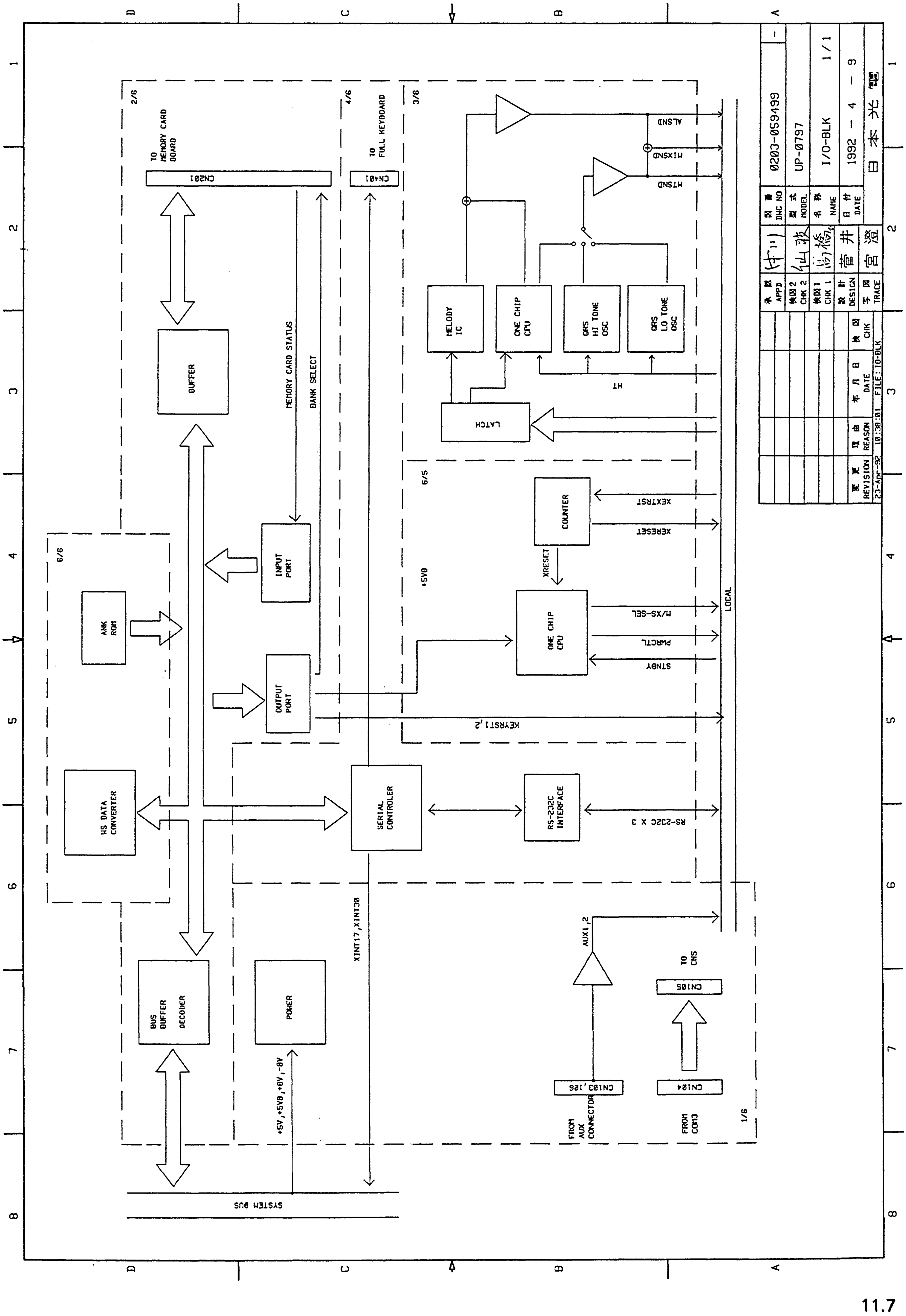

POWER SUPPLY CIRCUITRY DIAGRAM
(MU-881R)
KEYPAD RY-881P/PA
+5VB
E2
CONNECTOR UP-0807
+5VL
+5VBL
E1
E2
MOTHER UP-0798
MEMORYCARD UP-0799
+5V
E2
I/O UP-0797
+5V
-8V
+5VB
E1
E2
CRTC UP-0795
+5V
-8V
E2
CPU UR-3027
+5V
±21V
E2
COM3 QI-816P
+5V
±21V
E4
E2
DPU UP-0670
+5V
±21V
±8V
E1
E2
E4
JA-800P/860P
+8V
+21V
E1
ER
EH
EHC
E3
ZR-800P
+8V
E2
CHASSIS
+5V
±21V
±8V
+5VB
E5,ER1
E1
E2
E4
POWER SUPPLY
REGULATOR (UP-0813)
TRANS UNIT (SC-018R)
AC LINE
UNREG. +12V
COOLING FAN
A
B
C
D
1
2
3
4
5
6
7
8
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
中川
仙波
菅井
高橋(億)
図番 DWG NO
0203 - 059427
-
型式 MODEL
MU - 881R
名称 NAME
POWER SUPPLY 1/1
日付 DATE
92 - 04 - 21
日本光電
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
21-Apr-92 11:42:49 FILE:POWER

Power Tranfrormer Unit, SC-018R

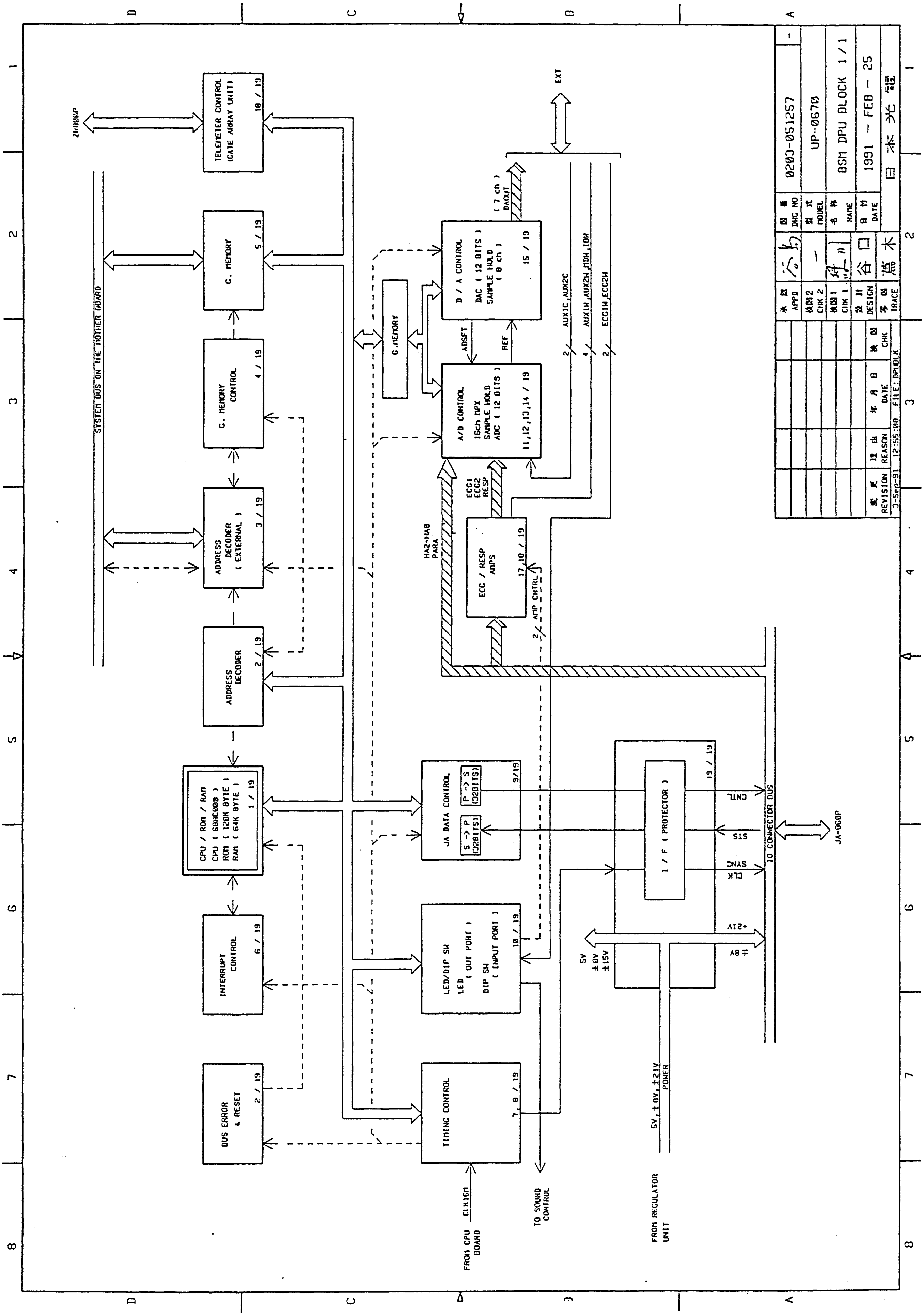

AC
INLET
Trans-
former
①
RECTIFIER
+5.1V
REGULATOR
OVERCURRENT AND OVERVOLTAGE
PROTECTOR
+5.1V
E2
+5VS
②
RECTIFIER
+5VB REG
OVER
VOLTAGE
PROTECTOR
+5VB
EB
③
THERMAL
PROTECTOR
STANDBY
POWER
CIRCUIT
PWRCTL
④
RELAY
RECTIFIER
±21V
E4
RELAY
RECTIFIER
±8V
ER1
E1
+12V
E5
(Transformer)
UP-0813
(REGULATOR board)
Power Transformer Unit (SC-018R)

11. BLOCK DIAGRAM

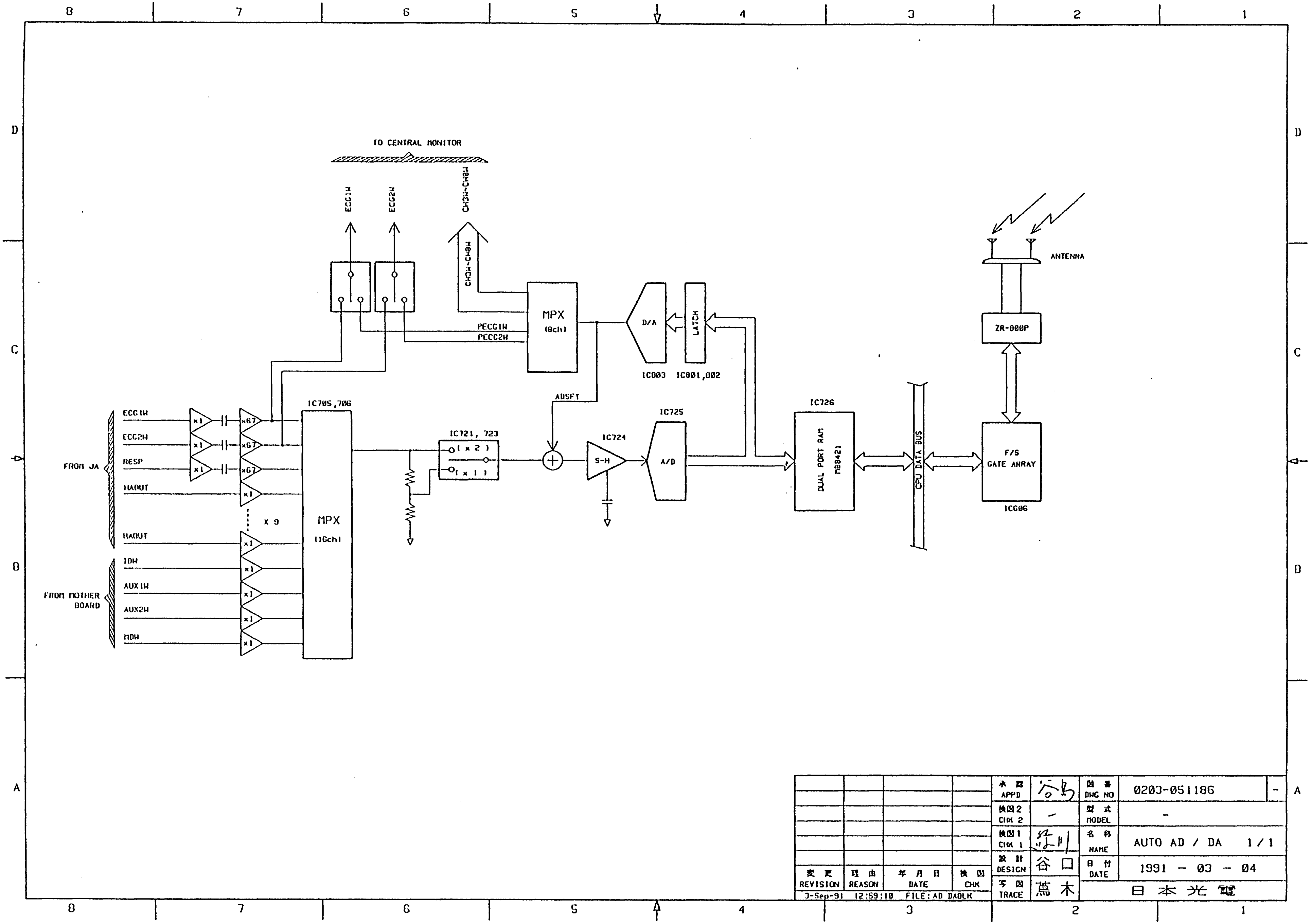

DX10M-26SE
CN102
TO DISPLAY UNIT
RDAD-15SE-LNA
CN103
EXTERNAL RGB OUT
ANALOG RGB
COLOR PALETTE 19/20
P/S
WAVE FRAME MEMORY (R,G,B) 10/20~15/20
32MHz,X32MHz
64MHz
CHARA ATTRI BUTE (I,R,G,B)
PRIORITY 7/20
P/S
P/S
32MHz
16MHz
GRAPH PLANE (I,R,G,B) 3/20
ANK ROM 17/20
GATE ARRAY DCW 6/20
GA CNTL
GATE ARRAY ACW 8/20,9/20
BUS CNTL
RS-232C X 2
SOUND
DISPLAY TIMING
ACRTC 2/20
CHARA RAM 16/20
WAVE BUFFER RAM 4/20,5/20
16MHz
INTERNAL BUS
8MHz
POWER 20/20
TIMING 64MHz 18/20
BUS BUFFER, DECODER 1/20
XINT40
+5V,-8V
XINT50
LOCAL
SYSTEM BUS
図番 DWG NO 0203 - 059481 -
型式 MODEL UP-0795
名称 NAME CRTC BLOCK 1/1
日付 DATE 92 - 04 - 21
日本光電
承認 APPD 中川
検図2 CHK 2 仙波
検図1 CHK 1 菅井
設計 DESIGN 高橋
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
21-Apr-92 11:37:32 FILE:CRTC-BLK
A B C D
1 2 3 4 5 6 7 8


TO MEMORY CARD BOARD
CN201
2/6
4/6
TO FULL KEYBOARD
CN401
3/6
ALSND
MIXSND
HTSND
MELODY IC
ONE CHIP CPU
QRS HI TONE OSC
QRS LO TONE OSC
HT
LATCH
BUFFER
MEMORY CARD STATUS
BANK SELECT
6/6
ANK ROM
INPUT PORT
OUTPUT PORT
5/6
+5VB
COUNTER
XEXTRST
XERESET
XRESET
ONE CHIP CPU
M/XS-SEL
PWRCTL
STNBY
LOCAL
KEYRST1,2
HS DATA CONVERTER
SERIAL CONTROLER
RS-232C INTERFACE
RS-232C X 3
XINT17,XINT30
AUX1,2
TO CNS
CN105
CN104
CN103,106
FROM AUX CONNECTOR
FROM COM3
1/6
BUS BUFFER DECODER
POWER
+5V,+5VB,+8V,-8V
SYSTEM BUS
図番 DWG NO
0203-059499
型式 MODEL
UP-0797
名称 NAME
I/O-BLK
1/1
日付 DATE
1992 - 4 - 9
日本光電
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
中川
仙波
高橋
菅井
宮澄
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
23-Apr-92 10:38:01 FILE: IO-BLK
A
B
C
D
1
2
3
4
5
6
7
8

11. BLOCK DIAGRAM

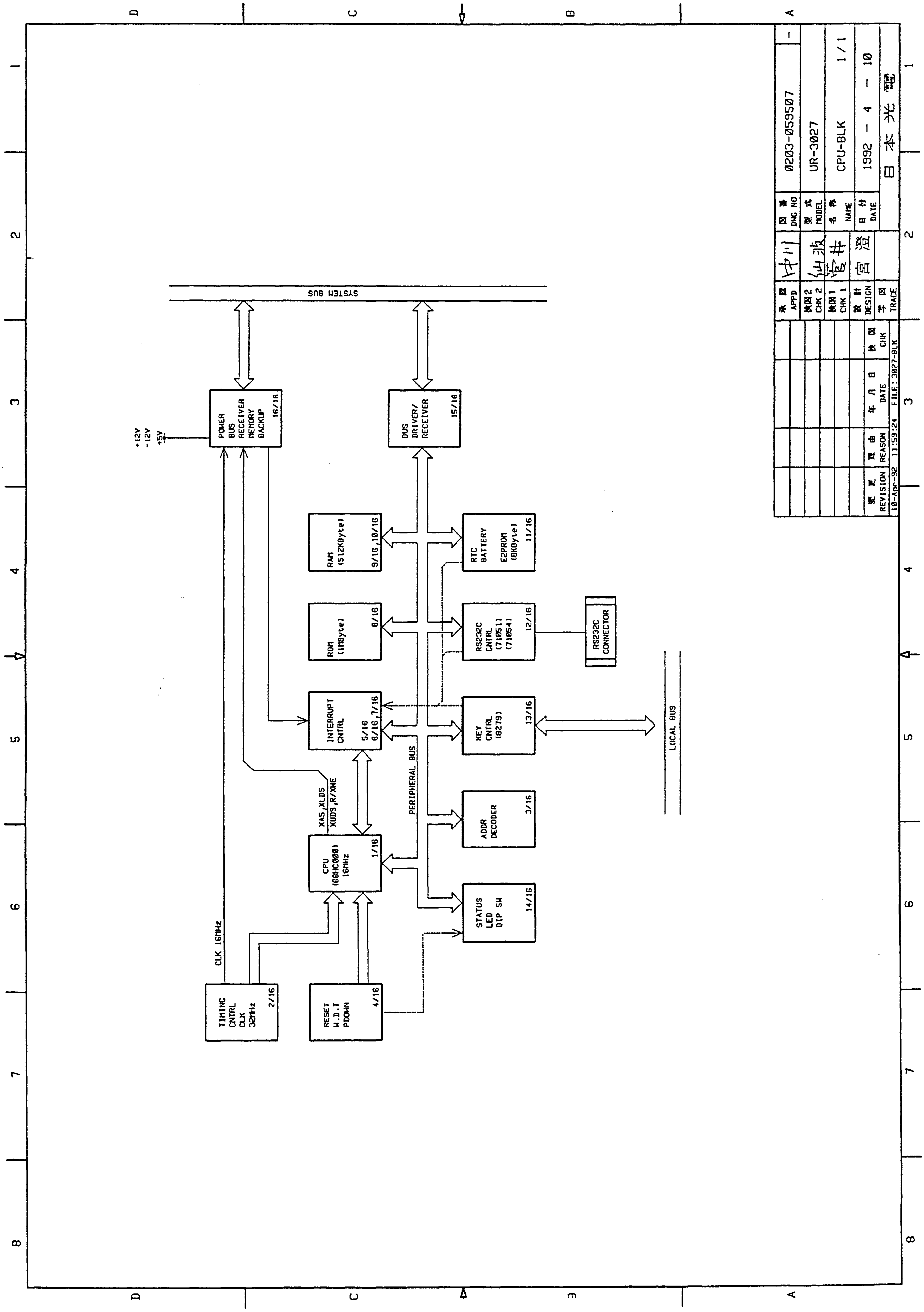

TELEMETER CONTROL (GATE ARRAY UNIT) 10 / 19
G. MEMORY 5 / 19
G. MEMORY CONTROL 4 / 19
ADDRESS DECODER (EXTERNAL) 3 / 19
ADDRESS DECODER 2 / 19
CPU / ROM / RAM
CPU (6DHC000)
ROM (120K BYTE)
RAM (64K BYTE) 1 / 19
INTERRUPT CONTROL 6 / 19
BUS ERROR & RESET 2 / 19
SYSTEM BUS ON THE MOTHER BOARD
TIMING CONTROL 7, 8 / 19
LED/DIP SW
LED (OUT PORT)
DIP SW (INPUT PORT) 10 / 19
JA DATA CONTROL 9/19
P -> S (32BITS)
S -> P (32BITS)
I / F (PROTECTOR) 19 / 19
ECC / RESP AMPS 17, 18 / 19
AMP CNTRL
A/D CONTROL
16ch MPX
SAMPLE HOLD
ADC (12 BITS) 11, 12, 13, 14 / 19
D / A CONTROL
DAC (12 BITS)
SAMPLE HOLD (8 ch) 15 / 19
G.MEMORY
ADSFT
REF
(7 ch) DAOUT
EXT
AUX1C, AUX2C
AUX1H, AUX2H, MDH, IDH
ECC1H, ECC2H
ECC1 ECC2 RESP
HA2~HA0 PARA
IO CONNECTOR BUS
JA-060P
CNTL
STS
SYNC
CLK
+21V
±8V
5V ±0V ±15V
5V, ±0V, ±21V POWER
FROM CPU BOARD
CLK16M
TO SOUND CONTROL
FROM REGULATOR UNIT
D
C
B
A
1
2
3
4
5
6
7
8
図番 DWG NO
0203-051257
型式 MODEL
UP-0670
名称 NAME
BSM DPU BLOCK 1/1
日付 DATE
1991 - FEB - 25
日本光電
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
3-Sep-91 12:55:00 FILE: DPUBLK

11. BLOCK DIAGRAM

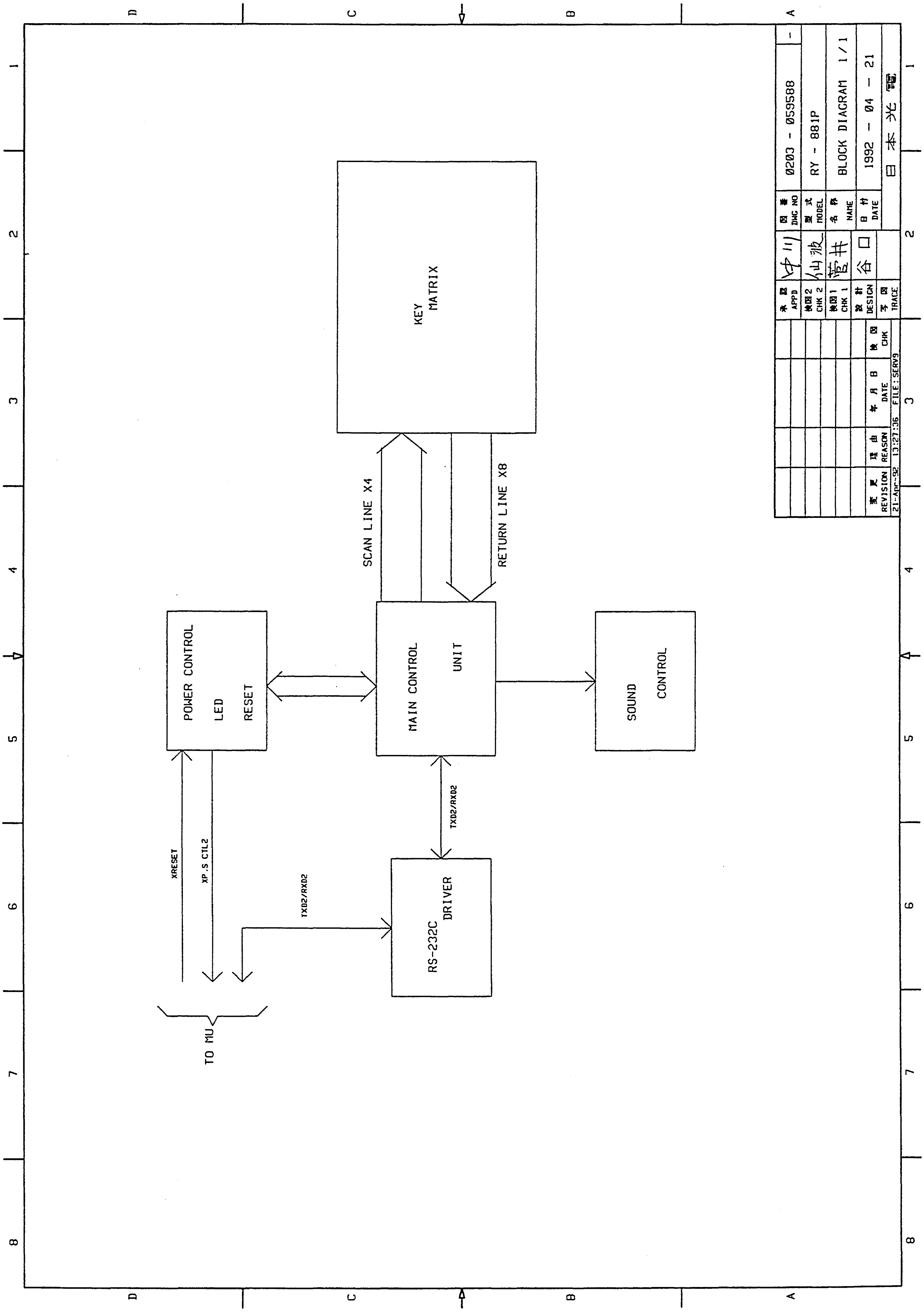


TO CENTRAL MONITOR
ECG1W
ECG2W
CH3W~CH8W
ANTENNA
ZR-000P
MPX
(8ch)
PECG1W
PECG2W
D/A
LATCH
IC003
IC001,002
ADSFT
IC725
A/D
IC724
S-H
IC726
DUAL PORT RAM
MB8421
CPU DATA BUS
F/S
GATE ARRAY
IC606
IC705,706
MPX
(16ch)
IC721, 723
(x 2)
(x 1)
FROM JA
ECG1W
ECG2W
RESP
HAOUT
FROM MOTHER BOARD
IDW
AUX1W
AUX2W
MDW
x1
x67
x 9
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
谷口
写図 TRACE
蔦木
図番 DWG NO
0203-051186
-
型式 MODEL
-
名称 NAME
AUTO AD / DA 1 / 1
日付 DATE
1991 - 03 - 04
日本光電
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
3-Sep-91 12:59:10 FILE:AD DABLK
A
B
C
D
1
2
3
4
5
6
7
8

11. BLOCK DIAGRAM

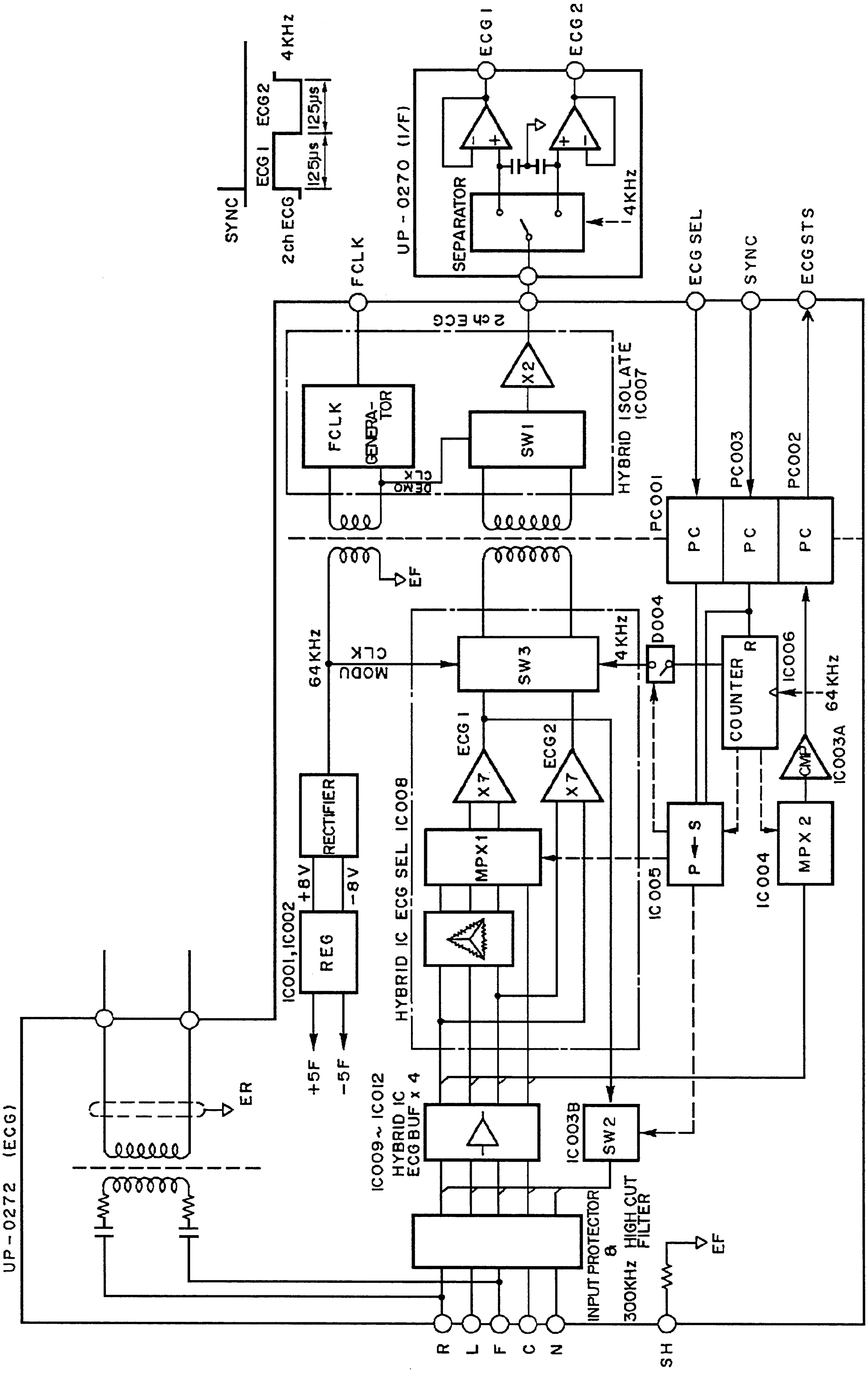

SYSTEM BUS
POWER BUS RECEIVER MEMORY BACKUP 16/16
+12V
-12V
+5V
BUS DRIVER/ RECEIVER 15/16
RAM (512KByte) 9/16,10/16
RTC BATTERY E2PROM (8KByte) 11/16
ROM (1MByte) 8/16
RS232C CNTRL (71051) (71054) 12/16
RS232C CONNECTOR
INTERRUPT CNTRL 5/16 6/16,7/16
KEY CNTRL (8279) 13/16
LOCAL BUS
XAS,XLDS
XUDS,R/XWE
PERIPHERAL BUS
ADDR DECODER 3/16
CPU (68HC000) 16MHz 1/16
STATUS LED DIP SW 14/16
CLK 16MHz
TIMING CNTRL CLK 32MHz 2/16
RESET W.D.T PDOWN 4/16
図番 DWG NO
0203-059507
-
型式 MODEL
UR-3027
名称 NAME
CPU-BLK 1/1
日付 DATE
1992 - 4 - 10
日本光電
承認 APPD
中川
検図2 CHK 2
仙波
検図1 CHK 1
宮井
設計 DESIGN
宮澄
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
10-Apr-92 11:59:24 FILE:3027-BLK
D
C
B
A
1
2
3
4
5
6
7
8

11. BLOCK DIAGRAM


KEY MATRIX
SCAN LINE X4
RETURN LINE X8
POWER CONTROL
LED
RESET
MAIN CONTROL UNIT
SOUND CONTROL
TXD2/RXD2
RS-232C DRIVER
XRESET
XP.S CTL2
TXD2/RXD2
TO MU
図番 DWG NO 0203 - 059588 -
型式 MODEL RY - 881P
名称 NAME BLOCK DIAGRAM 1/1
日付 DATE 1992 - 04 - 21
日本光電
承認 APPD 中川
検図2 CHK 2 仙波
検図1 CHK 1 菅井
設計 DESIGN 谷口
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
21-Apr-92 13:27:36 FILE:SERV9
A B C D
1 2 3 4 5 6 7 8

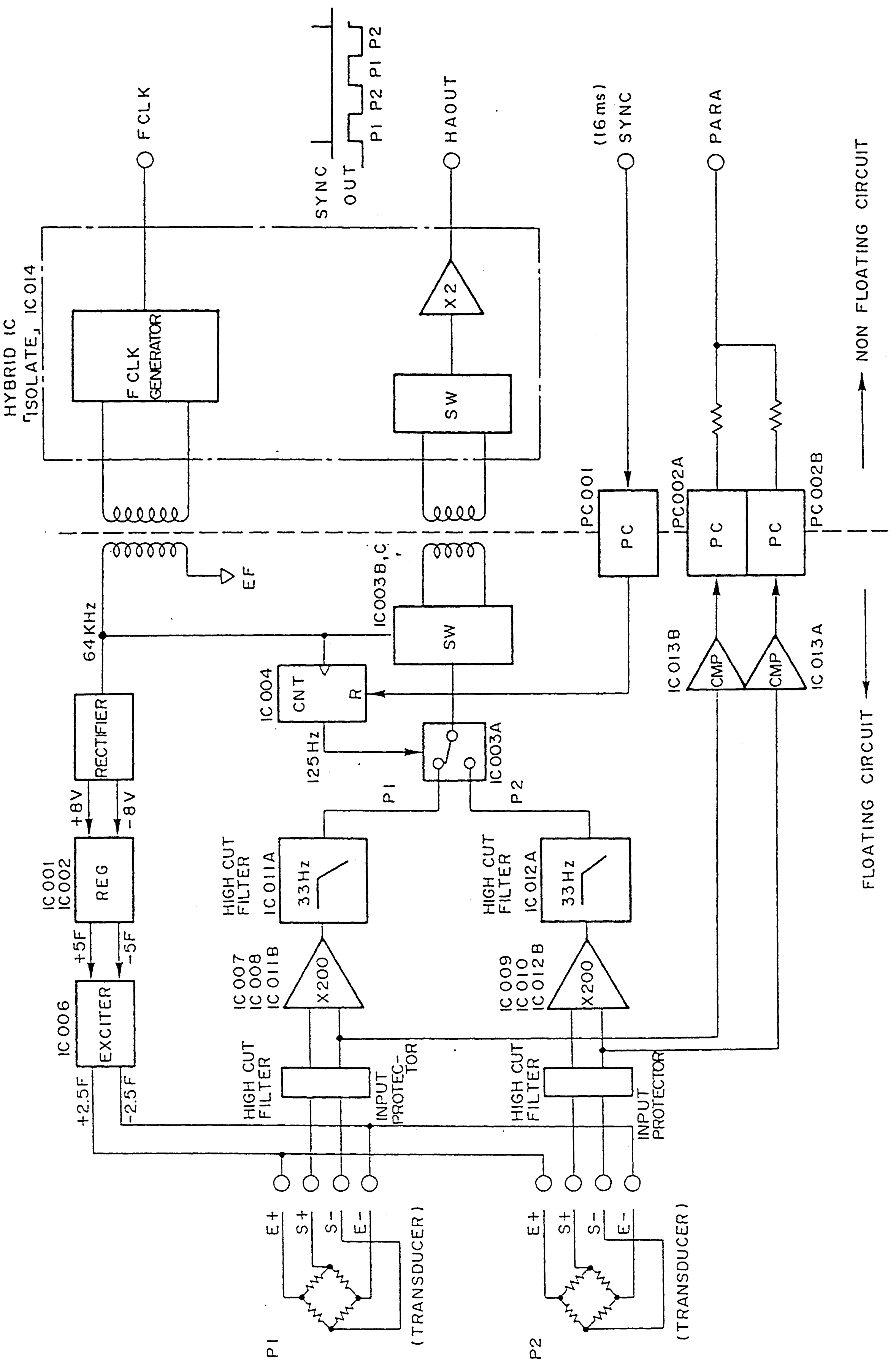
11. BLOCK DIAGRAM

ECG/Respiration Head Amp, AC-800P


SYNC
2ch ECG
ECG 1
ECG2
4KHz
125μs
125μs
ECG 1
ECG 2
UP - 0270 (I/F)
SEPARATOR
4KHz
FCLK
ECG SEL
SYNC
ECG STS
2 ch ECG
X2
FCLK GENERA-TOR
SW1
DEMO CLK
HYBRID ISOLATE IC007
PC001
PC003
PC002
PC
PC
PC
EF
64KHz
MODU CLK
SW3
4KHz
D004
COUNTER
R
IC006
64KHz
ECG 1
ECG2
X7
X7
CMP
IC003A
RECTIFIER
+8V
-8V
MPX1
P ← S
MPX 2
IC005
IC004
HYBRID IC ECG SEL IC008
REG
IC001,IC002
+5F
-5F
ER
IC009~ IC012
HYBRID IC
ECG BUF x 4
IC003B
SW2
UP - 0272 (ECG)
INPUT PROTECTOR &
300KHz HIGH CUT FILTER
EF
R
L
F
C
N
SH

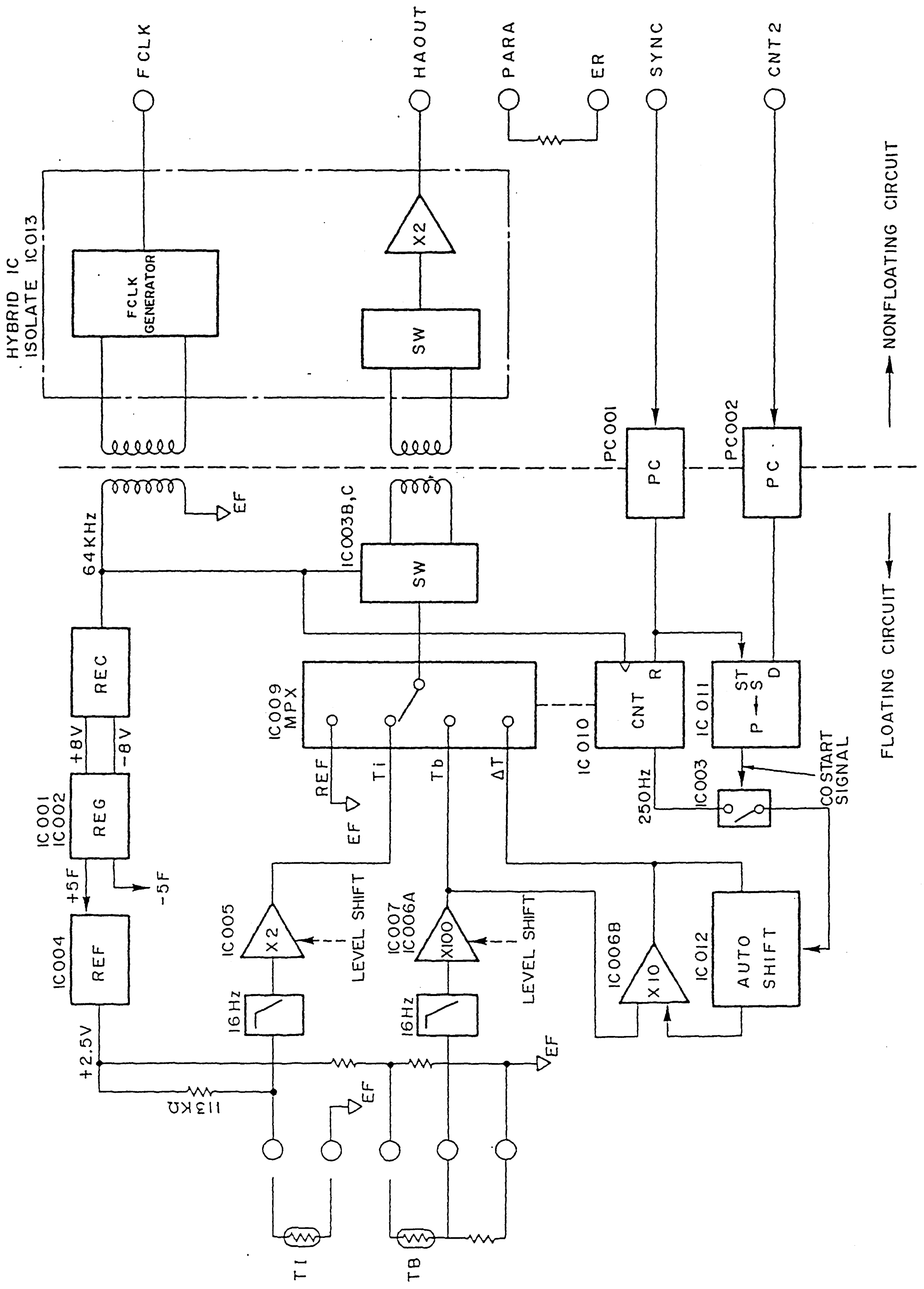
11. BLOCK DIAGRAM

PRESS Head Amp, AP-800PA

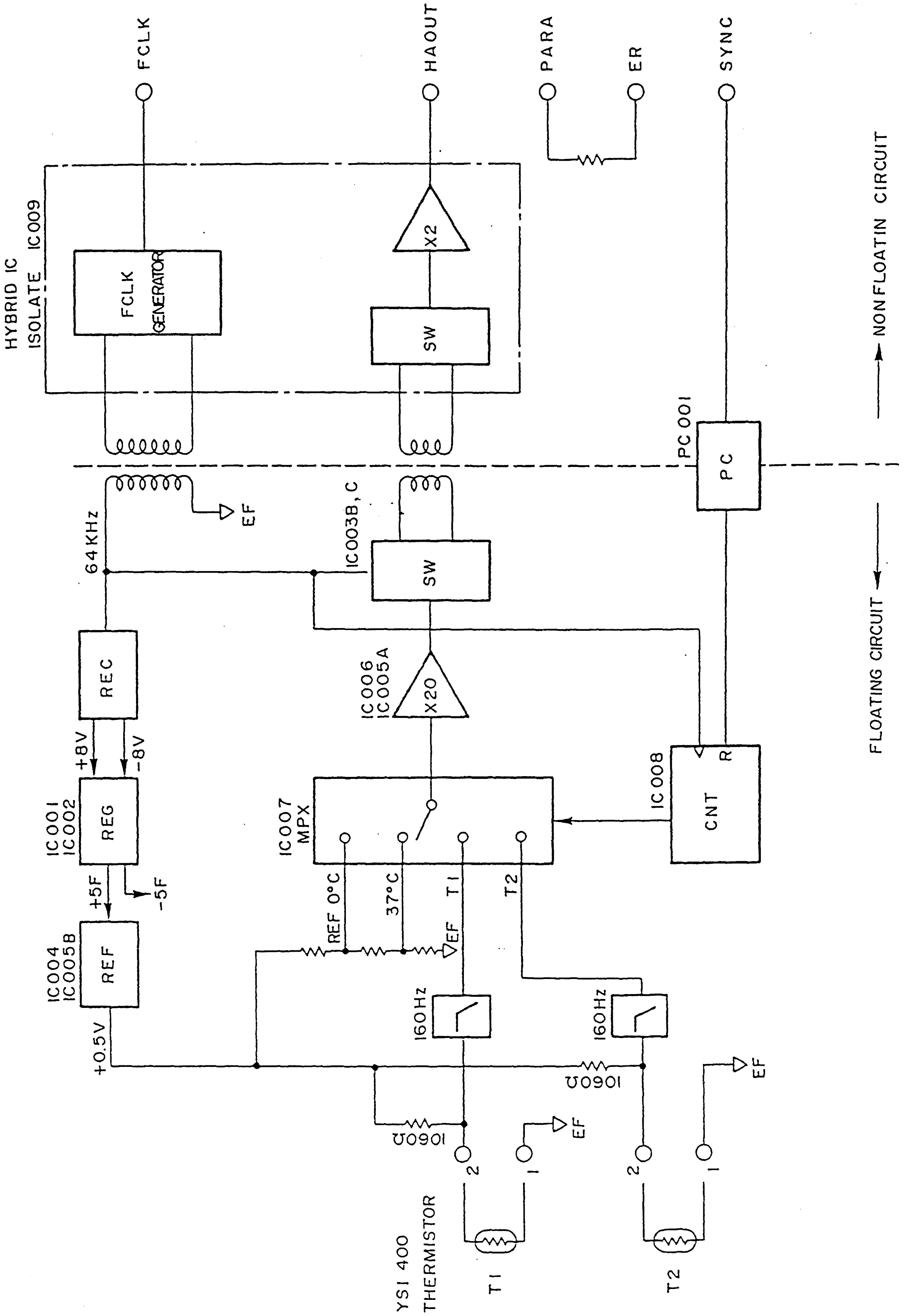

FCLK
SYNC
OUT
P1 P2 P1 P2
HAOUT
(16ms) SYNC
PARA
HYBRID IC
[ISOLATE] IC014
F CLK GENERATOR
X2
SW
NON FLOATING CIRCUIT
FLOATING CIRCUIT
PC001
PC
IPC002A
PC
PC
PC002B
EF
64KHz
IC003B,C
SW
IC004
CNT
R
125Hz
IC003A
P1
P2
IC013B
CMP
CMP
IC013A
RECTIFIER
+8V
-8V
IC001
IC002
REG
+5F
-5F
IC006
EXCITER
+2.5F
-2.5F
HIGH CUT FILTER
IC011A
33Hz
HIGH CUT FILTER
IC012A
33Hz
IC007
IC008
IC011B
X200
IC009
IC010
IC012B
X200
HIGH CUT FILTER
INPUT PROTECTOR
HIGH CUT FILTER
INPUT PROTECTOR
E+
S+
S-
E-
P1
(TRANSDUCER)
E+
S+
S-
E-
P2
(TRANSDUCER)

11. BLOCK DIAGRAM

CO Head Amp, AH-800PA

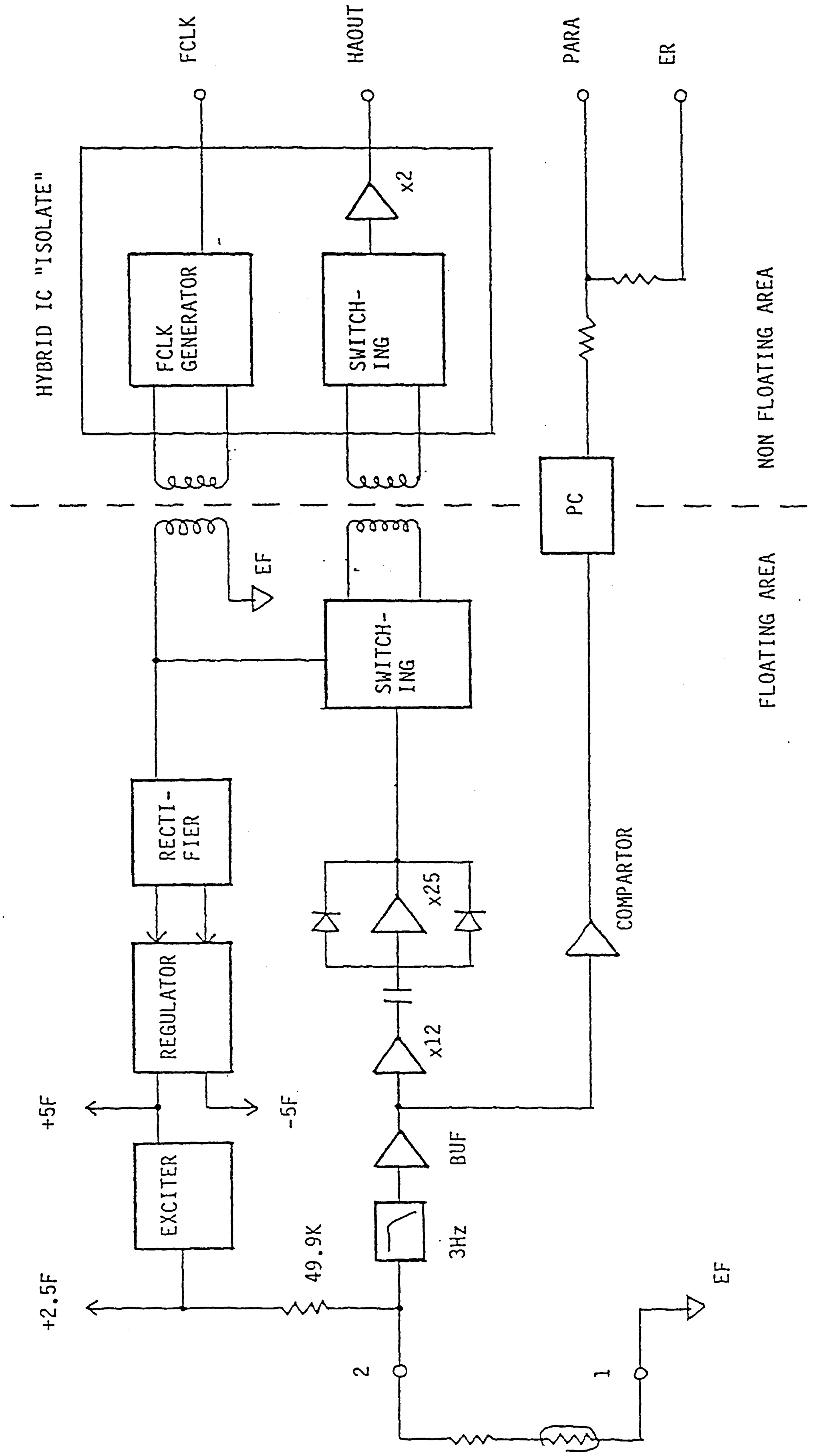

FCLK
HAOUT
PARA
ER
SYNC
CNT2
HYBRID IC
ISOLATE IC013
FCLK GENERATOR
X2
SW
NONFLOATING CIRCUIT
FLOATING CIRCUIT
PC001
PC
PC002
PC
64KHz
EF
IC003B,C
SW
REC
+8V
-8V
IC001
IC002
REG
+5F
-5F
IC004
REF
+2.5V
113KΩ
IC009
MPX
REF
EF
Ti
Tb
ΔT
IC010
CNT
R
IC011
ST
P→S
D
250Hz
IC003
COSTART SIGNAL
IC005
X2
LEVEL SHIFT
IC007
IC006A
X100
LEVEL SHIFT
16Hz
16Hz
IC006B
X10
IC012
AUTO SHIFT
EF
EF
TI
TB

TEMP Head Amp, AW-800PA

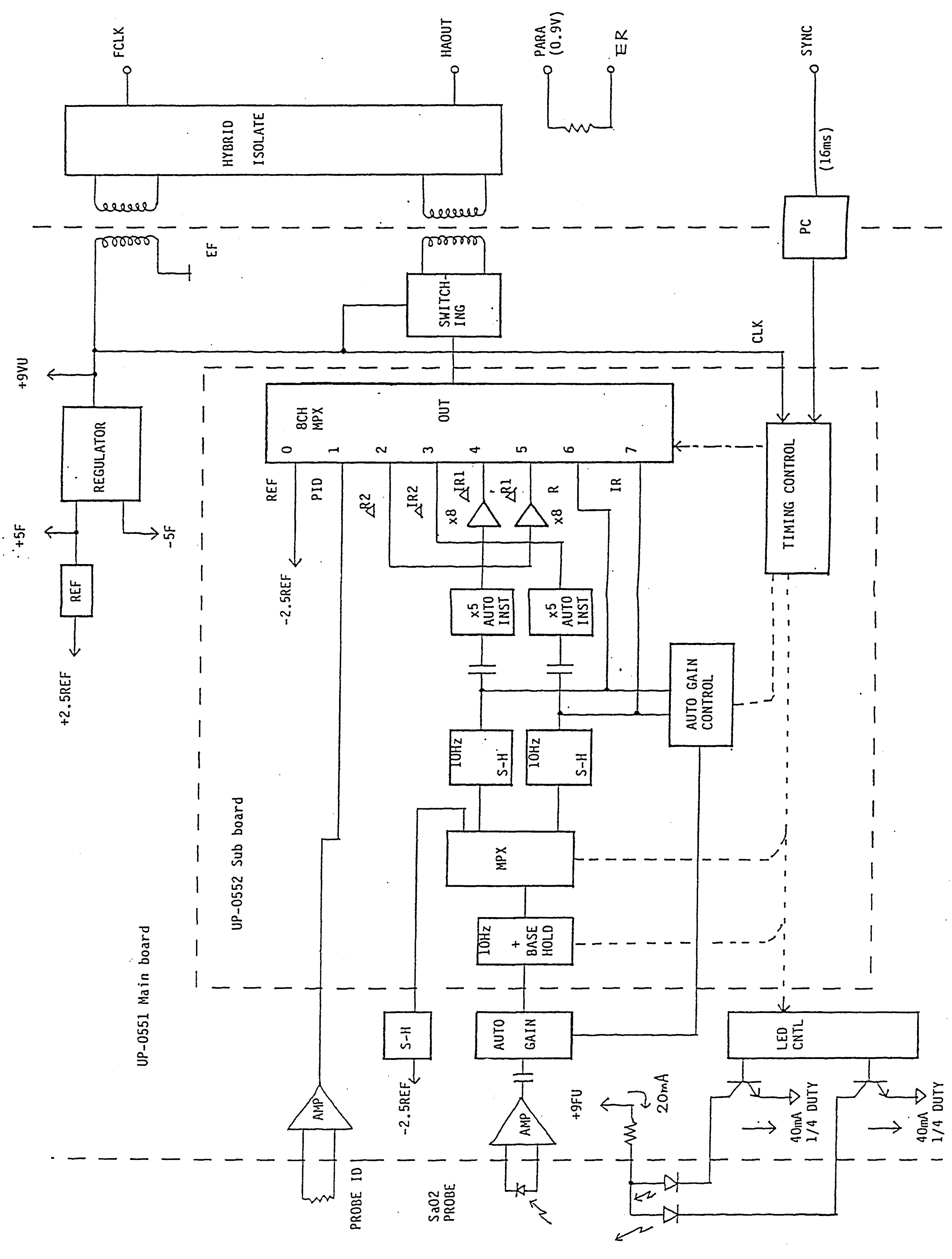

FCLK
HAOUT
PARA
ER
SYNC
HYBRID IC
ISOLATE IC009
FCLK GENERATOR
X2
SW
NON FLOATIN CIRCUIT
FLOATING CIRCUIT
PC001
PC
64KHz
EF
IC003B, C
SW
REC
IC006
IC005A
X20
+8V
-8V
IC001
IC002
REG
IC007
MPX
IC008
CNT
R
+5F
-5F
IC004
IC005B
REF
REF 0°C
37°C
T1
T2
EF
160Hz
160Hz
+0.5V
1060Ω
1060Ω
EF
EF
2
1
2
1
YSI 400
THERMISTOR
T1
T2

11. BLOCK DIAGRAM

RESPIRATION Head Amp, AR-800PA

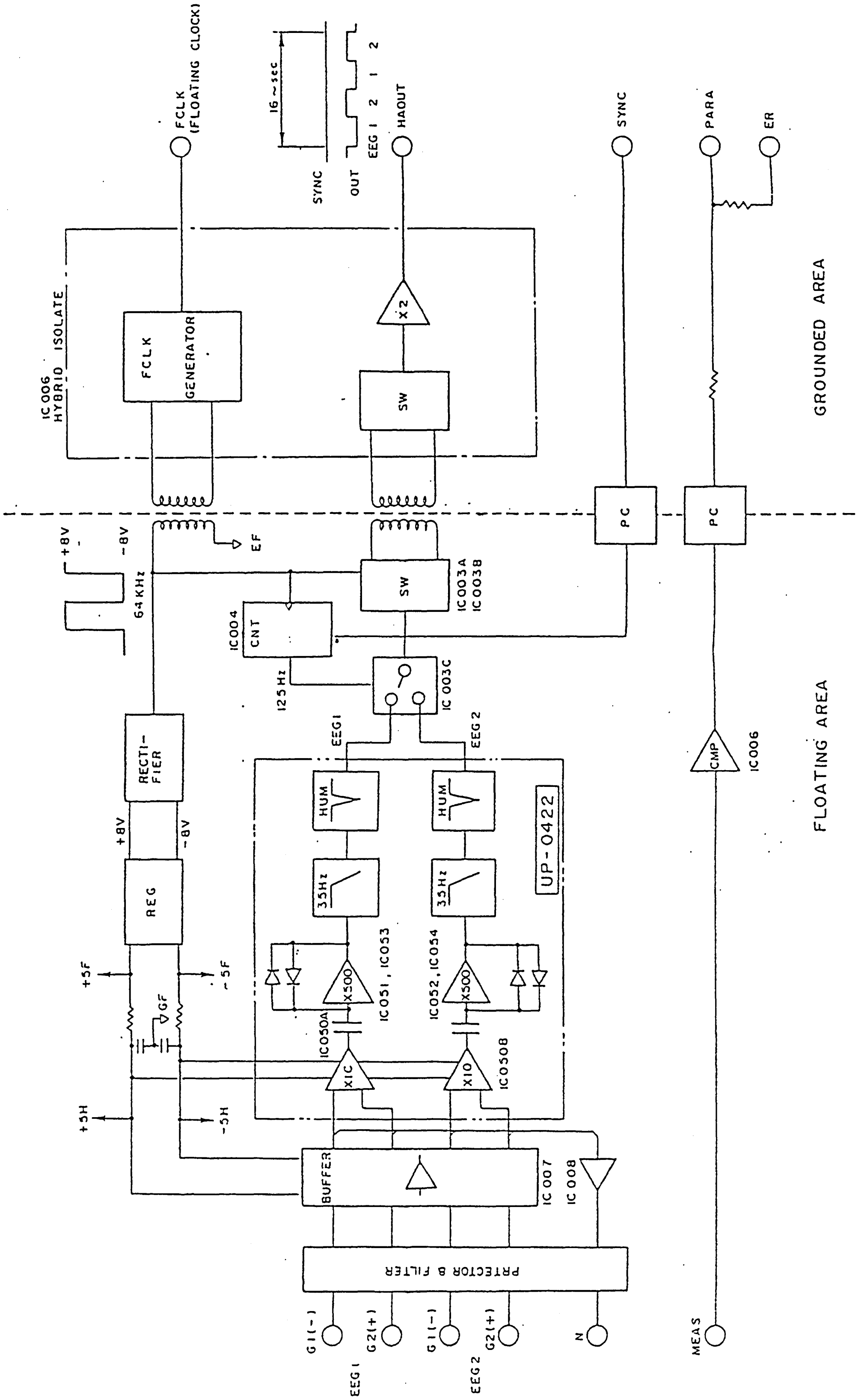

FCLK
HAOUT
PARA
ER
HYBRID IC "ISOLATE"
x2
FCLK GENERATOR
SWITCH-ING
NON FLOATING AREA
PC
EF
SWITCH-ING
FLOATING AREA
RECTI-FIER
x25
COMPARTOR
REGULATOR
x12
+5F
-5F
EXCITER
BUF
49.9K
3Hz
+2.5F
EF
2
1

SpO$_2$ Head Amp, AL-800PA


FCLK
HAOUT
PARA
(0.9V)
ER
SYNC
HYBRID
ISOLATE
(16ms)
PC
EF
SWITCH-
ING
CLK
+9VU
REGULATOR
+5F
-5F
REF
+2.5REF
8CH
MPX
OUT
0
1
2
3
4
5
6
7
REF
PID
R2
IR2
IR1
R1
R
IR
x8
x8
-2.5REF
TIMING CONTROL
x5
AUTO
INST
x5
AUTO
INST
AUTO GAIN
CONTROL
10Hz
S-H
10Hz
S-H
MPX
10Hz
+
BASE
HOLD
UP-0552 Sub board
UP-0551 Main board
S-H
-2.5REF
AUTO
GAIN
LED
CNTL
AMP
AMP
+9FU
20mA
40mA
1/4 DUTY
40mA
1/4 DUTY
PROBE ID
SaO2
PROBE

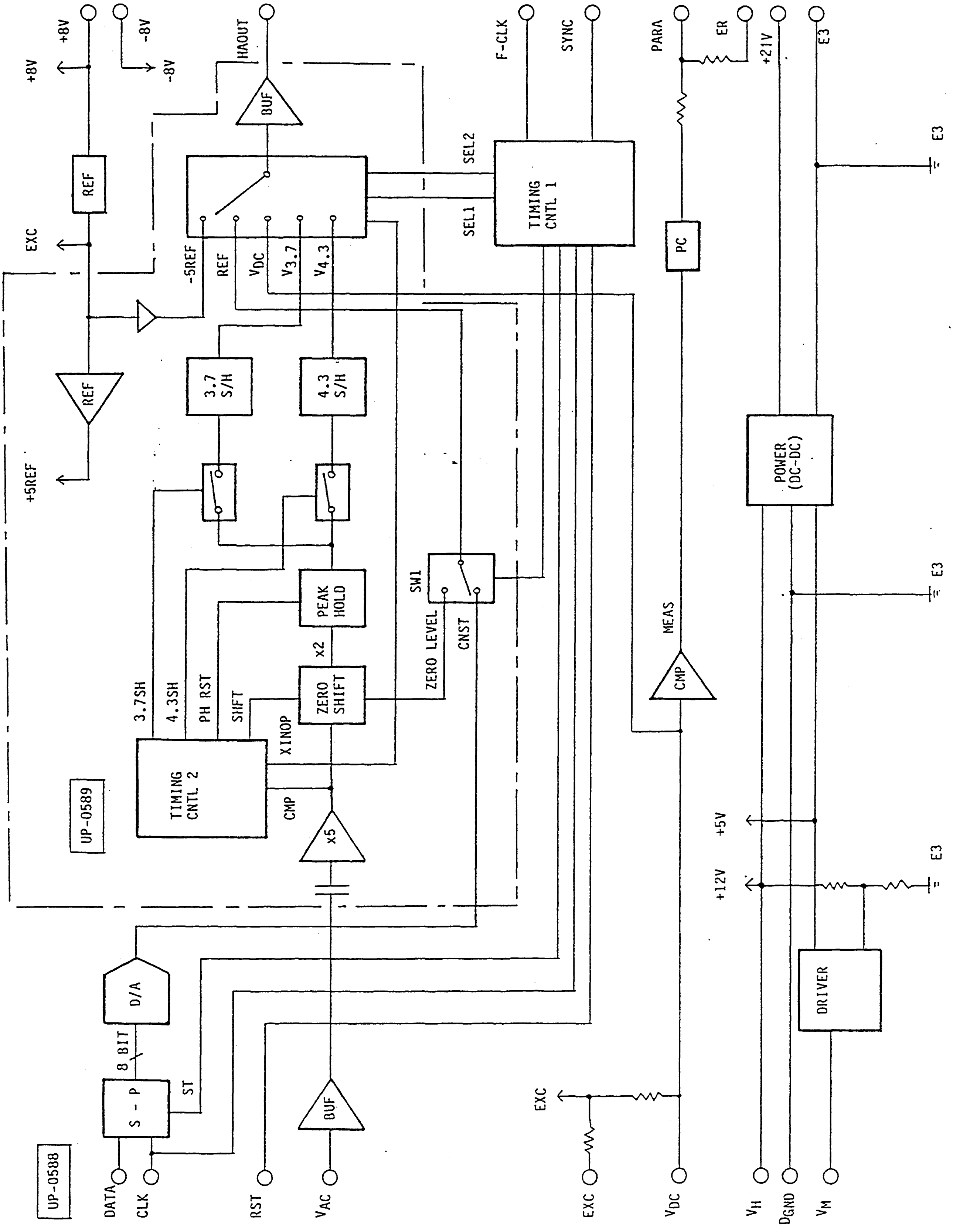
11. BLOCK DIAGRAM

EEG Head Amp, AE-800PA


FCLK (FLOATING CLOCK)
SYNC
OUT
16 μsec
EEG 1 2 1 2
HAOUT
SYNC
PARA
ER
IC006 HYBRID ISOLATE
FCLK GENERATOR
X2
SW
GROUNDED AREA
PC
PC
+8V
-8V
64KHz
EF
SW
IC003A
IC003B
IC004
CNT
125Hz
IC003C
EEG1
EEG2
CMP
IC006
FLOATING AREA
RECTI-FIER
+8V
-8V
REG
HUM
35Hz
UP-0422
X500
IC051, IC053
IC052, IC054
+5F
-5F
GF
IC050A
X10
X10
IC050B
+5H
-5H
BUFFER
IC007
IC008
PRETCTOR & FILTER
G1(-)
G2(+)
G1(-)
G2(+)
N
MEAS
EEG1
EEG2

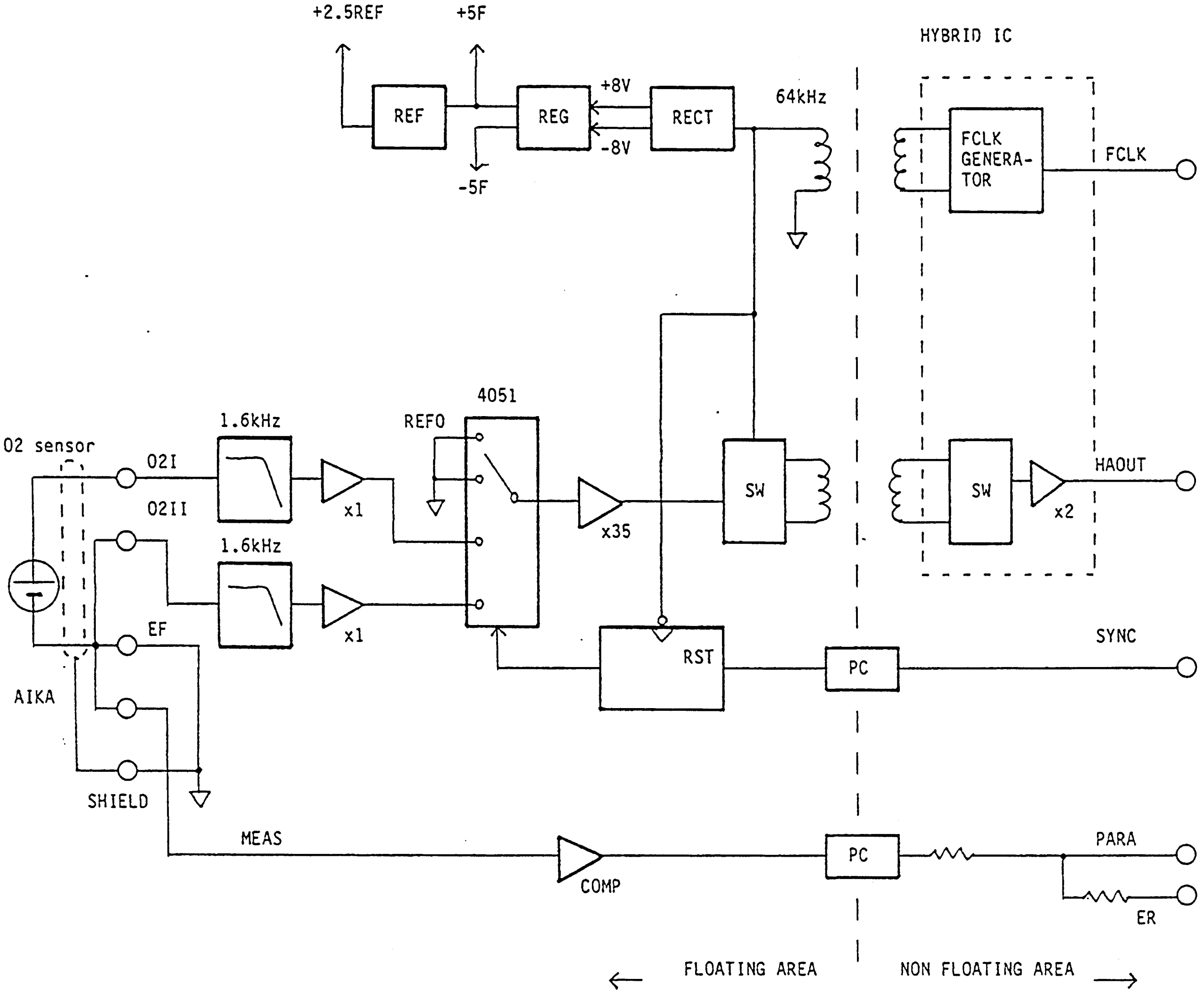
11. BLOCK DIAGRAM

CO_2 Head Amp, AG-800PA

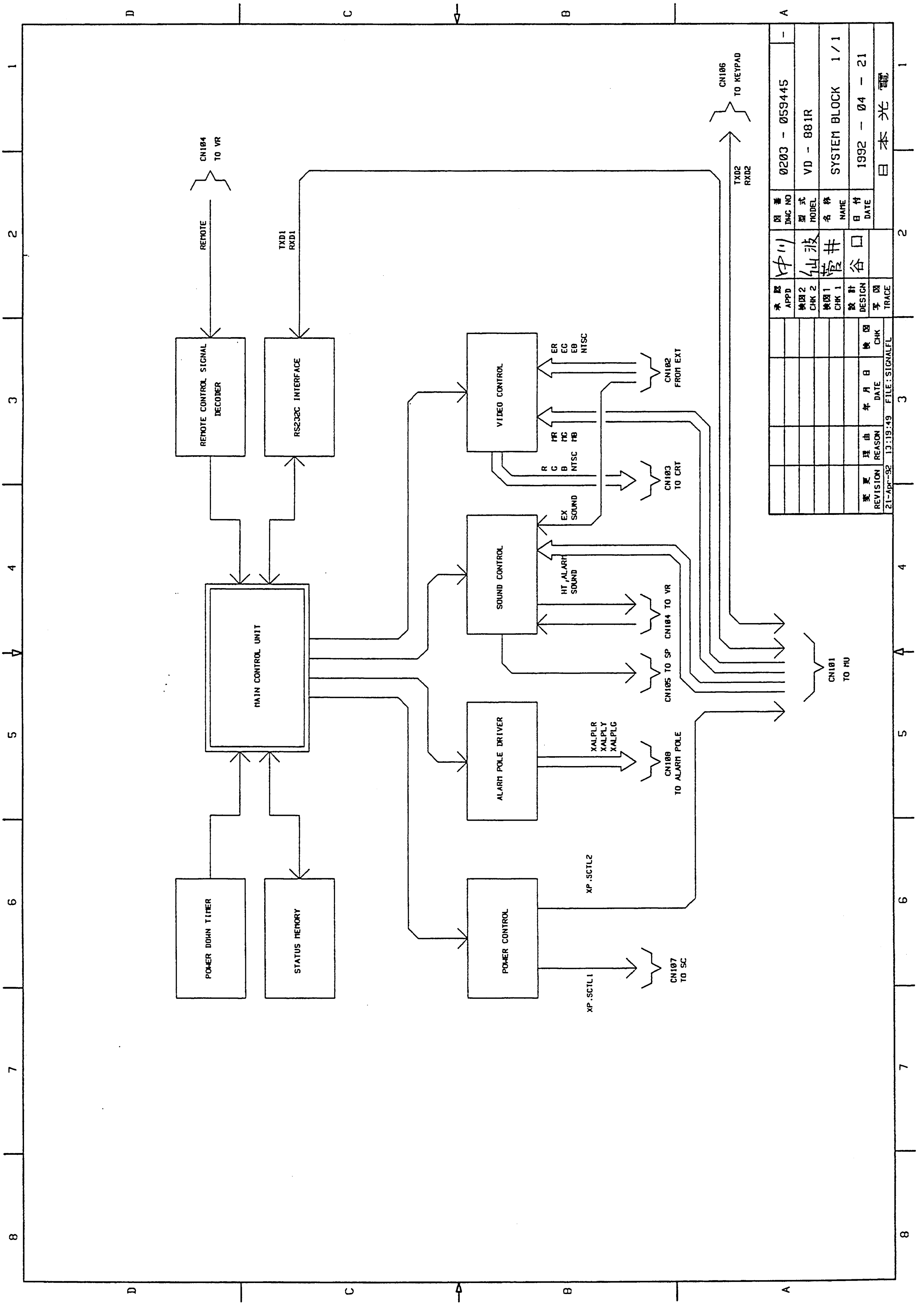

+8V
-8V
+8V
-8V
HAOUT
F-CLK
SYNC
PARA
ER
+21V
E3
BUF
REF
SEL2
SEL1
TIMING CNTL 1
E3
EXC
-5REF
REF
V_{DC}
$V_{3.7}$
$V_{4.3}$
PC
REF
3.7 S/H
4.3 S/H
POWER (DC-DC)
+5REF
SW1
E3
PEAK HOLD
ZERO LEVEL
CNST
MEAS
x2
ZERO SHIFT
CMP
3.7SH
4.3SH
PH RST
SHFT
XINOP
TIMING CNTL 2
CMP
UP-0589
x5
+5V
+12V
E3
D/A
8 BIT
DRIVER
S - P
ST
BUF
EXC
UP-0588
DATA
CLK
RST
V_{AC}
EXC
V_{DC}
V_H
D_{GND}
V_M

11. BLOCK DIAGRAM

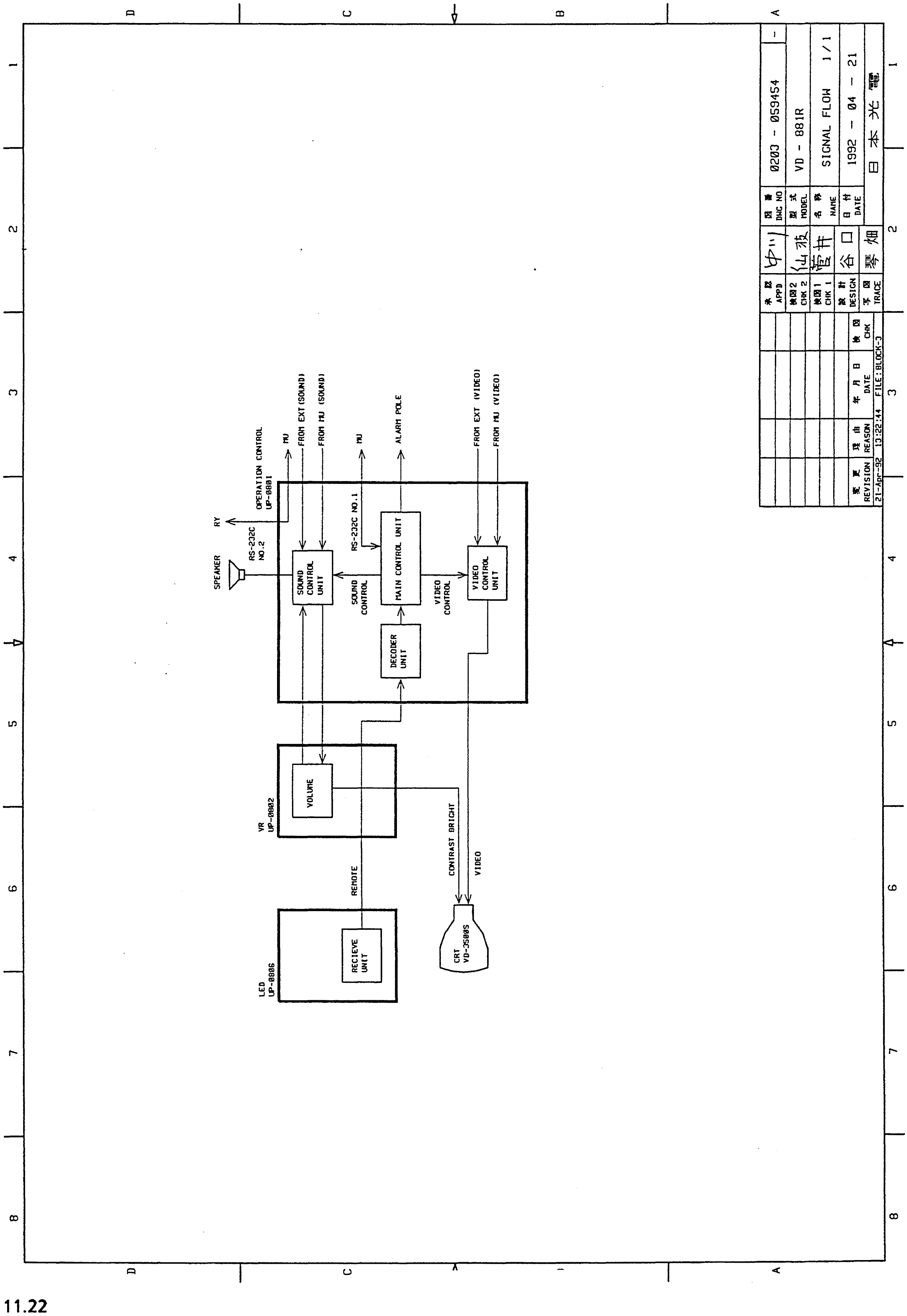
O_2 Head Amp, AG-820PA


+2.5REF
+5F
REF
REG
+8V
-8V
-5F
RECT
64kHz
HYBRID IC
FCLK GENERA-TOR
FCLK
4051
1.6kHz
REFO
O2 sensor
O2I
O2II
x1
x35
SW
SW
x2
HAOUT
1.6kHz
x1
EF
AIKA
RST
PC
SYNC
SHIELD
MEAS
COMP
PC
PARA
ER
← FLOATING AREA
NON FLOATING AREA →

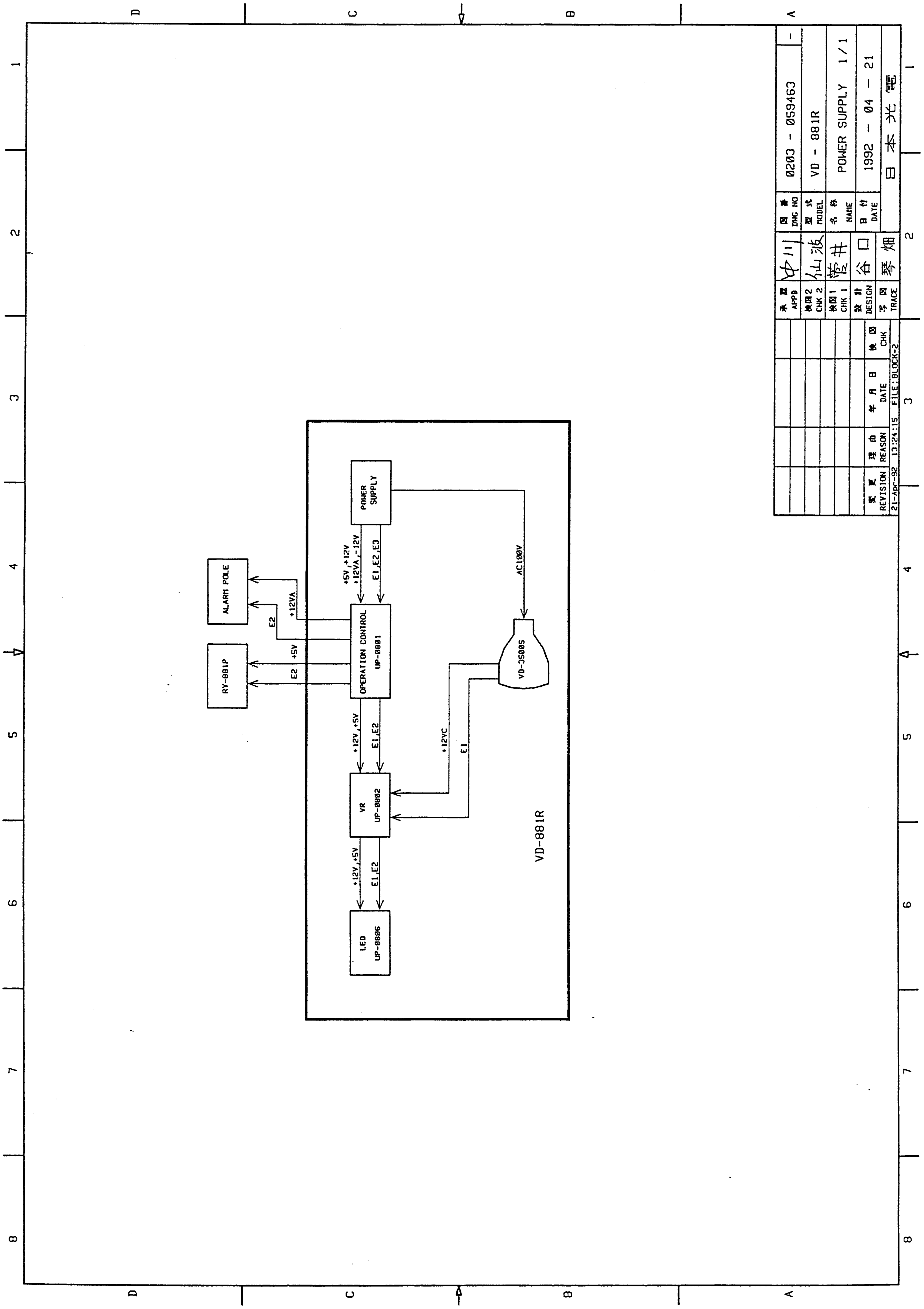
11. BLOCK DIAGRAM


REMOTE CONTROL SIGNAL DECODER
RS232C INTERFACE
MAIN CONTROL UNIT
POWER DOWN TIMER
STATUS MEMORY
VIDEO CONTROL
SOUND CONTROL
ALARM POLE DRIVER
POWER CONTROL
REMOTE
CN104 TO VR
TXD1
RXD1
TXD2
RXD2
CN106 TO KEYPAD
ER
EG
EB
NTSC
CN102 FROM EXT
MR
MG
MB
R
G
B
NTSC
CN103 TO CRT
EX SOUND
HT_ALARM SOUND
CN104 TO VR
CN105 TO SP
CN101 TO MU
XALPLR
XALPLY
XALPLG
CN108 TO ALARM POLE
XP_SCTL2
XP_SCTL1
CN107 TO SC
1
2
3
4
5
6
7
8
A
B
C
D
図番 DWG NO
0203 - 059445
-
型式 MODEL
VD - 881R
名称 NAME
SYSTEM BLOCK 1/1
日付 DATE
1992 - 04 - 21
日本光電
承認 APPD
中川
検図2 CHK 2
仙波
検図1 CHK 1
菅井
設計 DESIGN
谷口
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
21-Apr-92 13:19:49 FILE:SIGNALFL

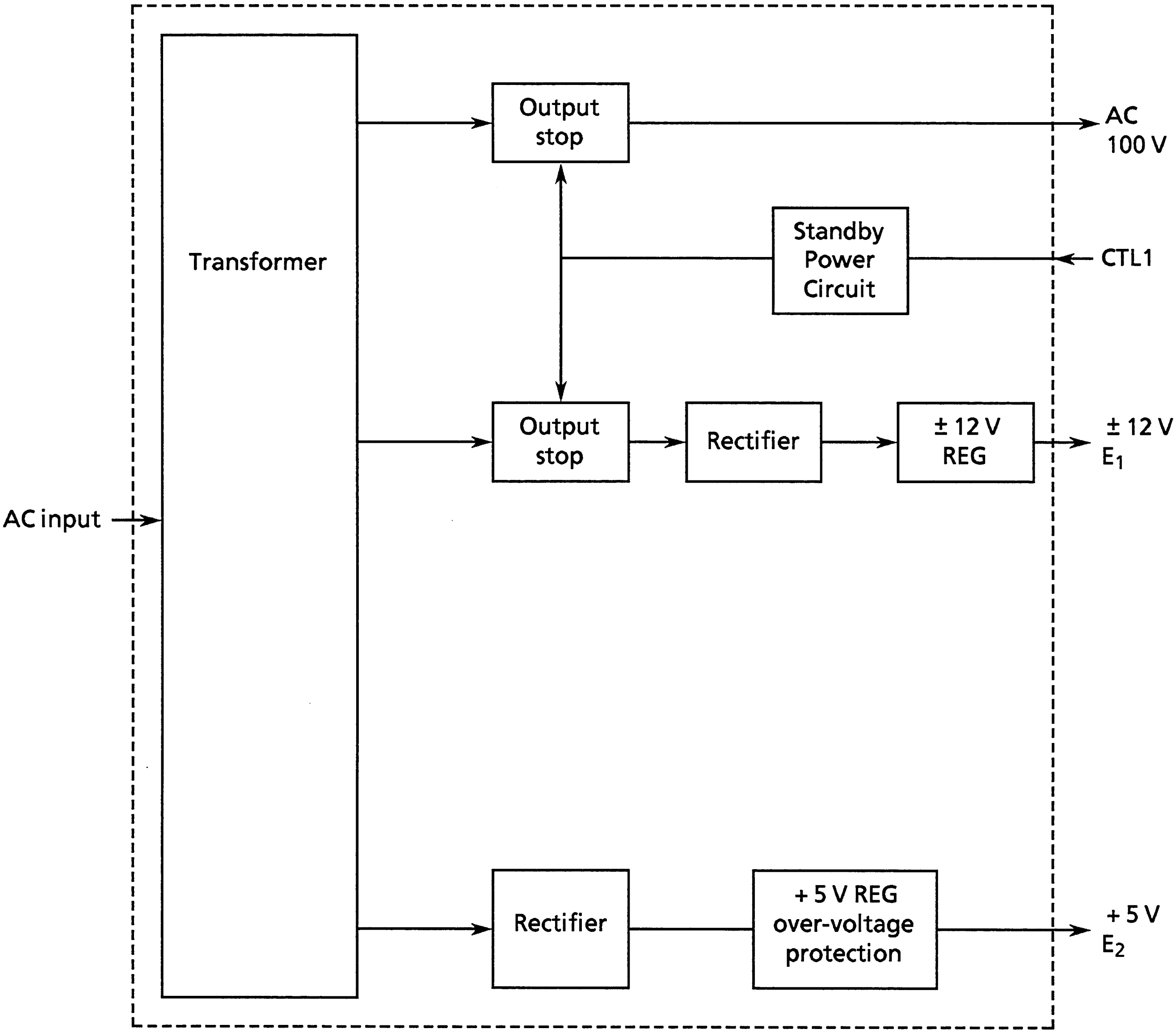
11. BLOCK DIAGRAM


OPERATION CONTROL
UP-0801
MU
FROM EXT (SOUND)
FROM MU (SOUND)
MU
ALARM POLE
FROM EXT (VIDEO)
FROM MU (VIDEO)
RY
RS-232C NO.2
RS-232C NO.1
SPEAKER
SOUND CONTROL UNIT
SOUND CONTROL
MAIN CONTROL UNIT
VIDEO CONTROL
VIDEO CONTROL UNIT
DECODER UNIT
VR
UP-0802
VOLUME
REMOTE
CONTRAST BRIGHT
VIDEO
LED
UP-0806
RECIEVE UNIT
CRT
VD-3500S
図番 DWG NO
0203 - 059454
型式 MODEL
VD - 881R
名称 NAME
SIGNAL FLOW 1/1
日付 DATE
1992 - 04 - 21
日本光電
承認 APPD
中川
検図2 CHK 2
仙波
検図1 CHK 1
藤井
設計 DESIGN
谷口
写図 TRACE
琴畑
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
21-Apr-92 13:22:44 FILE: BLOCK-3
A
B
C
D
1
2
3
4
5
6
7
8

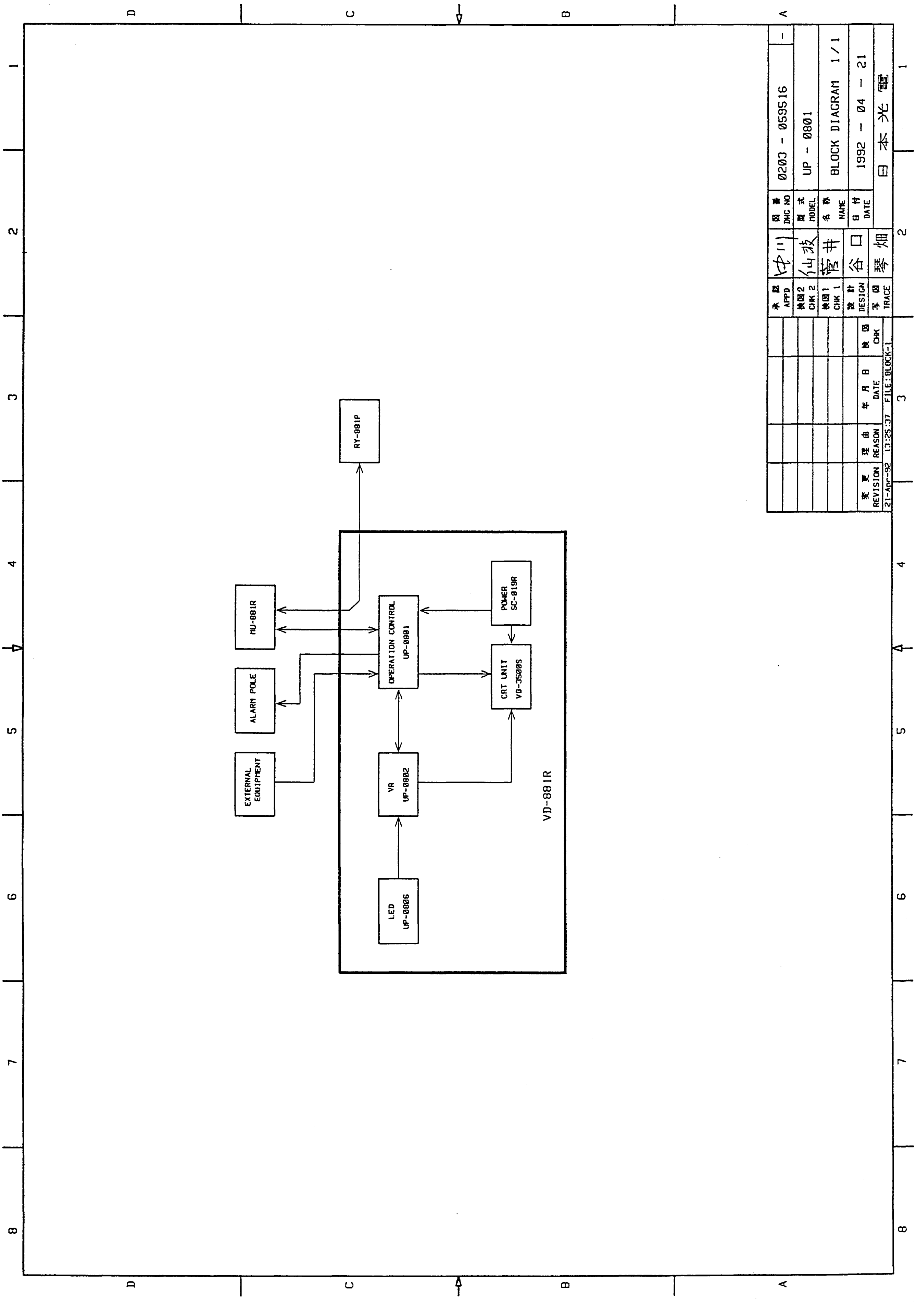
11. BLOCK DIAGRAM


POWER SUPPLY
+5V,+12V
+12VA,-12V
E1,E2,E3
AC100V
OPERATION CONTROL
UP-0801
ALARM POLE
+12VA
E2
RY-881P
+5V
E2
VD-3500S
+12V,+5V
E1,E2
+12VC
E1
VR
UP-0802
+12V,+5V
E1,E2
LED
UP-0806
VD-881R
図番 DWG NO
0203 - 059463
型式 MODEL
VD - 881R
名称 NAME
POWER SUPPLY 1/1
日付 DATE
1992 - 04 - 21
日本光電
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
21-Apr-92 13:24:15 FILE:BLOCK-2
A
B
C
D
1
2
3
4
5
6
7
8

Power Supply Unit, SC-019R

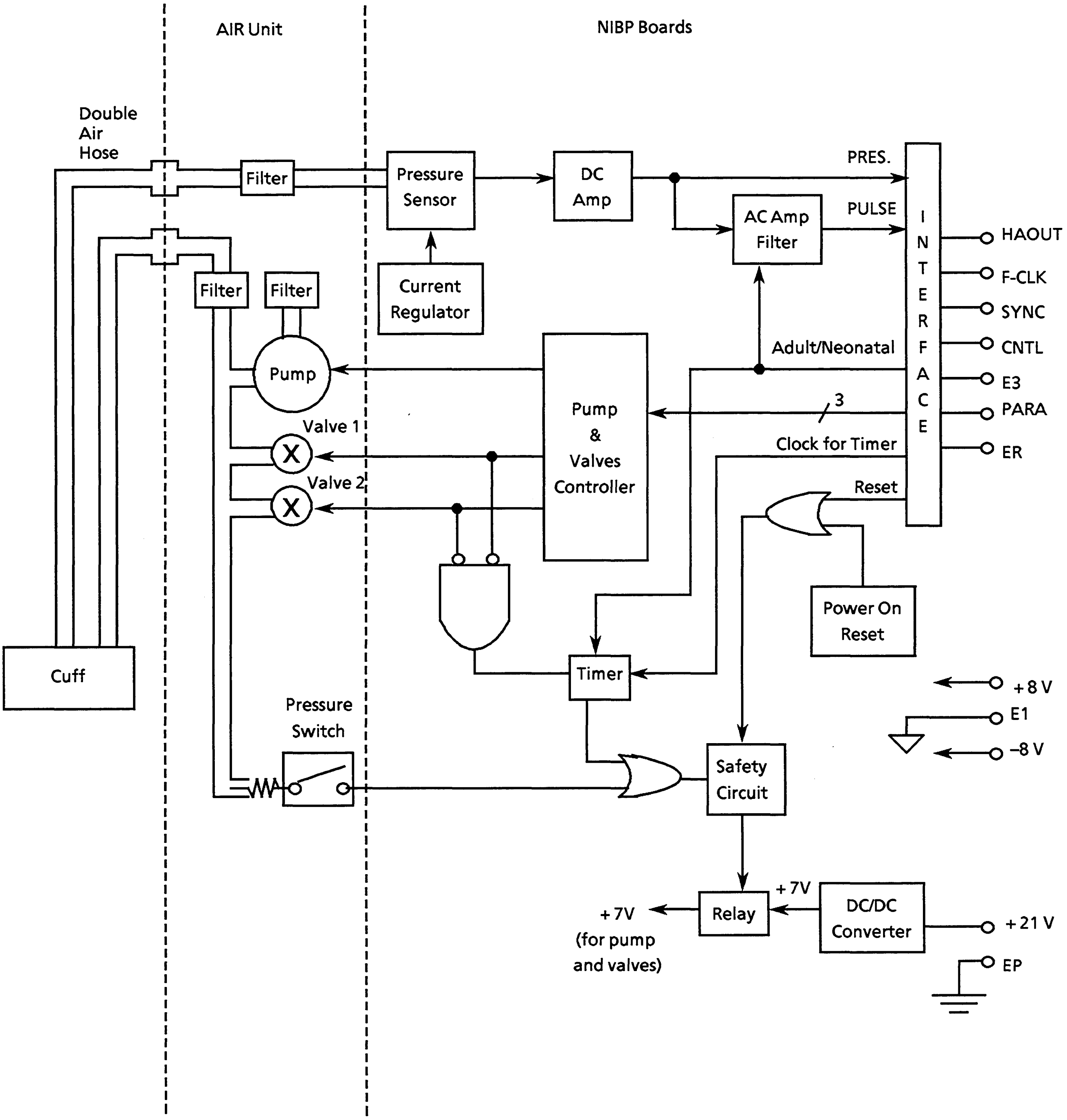

Transformer
Output stop
AC 100 V
Standby Power Circuit
CTL1
Output stop
Rectifier
± 12 V REG
± 12 V E1
AC input
Rectifier
+ 5 V REG over-voltage protection
+ 5 V E2

11. BLOCK DIAGRAM


RY-881P
MU-881R
ALARM POLE
EXTERNAL EQUIPMENT
OPERATION CONTROL UP-0801
POWER SC-019R
CRT UNIT VD-3500S
VR UP-0802
LED UP-0806
VD-881R
図番 DWG NO 0203 - 059516 -
型式 MODEL UP - 0801
名称 NAME BLOCK DIAGRAM 1/1
日付 DATE 1992 - 04 - 21
日本光電
承認 APPD 中川
検図2 CHK 2 仙波
検図1 CHK 1 菅井
設計 DESIGN 谷口
写図 TRACE 琴畑
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
21-Apr-92 13:25:37 FILE:BLOCK-1

11. BLOCK DIAGRAM

NIBP Head Amp, AP-860PA


AIR Unit
NIBP Boards
Double Air Hose
Filter
Pressure Sensor
DC Amp
PRES.
AC Amp Filter
PULSE
INTERFACE
HAOUT
F-CLK
SYNC
CNTL
E3
PARA
ER
Current Regulator
Filter
Filter
Pump
Adult/Neonatal
Pump & Valves Controller
3
Clock for Timer
Valve 1
Valve 2
Reset
Power On Reset
Cuff
Timer
+8 V
E1
-8 V
Pressure Switch
Safety Circuit
+7V
Relay
DC/DC Converter
+21 V
EP
+7V (for pump and valves)

Section 12 CIRCUIT DIAGRAM

12-1 BSM-8800 Connection Diagram 12.1
12-2 VD-881R Connection Diagram 12.2

12-3 Main Unit, MU-881R

12-3-1 MOTHER Board, UP-0798 .... 12.3
12-3-2 COM3 Board, UP-0563 .... 12.5
12-3-3 CRTC Board, UP-0795 .... 12.15
12-3-4 I/O Board, UP-0797 .... 12.35
12-3-5 MEMORY CARD Board, UP-0799 .... 12.41
12-3-6 CONNECTOR Board, UP-0807 .... 12.42
12-3-7 DPU Board, UP-0670 .... 12.43
12-3-8 CPU Board, UR-3023 .... 12.62
12-3-9 Transformer Unit, SC-018RA 12.77
12-3-10 Transformer Unit, SC-018RJ 12.79
12-3-11 Transformer Unit, SC-018RK 12.80
12-3-12 Regulator Unit (Board), UP-0813 .... 12.81

12-4 Keypad, RY-881PA

12-4-1 OPERATION Board, UR-3025 .... 12.83

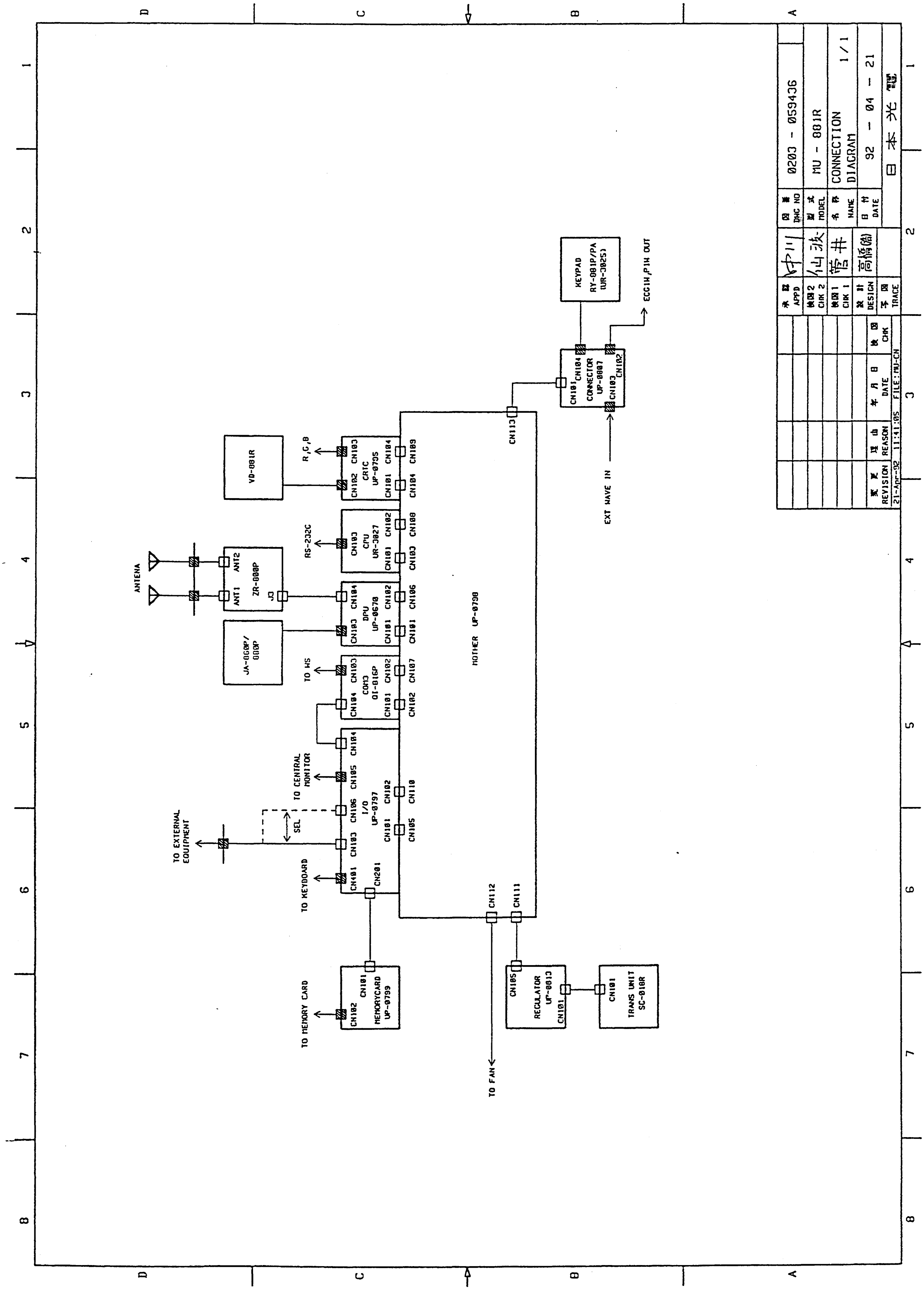
12-5 Head Amplifiers

12-5-1 ECG Head Amp (AC-800P) Board, UP-0272 .... 12.84
12-5-2 PRESS Head Amp (AP-800PA) Board, UP-0369 .... 12.85
12-5-3 CO Head Amp (AH-800PA) Board, UP-0318 .... 12.86
12-5-4 TEMP Head Amp (AW-800PA) Board, UP-0319 .... 12.87
12-5-5 RESPIRATION Head Amp (AR-800PA) Board, UP0548 .... 12.88
12-5-6 SpO_2 Head Amp (AL-800PA) Main Board, UP-0551 .... 12.89
12-5-7 SpO_2 Head Amp (AL-800PA) Sub Board, UP-0552 .... 12.90
12-5-8 EEG Head Amp (AE-800PA) Main Board, UP-0421 .... 12.91
12-5-9 EEG Head Amp (AE-800PA) Sub Board, UP-0422 .... 12.92
12-5-10 CO_2 Head Amp (AG-800PA) Main Board, UP-0588 .... 12.93
12-5-11 CO_2 Head Amp (AG-800PA) Sub Board, UP0589 .... 12.94
12-5-12 CO_2 Sensor Board, TG-706P 12.95
12-5-13 O_2 Head Amp (AG-820PA) Board, UP-0592 .... 12.96
12-5-14 NIBP Head Amp (AP-860PA) Main Board, UP-0629 .... 12.106
12-5-15 NIBP Head Amp (AP-860PA) Sub Board, UP-0630 .... 12.108

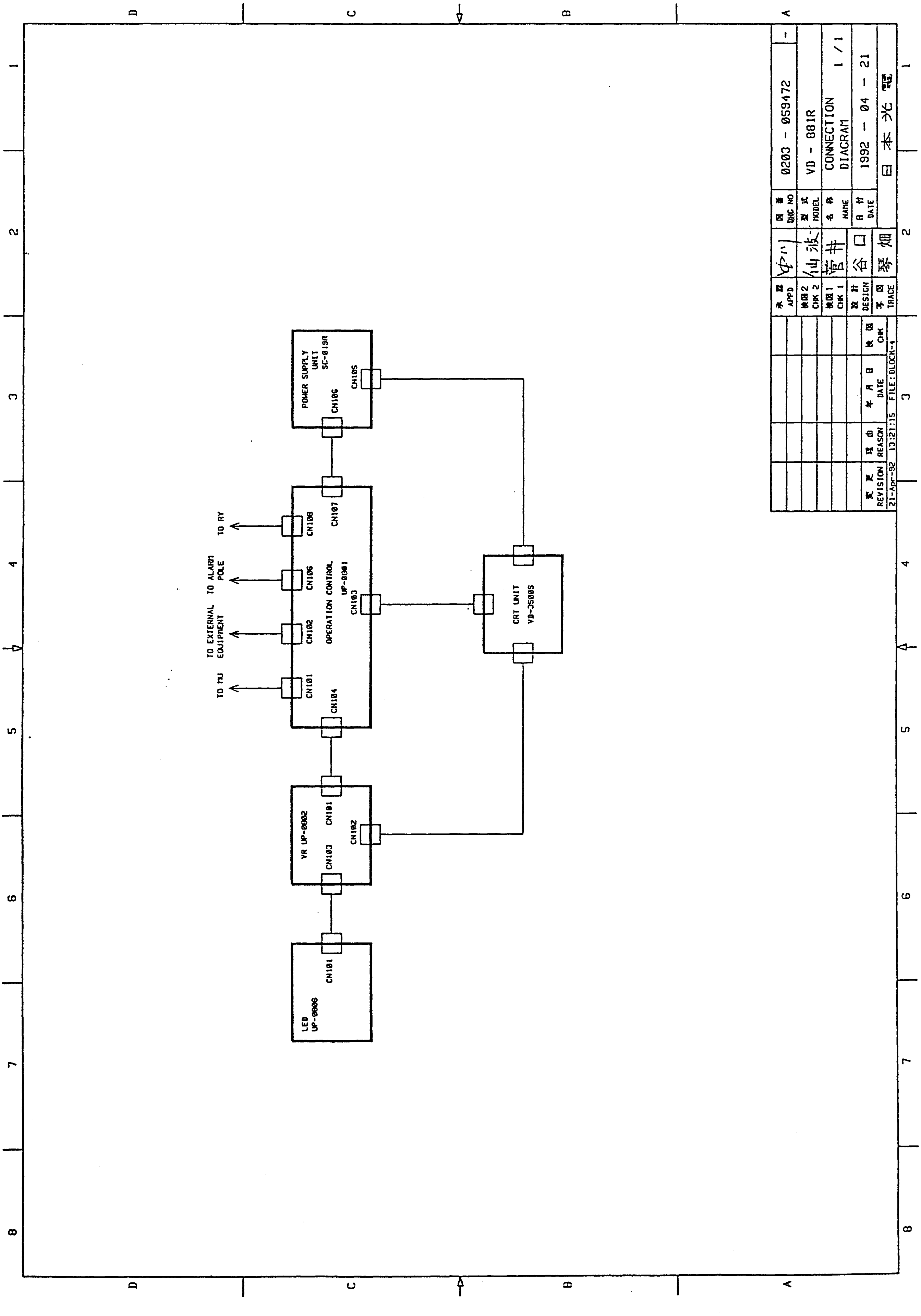
12-6 Display Unit, VD-881R

12-6-1 OPERATION CONTROL Board, UP-0801 .... 12.97
12-6-2 OPERATION (VR) Board, UP-0802 .... 12.101
12-6-3 LED Board, UP-0806 .... 12.102
12-6-4 Power Supply Unit, SC-019RJ 12.104
12-6-5 Power Supply Unit, SC-019RK 12.105

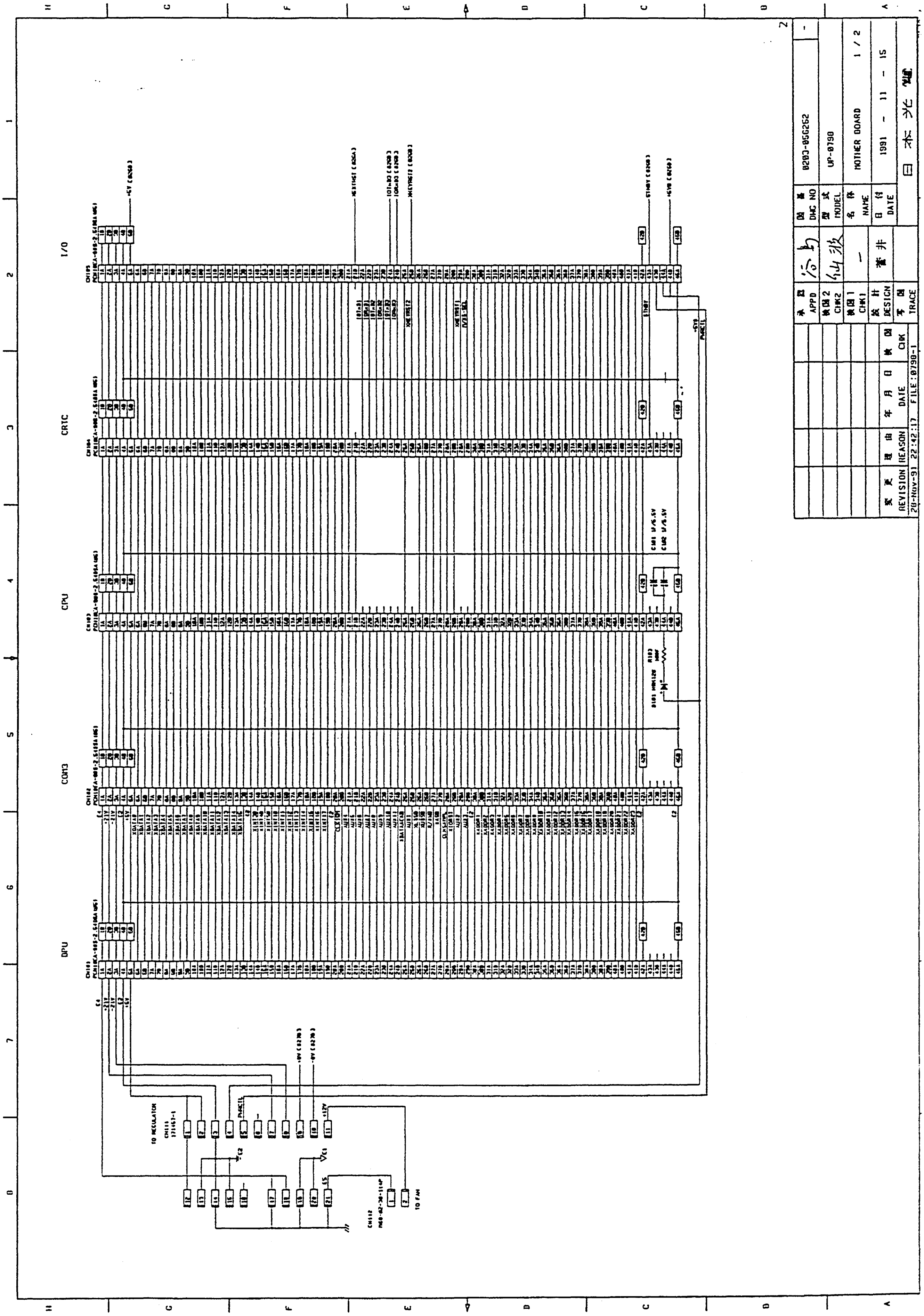
12. CIRCUIT DIAGRAM


0203 - 059436
MU - 801R
CONNECTION DIAGRAM
1/1
92 - 04 - 21
日本光電
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
21-Apr-92 11:41:05 FILE:MU-CN
KEYPAD
RY-081P/PA
(UR-3025)
ECG1H,P1H OUT
CN101
CN104
CONNECTOR
UP-0807
CN103
CN102
EXT WAVE IN
CN113
MOTHER UP-0798
CN103
CRTC
UP-0795
CN102
CN101
CN104
CN104
CN109
R,G,B
VD-081R
CN103
CPU
UR-3027
CN101
CN102
CN103
CN108
RS-232C
ANTENA
ANT1
ANT2
ZR-080P
J3
CN104
DPU
UP-0670
CN103
CN101
CN102
CN101
CN106
JA-060P/
080P
CN103
COMM
OI-016P
CN104
CN101
CN102
CN102
CN107
TO HS
CN104
CN105
CN106
I/O
UP-0797
CN103
CN101
CN102
CN105
CN110
CN401
CN201
TO CENTRAL MONITOR
SEL
TO EXTERNAL EQUIPMENT
TO KEYBOARD
CN101
CN102
MEMORYCARD
UP-0799
TO MEMORY CARD
CN112
CN111
TO FAN
CN105
REGULATOR
UP-0813
CN101
CN101
TRANS UNIT
SC-010R
A
B
C
D
1
2
3
4
5
6
7
8

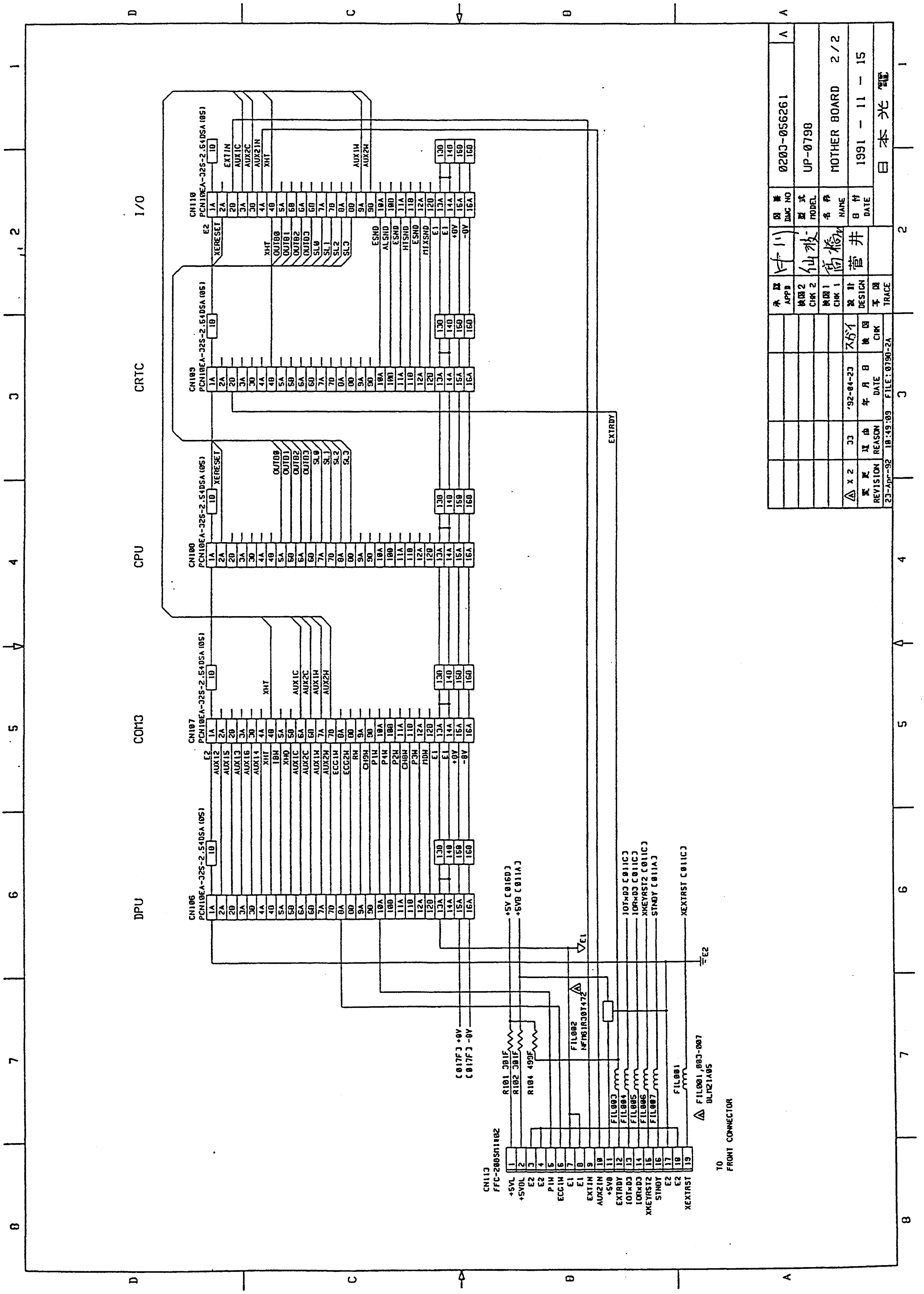
12. CIRCUIT DIAGRAM


POWER SUPPLY UNIT SC-019R
CN105
CN106
OPERATION CONTROL UP-0081
CN107
CN108
CN106
CN102
CN101
CN103
CN104
TO RY
TO ALARM POLE
TO EXTERNAL EQUIPMENT
TO MJ
CRT UNIT VD-J508S
VR UP-0082
CN101
CN102
CN103
LED UP-0006
CN101
0203 - 059472
-
VD - 881R
CONNECTION DIAGRAM
1 / 1
1992 - 04 - 21
日本光電
図番 DWG NO
型式 MODEL
名称 NAME
日付 DATE
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
仙波
菅井
谷口
琴畑
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
21-Apr-92 13:21:15 FILE: BLOCK-4
A
B
C
D
1
2
3
4
5
6
7
8

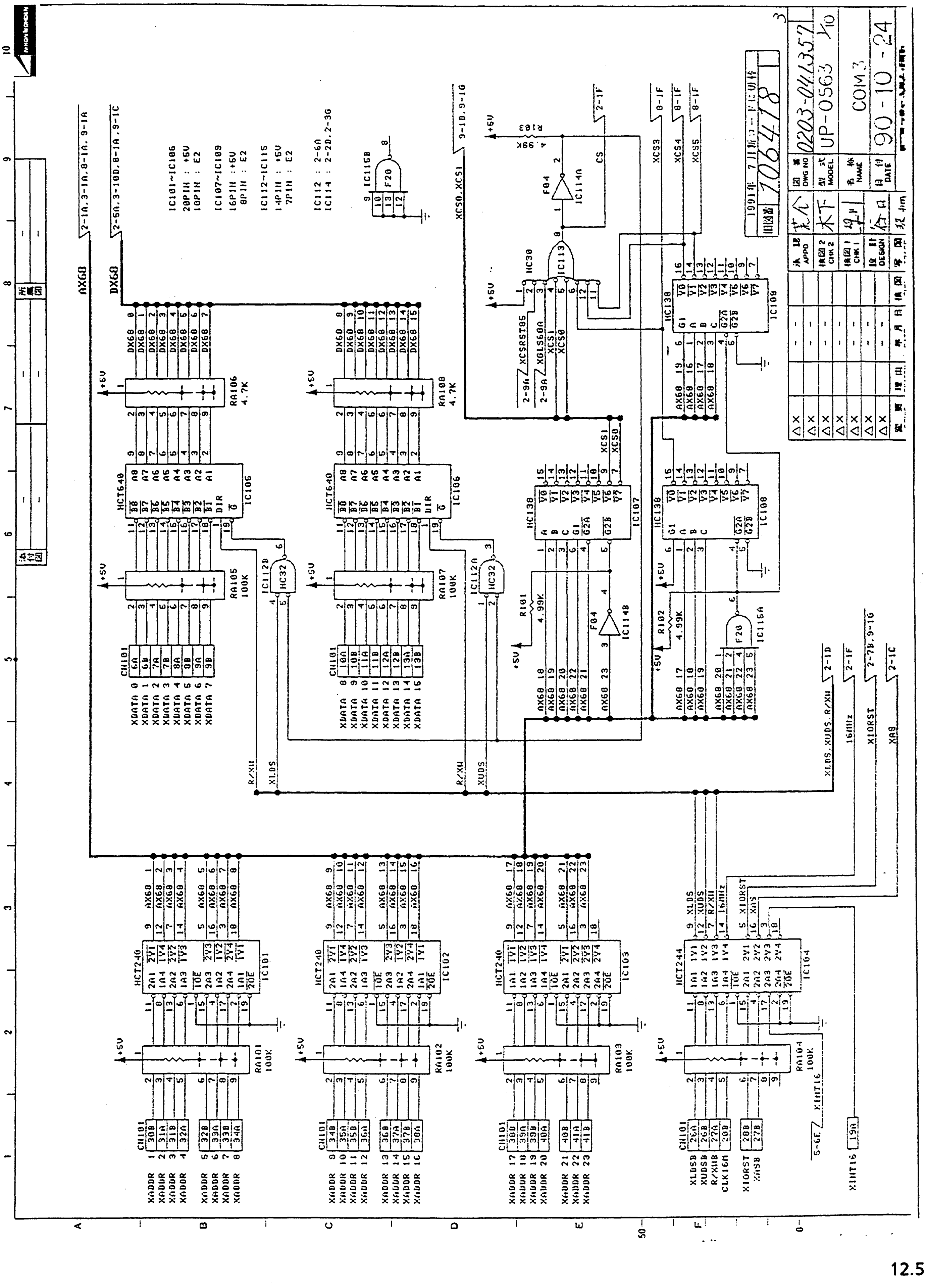
12. CIRCUIT DIAGRAM


I/O
CRTC
CPU
COM3
DPU
TO REGULATOR
TO FAN
图番 DWG NO 0203-056262
型式 MODEL UP-0790
名称 NAME MOTHER BOARD 1 / 2
日付 DATE 1991 - 11 - 15
日本光電
承認 APPD
検図2 CHK2
検図1 CHK1
設計 DESIGN
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
20-Nov-91 22:42:17 FILE:0790-1

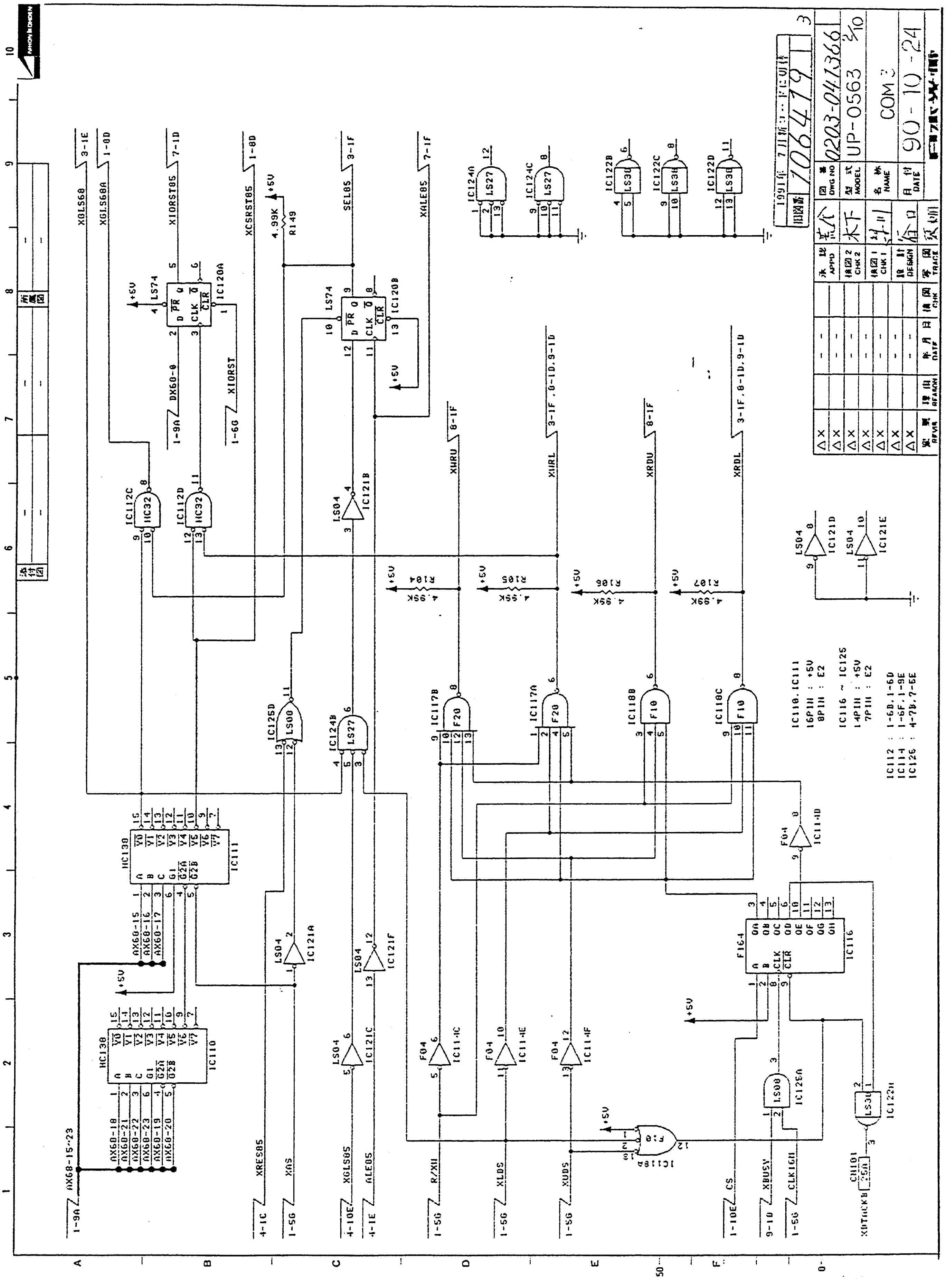
12. CIRCUIT DIAGRAM

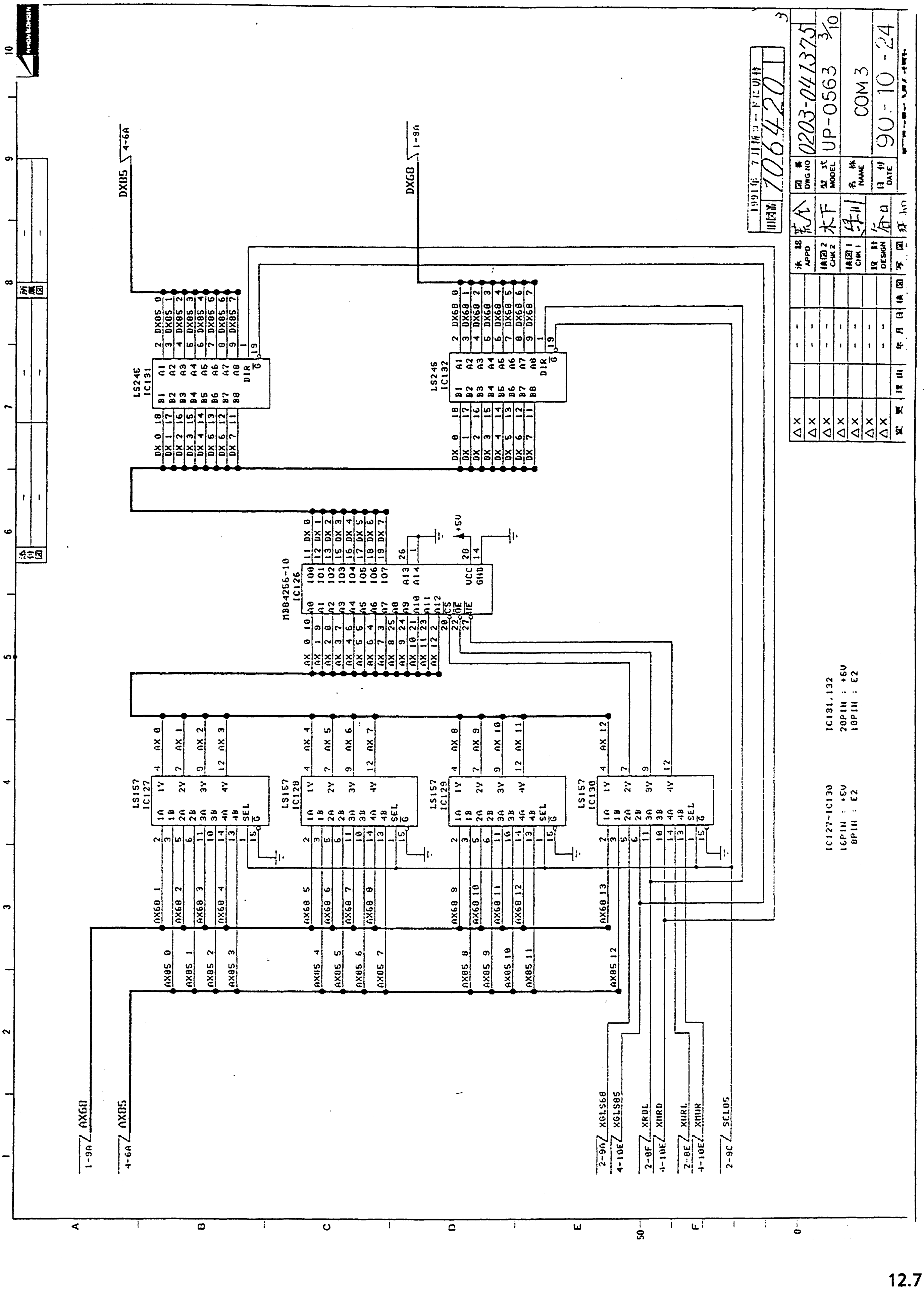


DPU
COM3
CPU
CRTC
I/O
CN106
CN107
CN108
CN109
CN110
PCN10EA-32S-2.54DSA(05)
XERESET
EXTRDY
CN113
FFC-20BSN1002
TO FRONT CONNECTOR
FIL001
FIL002
R101 301F
R102 301F
R104 499F
+5V
+5VD
E1
E2
0203-056261
UP-0798
MOTHER BOARD 2/2
1991 - 11 - 15
日本光電
'92-04-23
FILE:0790-2A

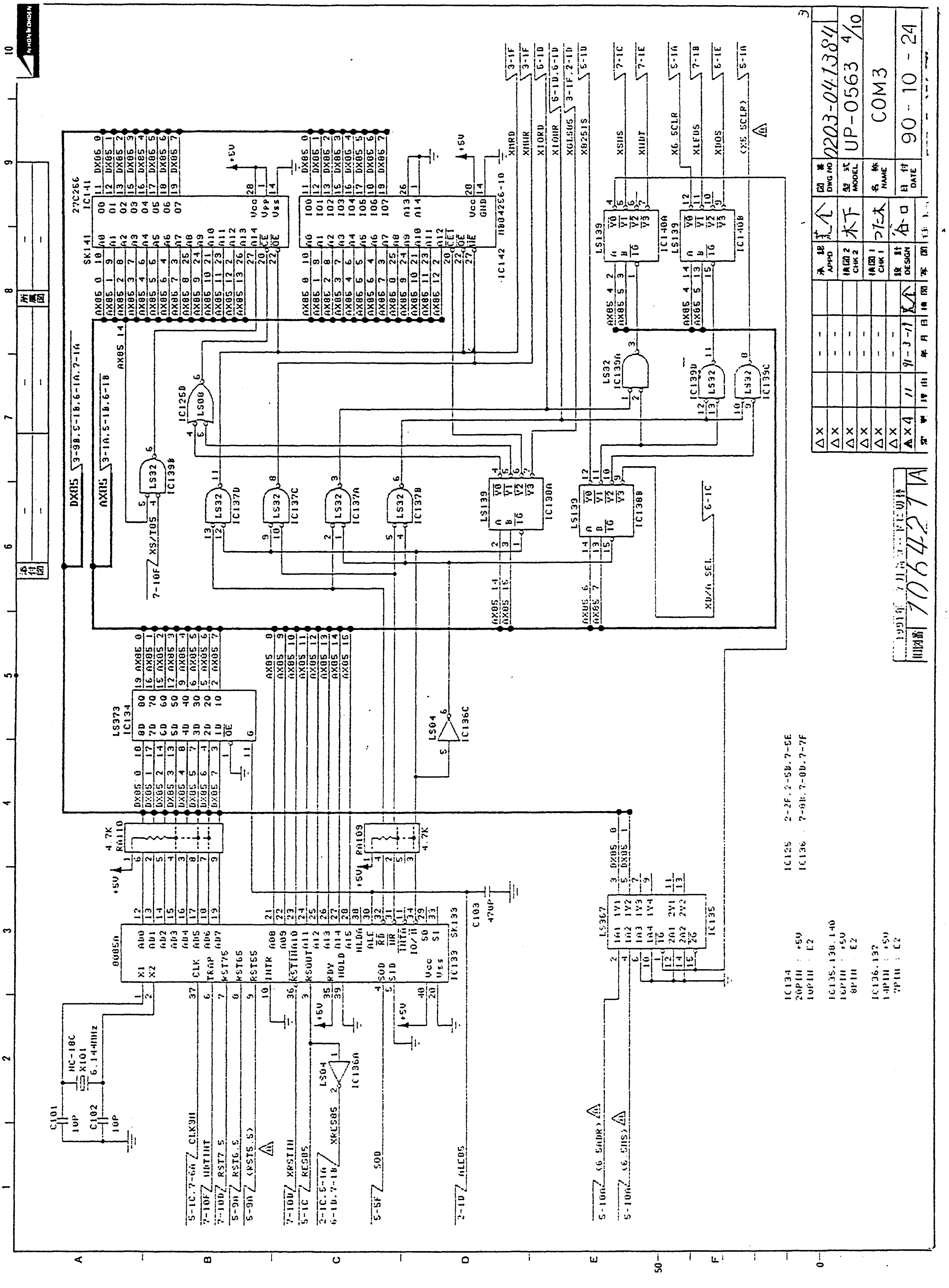

0203-044357
UP-0563
COM3
90-10-24
706478
HCT240
IC101
IC102
IC103
HCT244
IC104
HCT640
IC105
IC106
HC138
IC107
IC108
IC109
HC32
IC112A
IC112B
HC30
IC113
F04
IC114A
IC114B
F20
IC115A
IC115B
RA101 100K
RA102 100K
RA103 100K
RA104 100K
RA105 100K
RA106 4.7K
RA107 100K
RA108 4.7K
R101 4.99K
R102 4.99K
R103 4.99K
CN101
AX68
DX68
XDATA
XADDR
XLDS
XUDS
R/XW
XCS0
XCS1
XCS3
XCS4
XCS5
CS
XCSRST85
XGLS60A
XIORST
16MHz
XAS
XINT16
+5V
IC101~IC106
20PIN : +5V
10PIN : E2
IC107~IC109
16PIN : +5V
8PIN : E2
IC112~IC115
14PIN : +5V
7PIN : E2
IC112 : 2-6A
IC114 : 2-2D.2-3G

12. CIRCUIT DIAGRAM

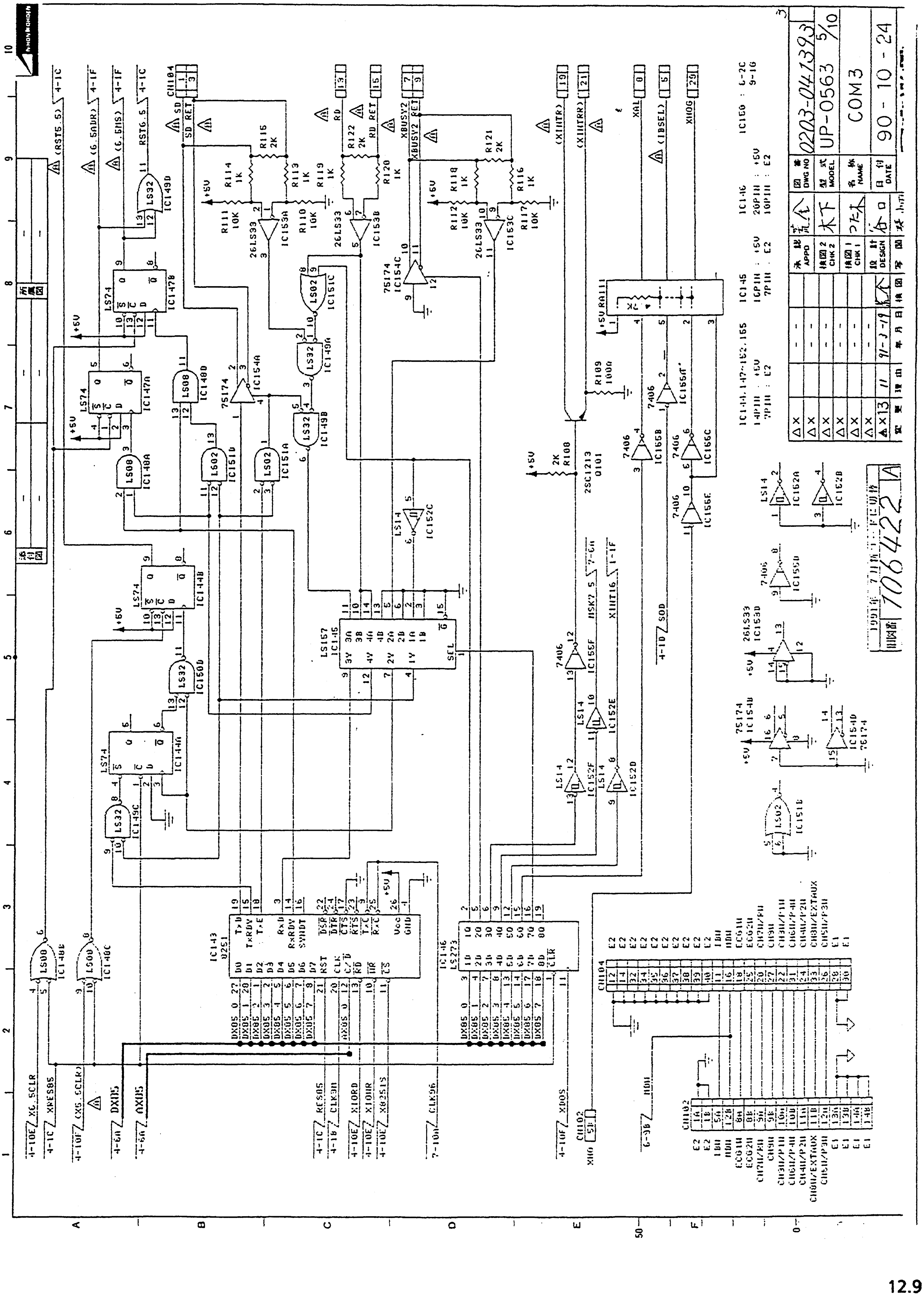

HC138
IC110
IC111
LS74
IC120A
IC120B
HC32
IC112C
IC112D
LS00
IC125D
IC125A
LS27
IC124A
IC124B
IC124C
F20
IC117A
IC117B
F10
IC118A
IC118B
IC118C
F164
IC116
LS04
IC121A
IC121B
IC121C
IC121D
IC121E
IC121F
F04
IC114C
IC114D
IC114E
IC114F
LS30
IC122B
IC122C
IC122D
IC122H
XOLS68
XGLS68A
XIORST05
XCSRST05
SEL05
XALE05
XWRU
XWRL
XRDU
XRDL
XRESOS
XAS
XGLS05
ALE05
R/XW
XLDS
XUDS
CS
XBUSY
CLK16M
DX60-0
XIORST
AX60-15
AX60-16
AX60-17
AX60-18
AX60-19
AX60-20
AX60-21
AX60-22
AX60-23
AX68-15~23
R104
R105
R106
R107
R149
4.99K
+5V
CH101
XDTACKB
IC110, IC111 16PIN : +5V 8PIN : E2
IC116 ~ IC125 14PIN : +5V 7PIN : E2
IC112 : 1-6D, 1-6D
IC114 : 1-6F, 1-9E
IC126 : 4-7B, 7-6E
0203-041366
UP-0563
2/10
COM3
90-10-24
1064179
A
B
C
D
E
F
1
2
3
4
5
6
7
8
9
10


LS245
IC131
LS245
IC132
MB84256-10
IC126
LS157
IC127
LS157
IC128
LS157
IC129
LS157
IC130
DX85
4-6A
DX68
1-9A
AX68
1-9A
AX85
4-6A
2-9A XGLS68
4-10E XGLS85
2-8F XRDL
4-10E XHRD
2-8E XURL
4-10E XHUR
2-9C SEL85
+5V
IC127~IC130
16PIN : +5V
8PIN : E2
IC131,132
20PIN : +5V
10PIN : E2
0203-041375
UP-0563
3/10
COM3
90-10-24
7064201
NIHON KOHDEN

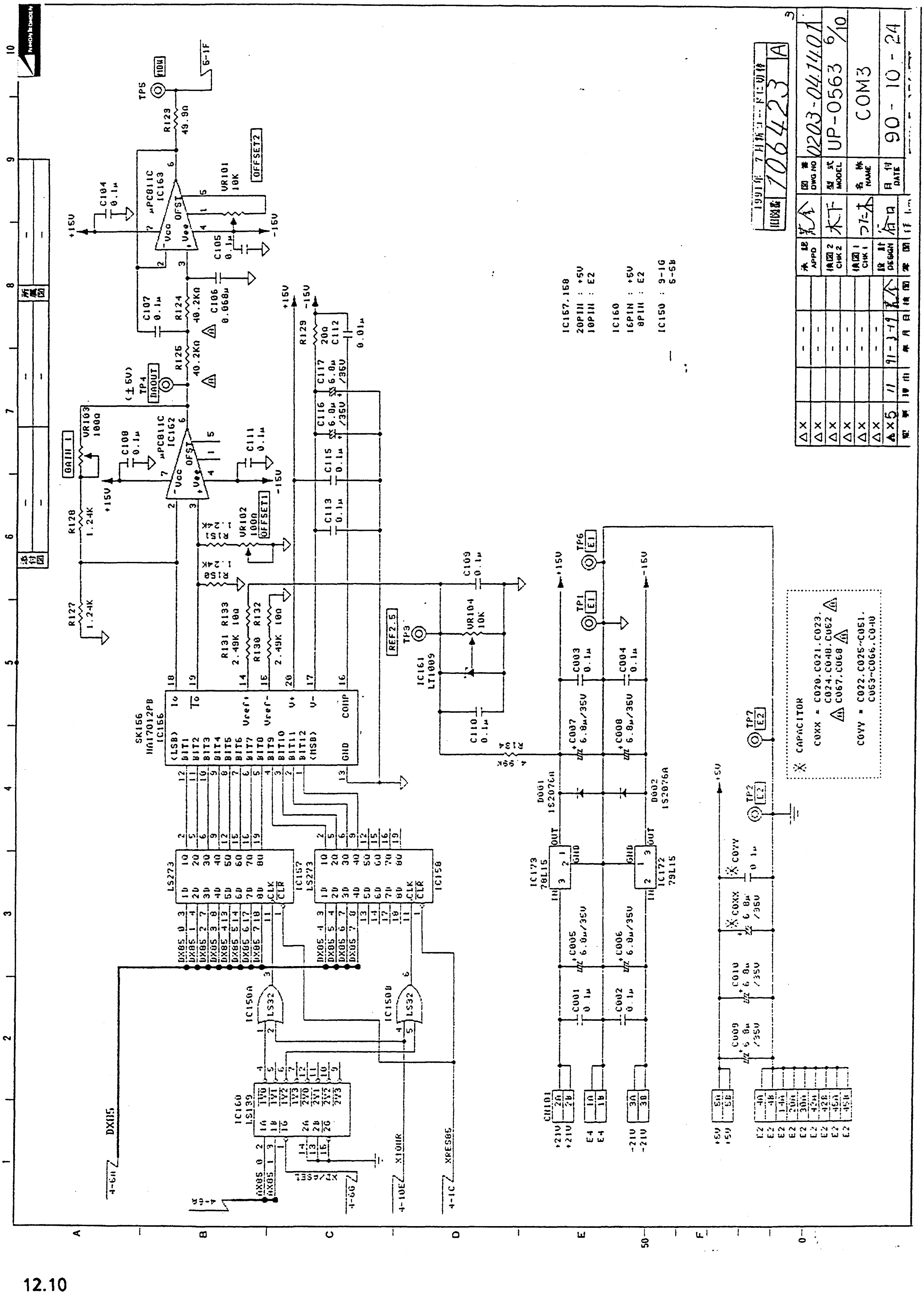
12. CIRCUIT DIAGRAM

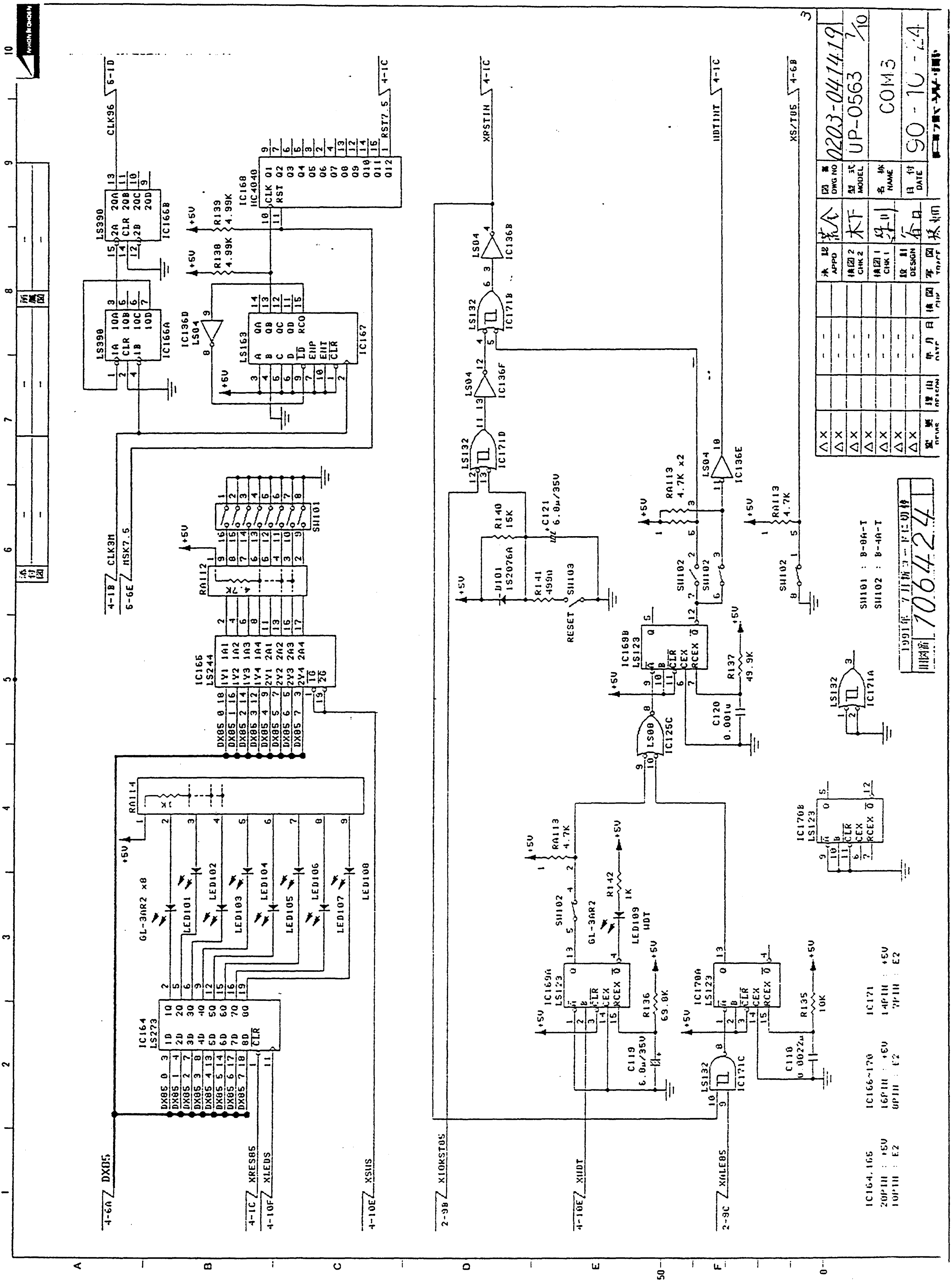


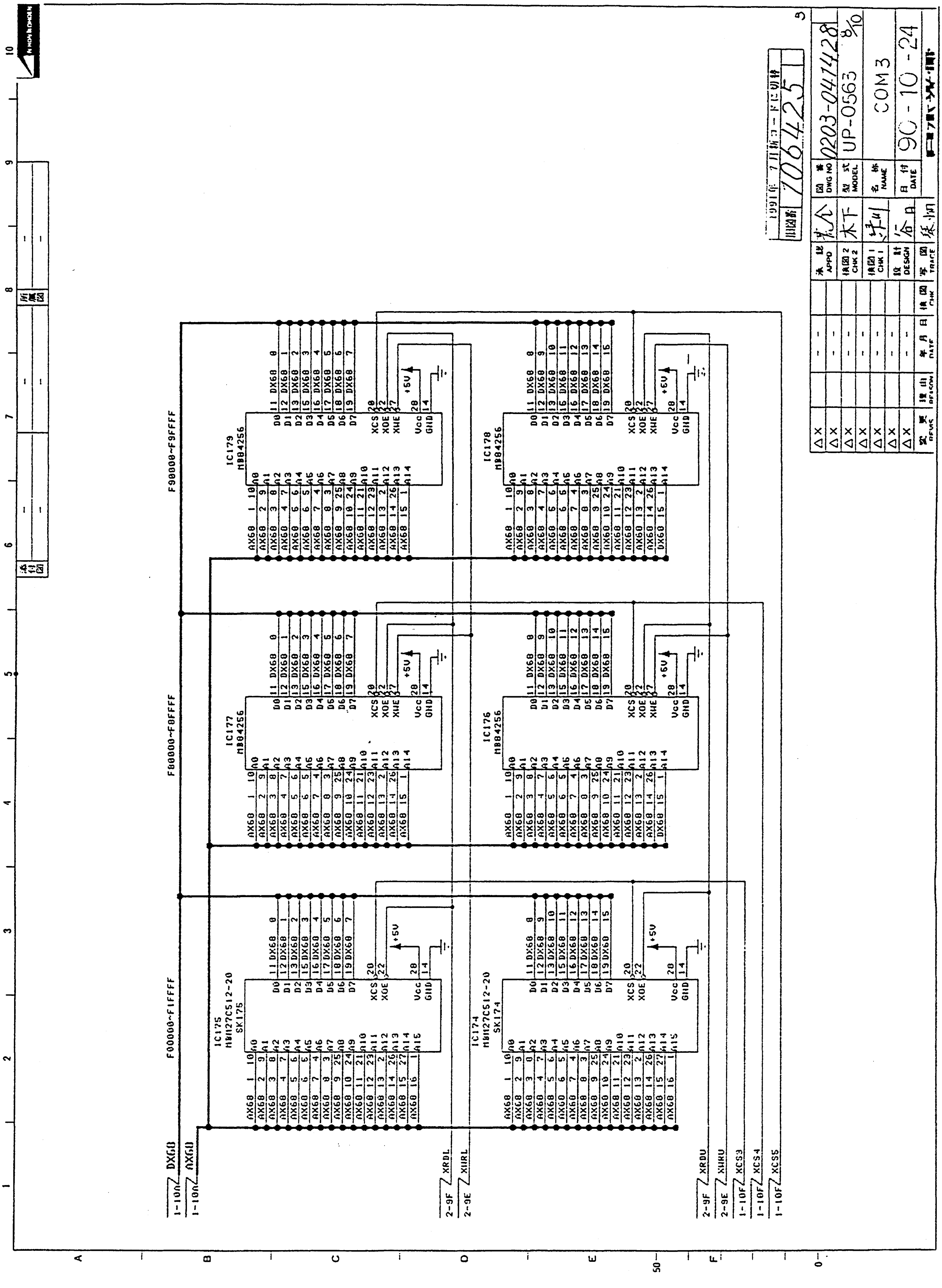
8085A
IC133
X101 6.144MHz HC-18C
C101 10P
C102 10P
C103 470P
RA110 4.7K
RA109 4.7K
LS373 IC134
LS367 IC135
27C256 IC141
SK141
HB8425G-10 IC142
LS139 IC138A
LS139 IC138B
LS139 IC140A
LS139 IC140B
LS32 IC137A
LS32 IC137B
LS32 IC137C
LS32 IC137D
LS32 IC139A
LS32 IC139B
LS32 IC139C
LS32 IC139D
LS00 IC125D
LS04 IC136A
LS04 IC136C
DX85
AX85
XS/TO5
XU/A SEL
0203-041384 4/10
UP-0563
COM3
90-10-24
706427A

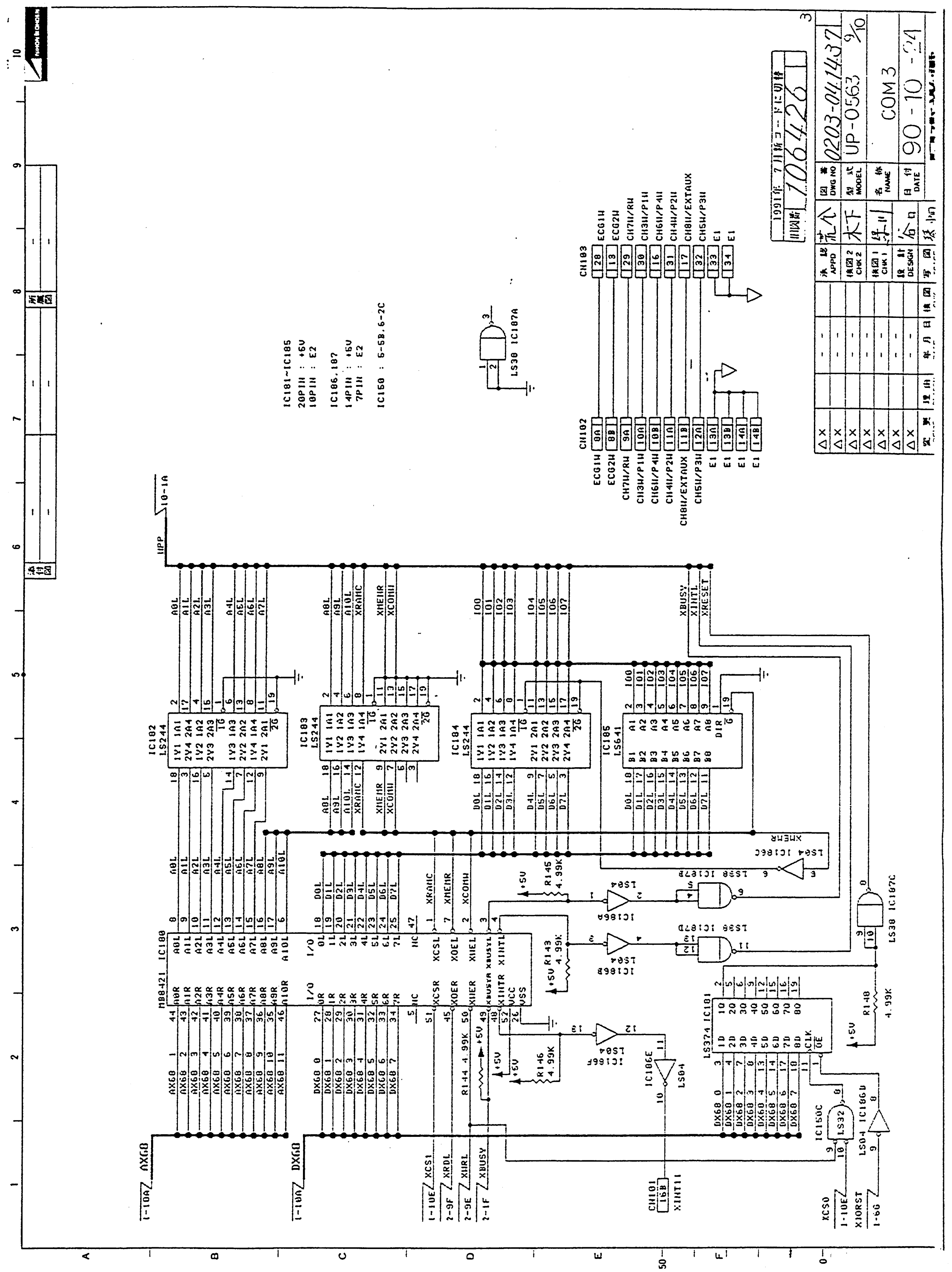

0203-041393
UP-0563 5/10
COM3
90-10-24
706422 A
IC143 8251
IC146 LS273
IC145 LS157
IC147A LS74
IC147B LS74
IC144A LS74
IC144B LS74
CN104
CN102

12. CIRCUIT DIAGRAM

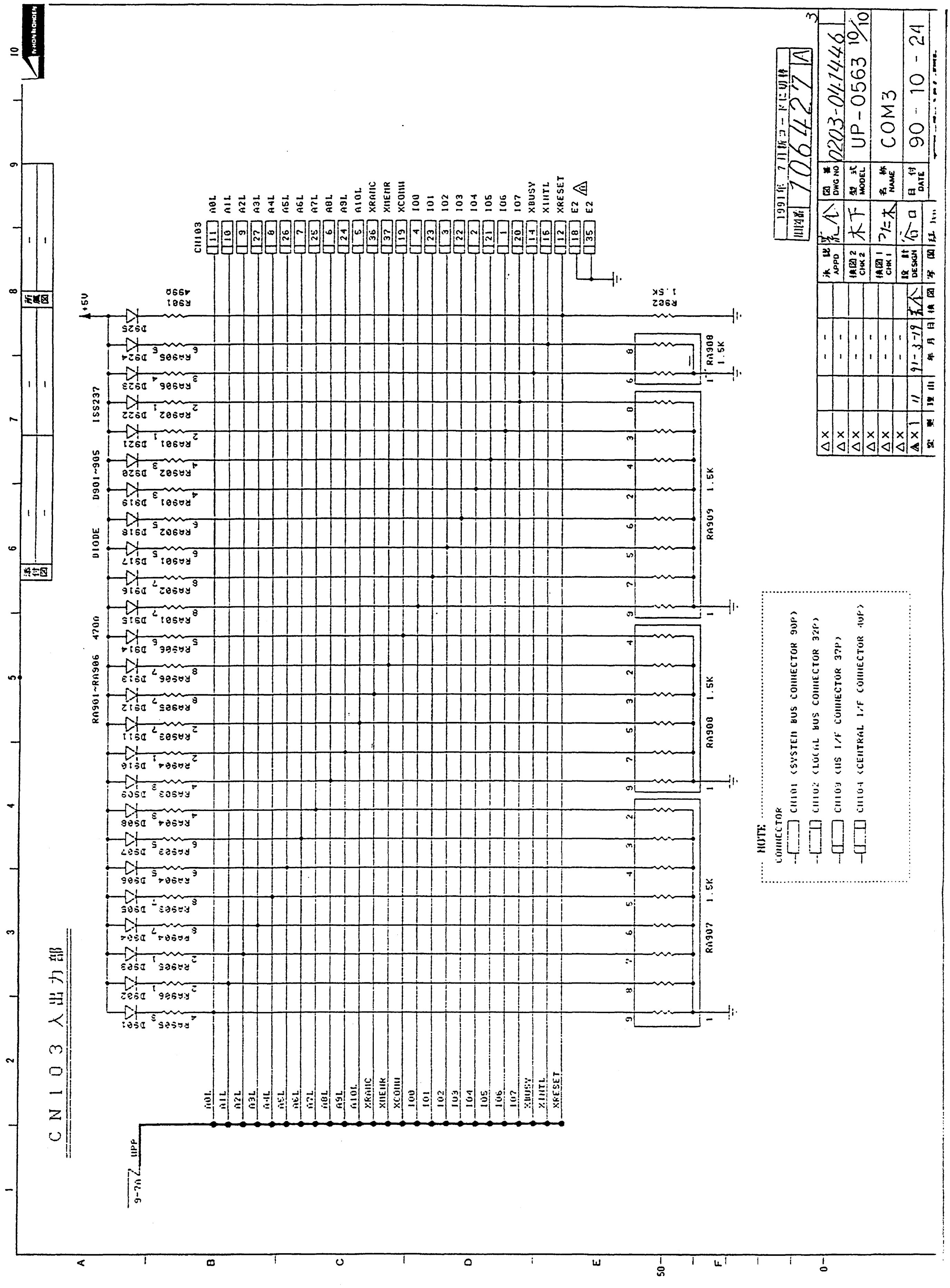

IC166
HA17012PB
SK156
IC162 μPC811C
IC163 μPC811C
IC157 LS273
IC158 LS273
IC150A LS32
IC150B LS32
IC160 LS139
IC161 LT1009
IC173 78L15
IC172 79L15
D001 1S2076A
D002 1S2076A
TP1 E1
TP2 E2
TP3 REF2.5
TP4 DAOUT (±5V)
TP5
TP6 E1
GAIN 1
OFFSET1
OFFSET2
VR101 10K
VR102 100Ω
VR103 100Ω
VR104 10K
R123 49.9Ω
R124 40.2KΩ
R126 40.2KΩ
R127 1.24K
R128 1.24K
R129 20Ω
R130 2.49K
R131 2.49K
R132 10Ω
R133 10Ω
R134 4.99K
R150 1.24K
R151 1.24K
+15V
-15V
+5V
CN101
+21V
-21V
E4
E2
DX05
XRESDS
X10HR
XD/ASEL
4-6H
4-6G
4-10E
4-1C
5-1F
IC157.158 20PIN : +5V 10PIN : E2
IC160 16PIN : +5V 8PIN : E2
IC150 : 9-1G 5-5B
※ CAPACITOR
COXX = C020, C021, C023, C024, C040, C062, C067, C068
COYY = C022, C025~C061, C063~C066, C010
1991年7月
706423 A
0203-041140
UP-0563 6/10
COM3
90-10-24
APPD
CHK2
CHK1
DESIGN
DWG NO
MODEL
NAME
DATE


IC164 LS273
IC165 LS244
IC166A LS390
IC166B LS390
IC167 LS163
IC168 IC4040
IC136B LS04
IC136D LS04
IC136E LS04
IC136F LS04
IC171A LS132
IC171B LS132
IC171C LS132
IC171D LS132
IC125C LS00
IC169A LS123
IC169B LS123
IC170A LS123
IC170B LS123
RA114 GL-3AR2 x8
LED101
LED102
LED103
LED104
LED105
LED106
LED107
LED108
LED109 HDT
RA112 4.7K
RA113 4.7K x2
R135 10K
R136 63.0K
R137 49.9K
R138 4.99K
R139 4.99K
R140 15K
R141 499Ω
R142 1K
C118 0.0022µ
C119 6.0µ/35V
C120 0.001µ
C121 6.0µ/35V
D101 1S2076A
SW101
SW102
SW103 RESET
+5V
DX05
XRES85
XLEDS
XSUS
XIOKSTOS
XHDT
XHLEDS
CLK3M
RST7.5
CLK96
XRSTIN
HDTINT
XS/T05
4-6A
4-1C
4-10F
4-10E
2-9B
2-9C
4-1B
6-6E
6-1D
4-6B
SW101 : B-0A-T
SW102 : B-4A-T
IC164,165 20PIN : +5V 10PIN : E2
IC166-170 16PIN : +5V 8PIN : E2
IC171 14PIN : +5V 7PIN : E2
DWG NO 0203-041419
MODEL UP-0563 7/10
NAME COM3
DATE 90-10-24
70642424

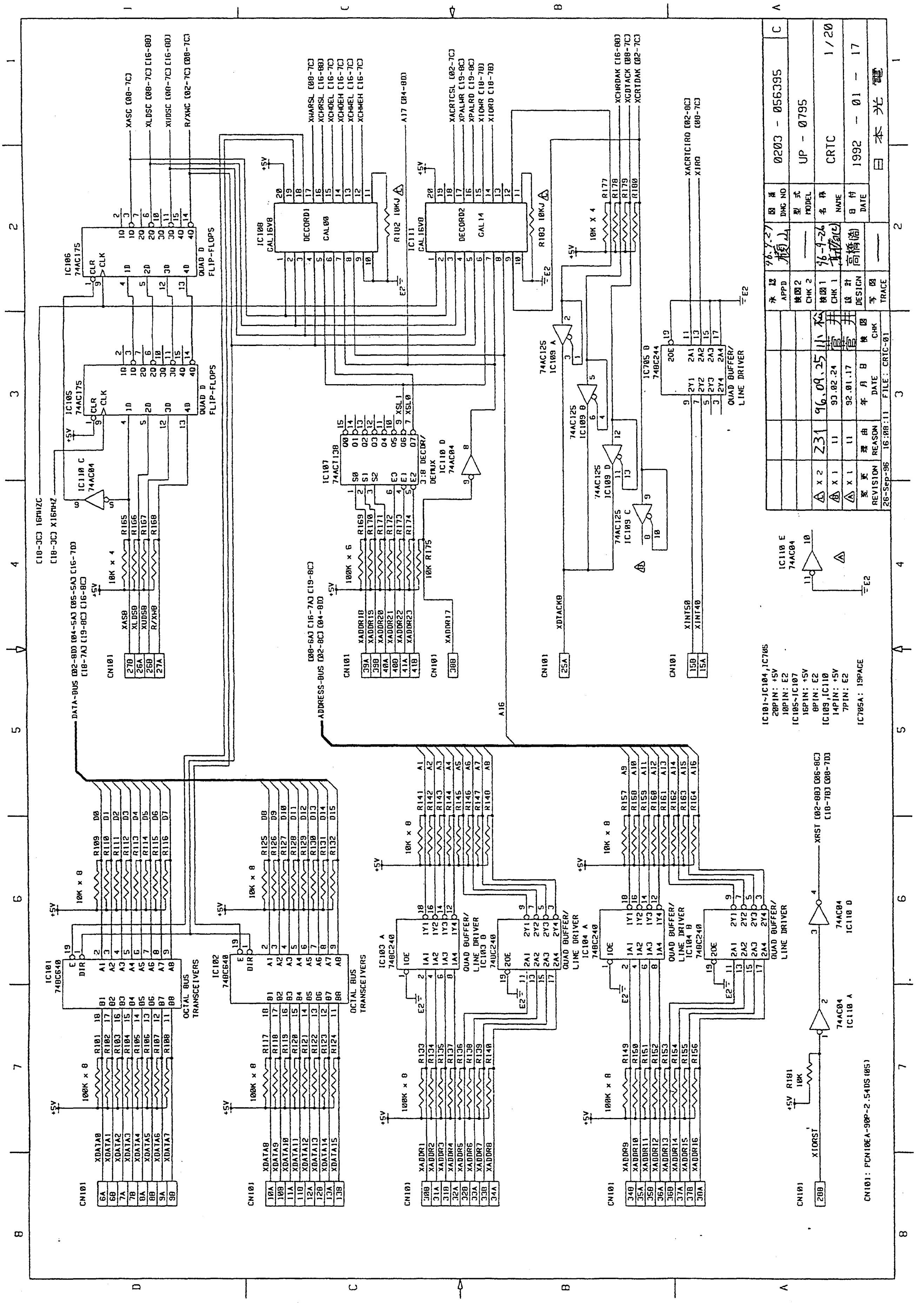

IC179
MB84256
IC178
MB84256
IC177
MB84256
IC176
MB84256
IC175
MBM27C512-20
SK175
IC174
MBM27C512-20
SK174
F9000-F9FFFF
F8000-F8FFFF
F0000-F1FFFF
DX60
AX60
XRDL
XWRL
XRDU
XWRU
XCS3
XCS4
XCS5
XCS
XOE
XWE
Vcc
GND
+5V
0203-041428
UP-0563
COM3
90-10-24
1064251


MB8421 IC180
IC182 LS244
IC183 LS244
IC184 LS244
IC185 LS641
LS324 IC181
IC150C LS32
LS04 IC186D
LS04 IC186E
LS04 IC186F
LS04 IC186A
LS04 IC186B
LS04 IC186C
LS38 IC187A
LS38 IC187B
LS38 IC187C
LS38 IC187D
IC181~IC185
20PIN : +5V
10PIN : E2
IC186,187
14PIN : +5V
7PIN : E2
IC150 : 5-5B,6-2C
CN102
CN103
CN101
AXGB
DXGB
HPP
10-1A
XCS1
XRDL
XHRL
XBUSY
XCS0
XIORST
XINT11
XBUSY
XINTL
XRESET
XMEMR
XCOMH
XRAMC
R143 4.99K
R144 4.99K
R145 4.99K
R146 4.99K
R148 4.99K
+5V
ECG1H
ECG2H
CH7H/RH
CH3H/P1H
CH6H/P4H
CH4H/P2H
CH8H/EXTAUX
CH5H/P3H
E1
1991年 7月1日
1064426
0203-041437
UP-0563
9/10
COM3
90-10-24
NIHON KOHDEN

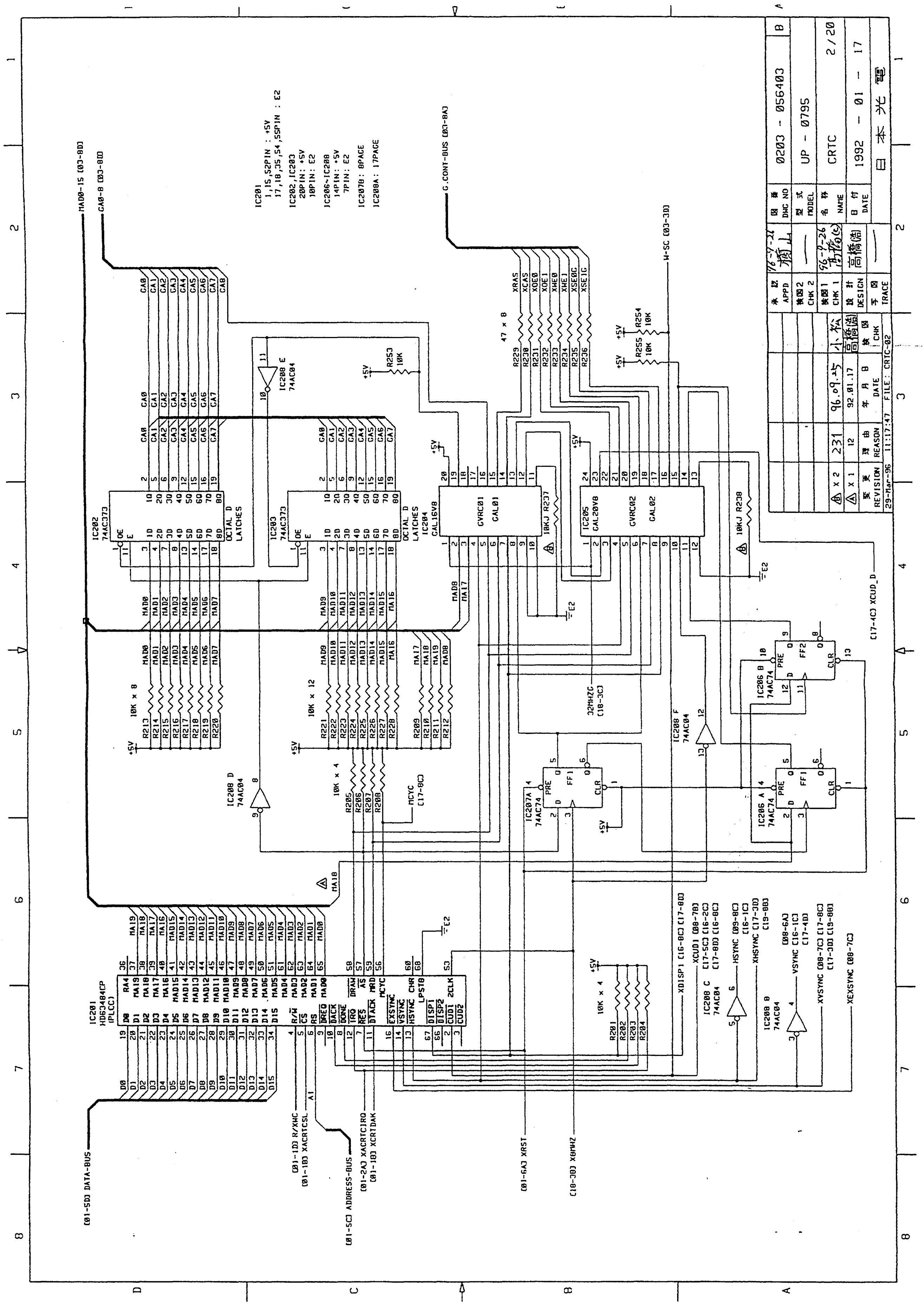
12. CIRCUIT DIAGRAM

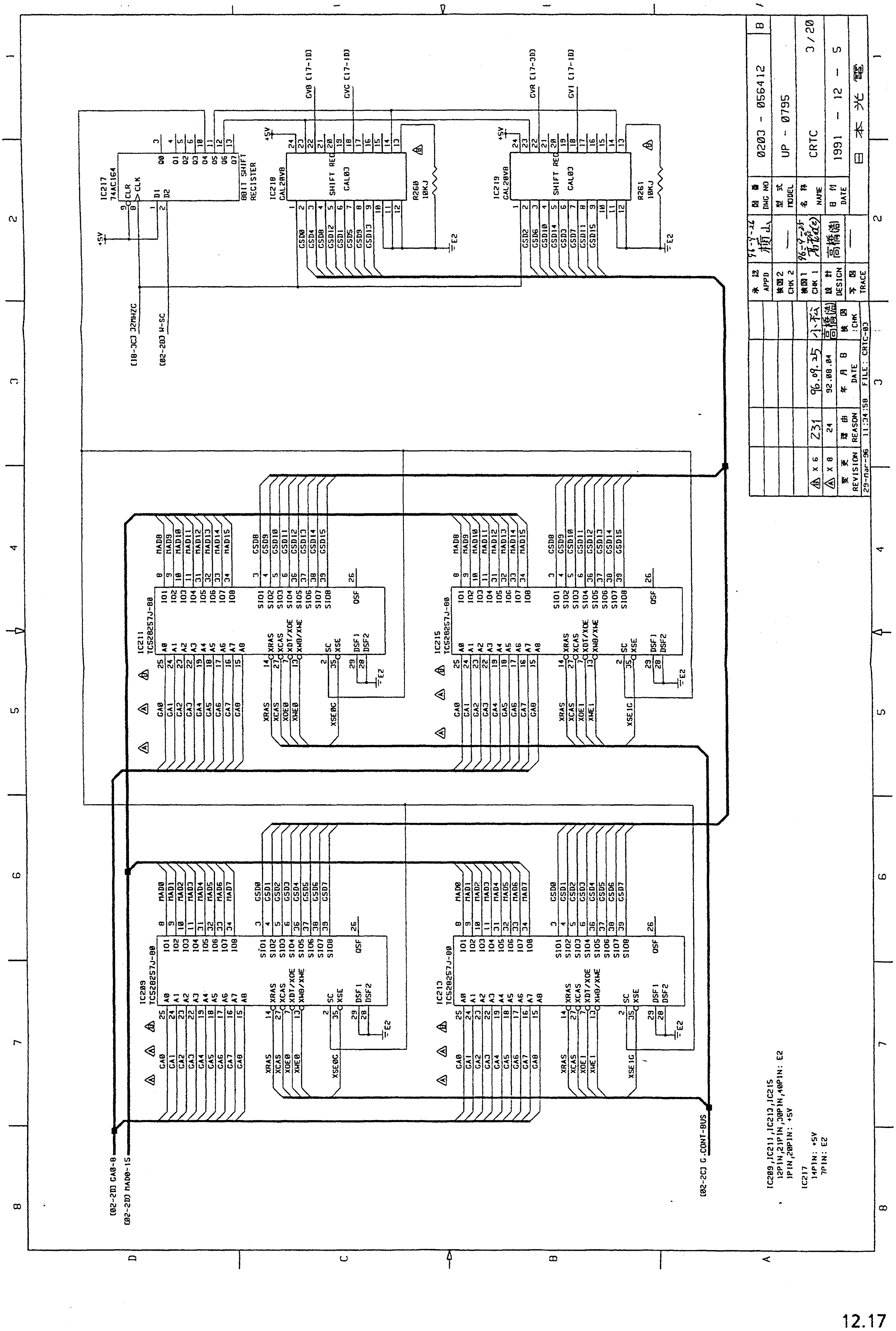


CN103 入出力部
CN103
A0L
A1L
A2L
A3L
A4L
A5L
A6L
A7L
A8L
A9L
A10L
XRAHC
XHEHR
XCOHH
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
XBUSY
XINTL
XRESET
E2
E2
+5V
R901 470Ω
R902 1.5K
RA901~RA906 470Ω
DIODE D901~905 1SS237
RA907 1.5K
RA908 1.5K
RA909 1.5K
NOTE
CONNECTOR
CN101 (SYSTEM BUS CONNECTOR 90P)
CN102 (LOCAL BUS CONNECTOR 32P)
CN103 (HS I/F CONNECTOR 37P)
CN104 (CENTRAL I/F CONNECTOR 40P)
706427A
0203-041446
UP-0563 10/10
COM3
90 - 10 - 24
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN

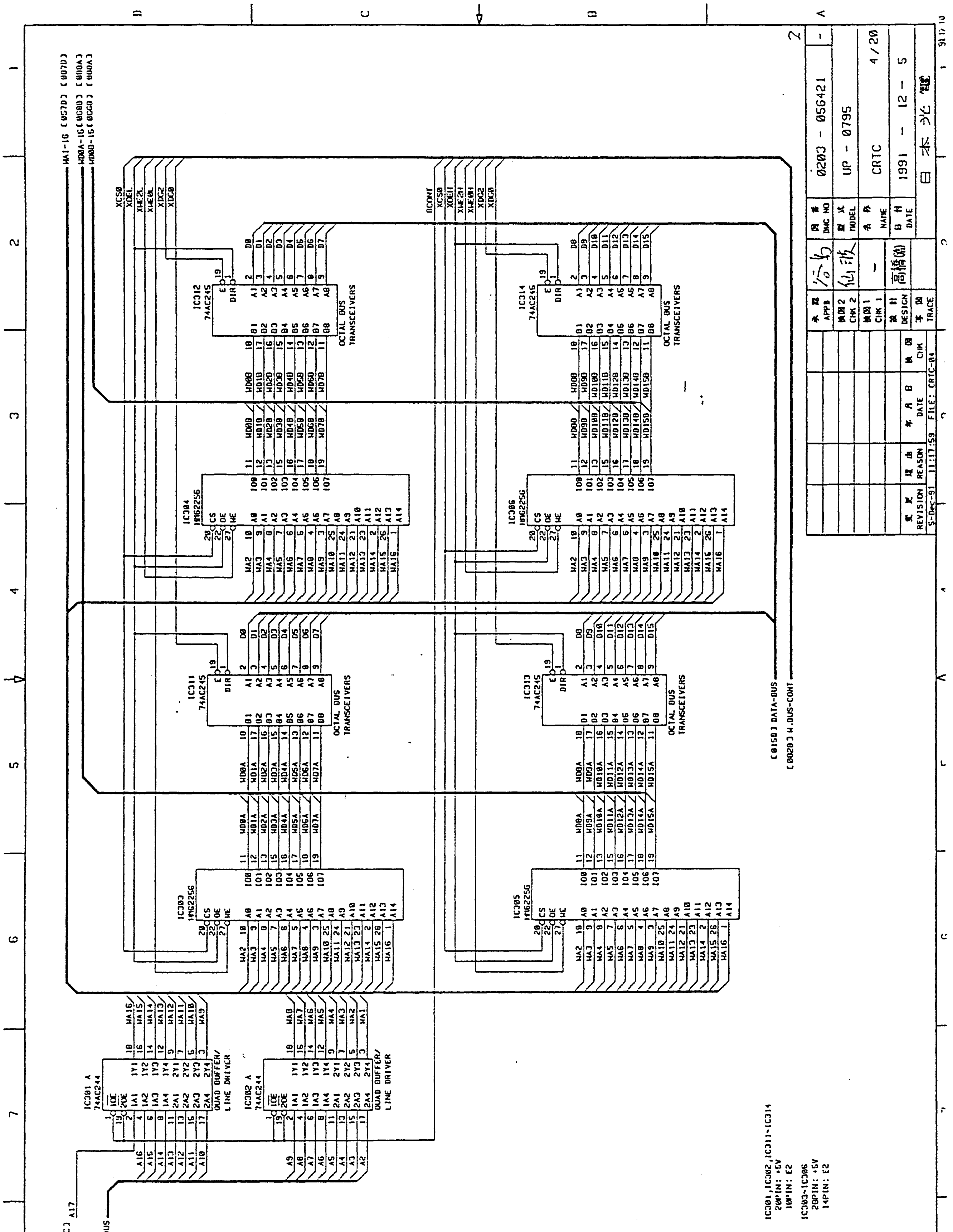

0203 - 056395
UP - 0795
CRTC
1/20
1992 - 01 - 17
日本光電
IC101 74BC640 OCTAL BUS TRANSCEIVERS
IC102 74BC640 OCTAL BUS TRANSCEIVERS
IC103 A 74BC240 QUAD BUFFER/LINE DRIVER
IC103 B 74BC240 QUAD BUFFER/LINE DRIVER
IC104 A 74BC240 QUAD BUFFER/LINE DRIVER
IC104 B 74BC240 QUAD BUFFER/LINE DRIVER
IC105 74AC175 QUAD D FLIP-FLOPS
IC106 74AC175 QUAD D FLIP-FLOPS
IC107 74AC138 3:8 DECDR/DEMUX
IC108 GAL16V8 DECORD1 CAL08
IC111 GAL16V8 DECORD2 GAL14
IC109 A 74AC125
IC109 B 74AC125
IC109 C 74AC125
IC109 D 74AC125
IC110 A 74AC04
IC110 C 74AC04
IC110 D 74AC04
IC110 E 74AC04
IC705 B 74BC244 QUAD BUFFER/LINE DRIVER
DATA-BUS
ADDRESS-BUS
CN101
CN101: PCN10EA-90P-2.54DS(05)
FILE: CRTC-01
26-Sep-96

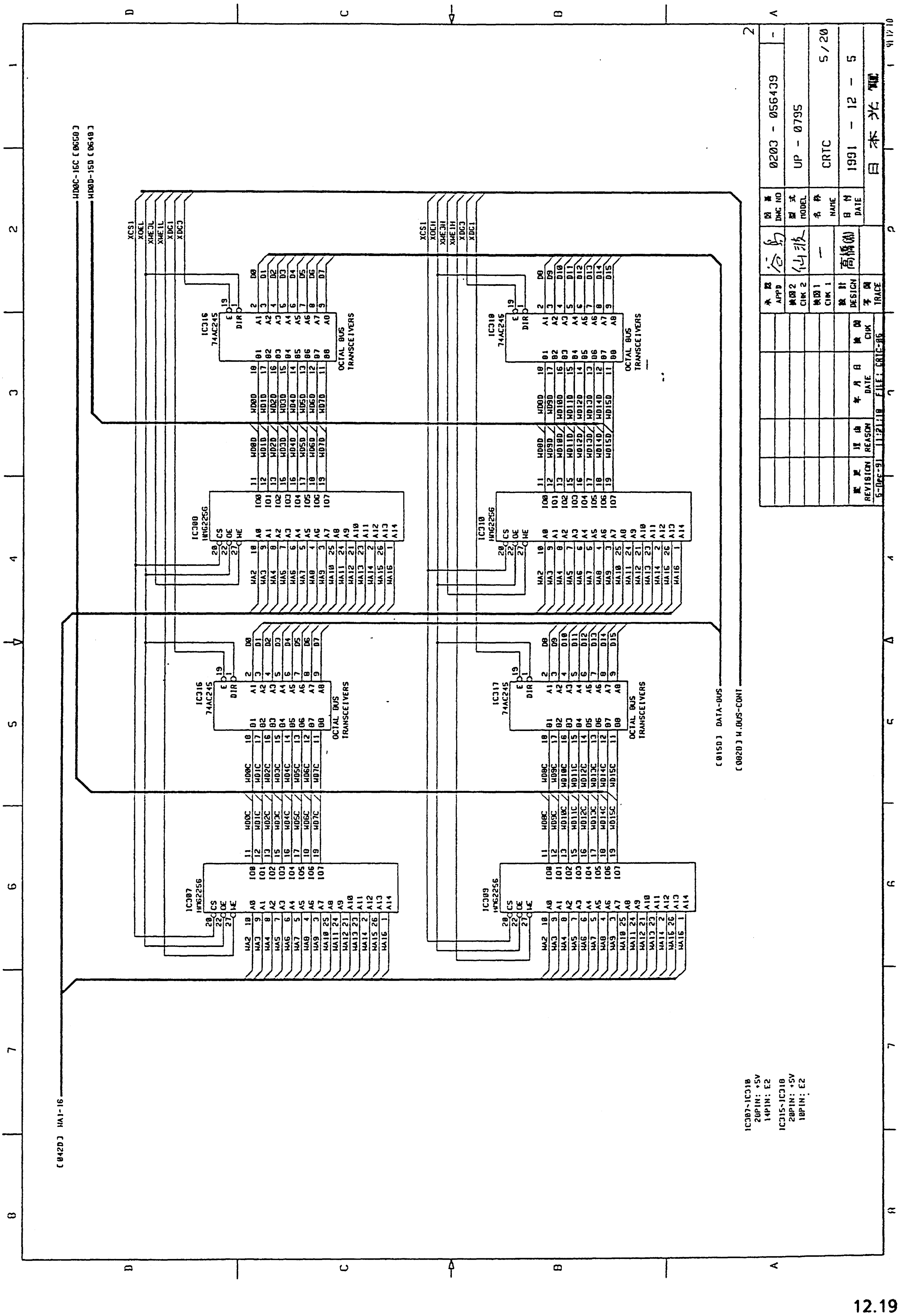
12. CIRCUIT DIAGRAM


0203 - 056403
B
UP - 0795
CRTC
2/20
1992 - 01 - 17
日 本 光 電
FILE : CRTC-02
29-Mar-96 11:17:47
IC201 HD63484CP (PLCC)
IC202 74AC373 OCTAL D LATCHES
IC203 74AC373 OCTAL D LATCHES
IC204 GAL16V8 GVRC01 GAL01
IC205 GAL20V8 GVRC02 GAL02
IC206 A 74AC74
IC206 B 74AC74
IC207A 74AC74
IC208 B 74AC04
IC208 C 74AC04
IC208 D 74AC04
IC208 E 74AC04
IC208 F 74AC04
[01-5D] DATA-BUS
[01-5C] ADDRESS-BUS
[01-1D] R/XWC
[01-1B] XACRTCSL
[01-2A] XACRTCIRQ
[01-1B] XCRTDAK
[01-6A] XRST
[18-3D] X8MHZ
MAD0-15 [03-8D]
GA0-8 [03-8D]
G.CONT-BUS [03-8A]
W-SC [03-3D]
32MHZC [18-3C]
MCYC [17-8C]
[17-4C] XCUD_D

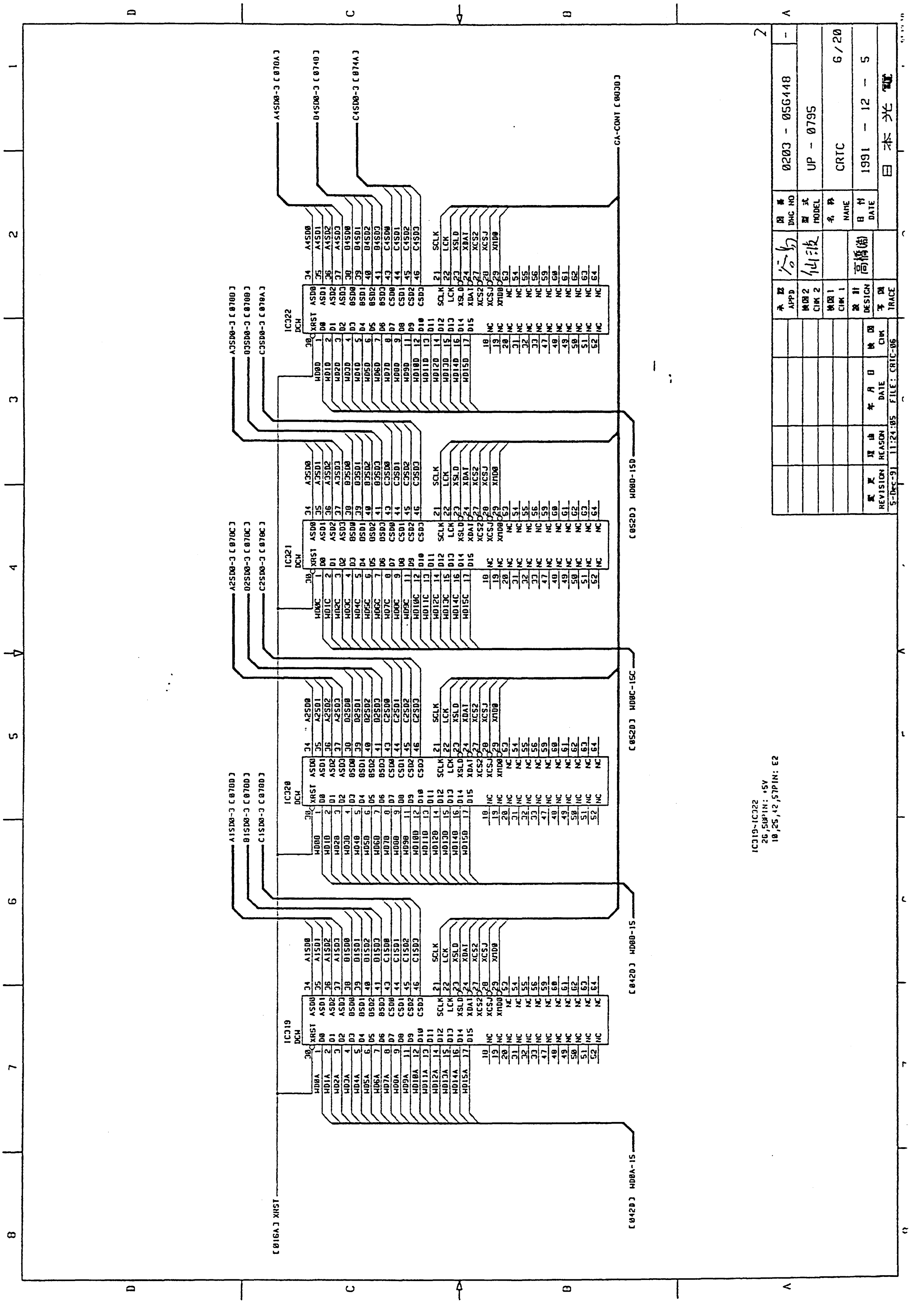

IC217
74AC164
8BIT SHIFT REGISTER
IC218
CAL20V8
SHIFT REG
CAL03
IC219
CAL20V8
R260
10KJ
R261
10KJ
CV0 [17-1D]
CVC [17-1D]
CVR [17-3D]
CVI [17-1D]
[10-3C] 32MHZC
[02-2D] H-SC
IC211
TC528257J-80
IC215
TC528257J-80
IC209
TC528257J-80
IC213
TC528257J-80
[02-2D] CA0-8
[02-2D] MAD0-15
[02-2C] G.CONT-BUS
IC209,IC211,IC213,IC215
12PIN,21PIN,30PIN,40PIN: E2
1PIN,20PIN: +5V
IC217
14PIN: +5V
7PIN: E2
0203 - 056412
UP - 0795
CRTC
3/20
1991 - 12 - 5
FILE: CRTC-03

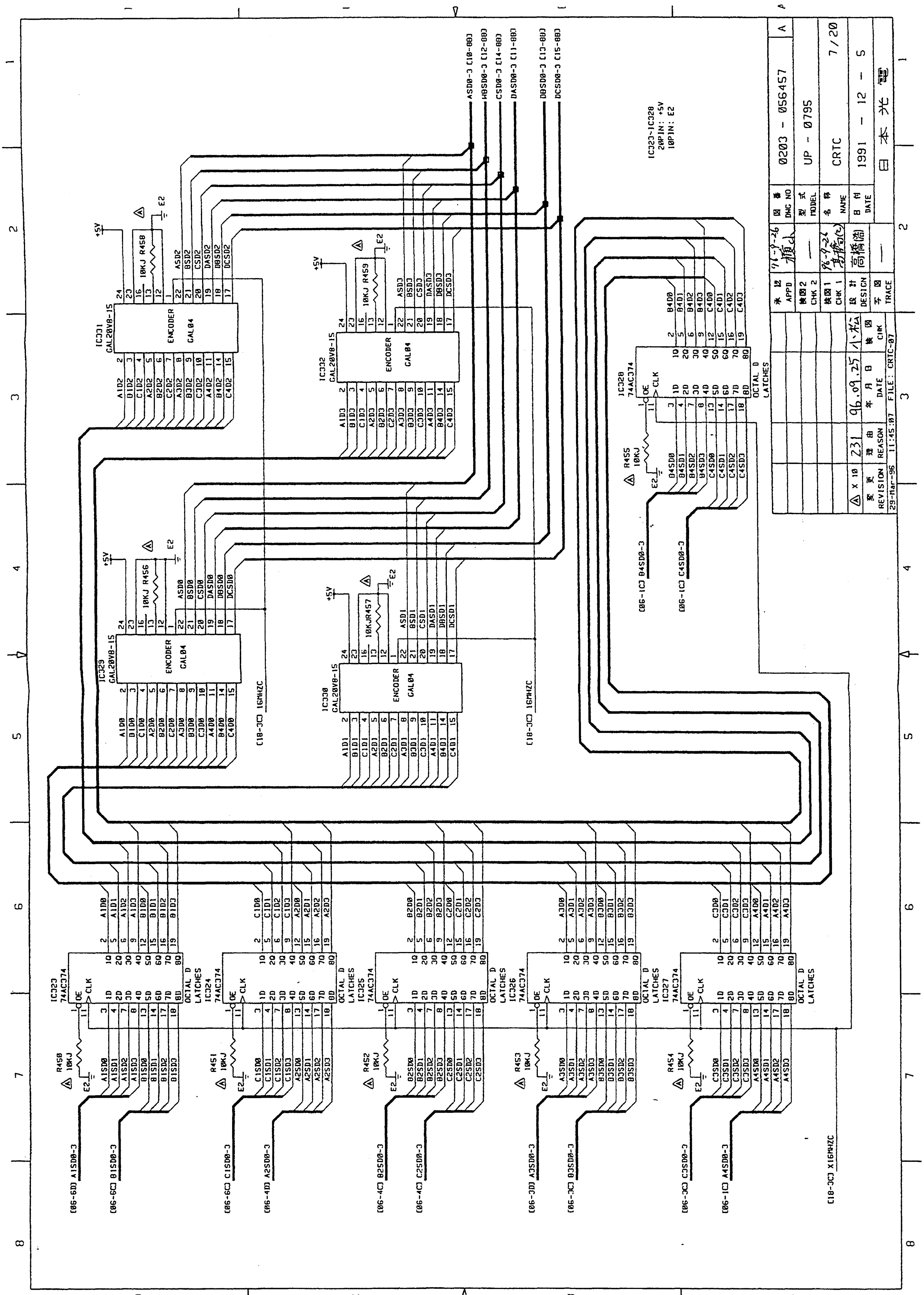
12. CIRCUIT DIAGRAM


IC301 A
74AC244
QUAD BUFFER/
LINE DRIVER
IC302 A
74AC244
QUAD BUFFER/
LINE DRIVER
IC303
HM62256
IC304
HM62256
IC305
HM62256
IC306
HM62256
IC311
74AC245
IC312
74AC245
IC313
74AC245
IC314
74AC245
OCTAL BUS
TRANSCEIVERS
HA1-16 [057D] [007D]
HD0A-15[060D] [010A]
HD00-15[066D] [000A]
XCS0
XOEL
XWE2L
XWE0L
XDG2
XDG0
DCONT
XOE1
XWE21
XWE01
[0150] DATA-BUS
[0020] H.BUS-CONT
[01C] A17
[015C] ADDRESS-BUS
IC301,IC302,IC311-IC314
20PIN: +5V
10PIN: E2
IC303-IC306
28PIN: +5V
14PIN: E2
0203 - 056421
UP - 0795
CRTC
4/20
1991 - 12 - 5
5-Dec-91 11:17:59 FILE: CRTC-04
REVISION
REASON
DATE
CHK
APPD
CHK 2
CHK 1
DESIGN
TRACE
DWG NO
MODEL
NAME
DATE
高橋

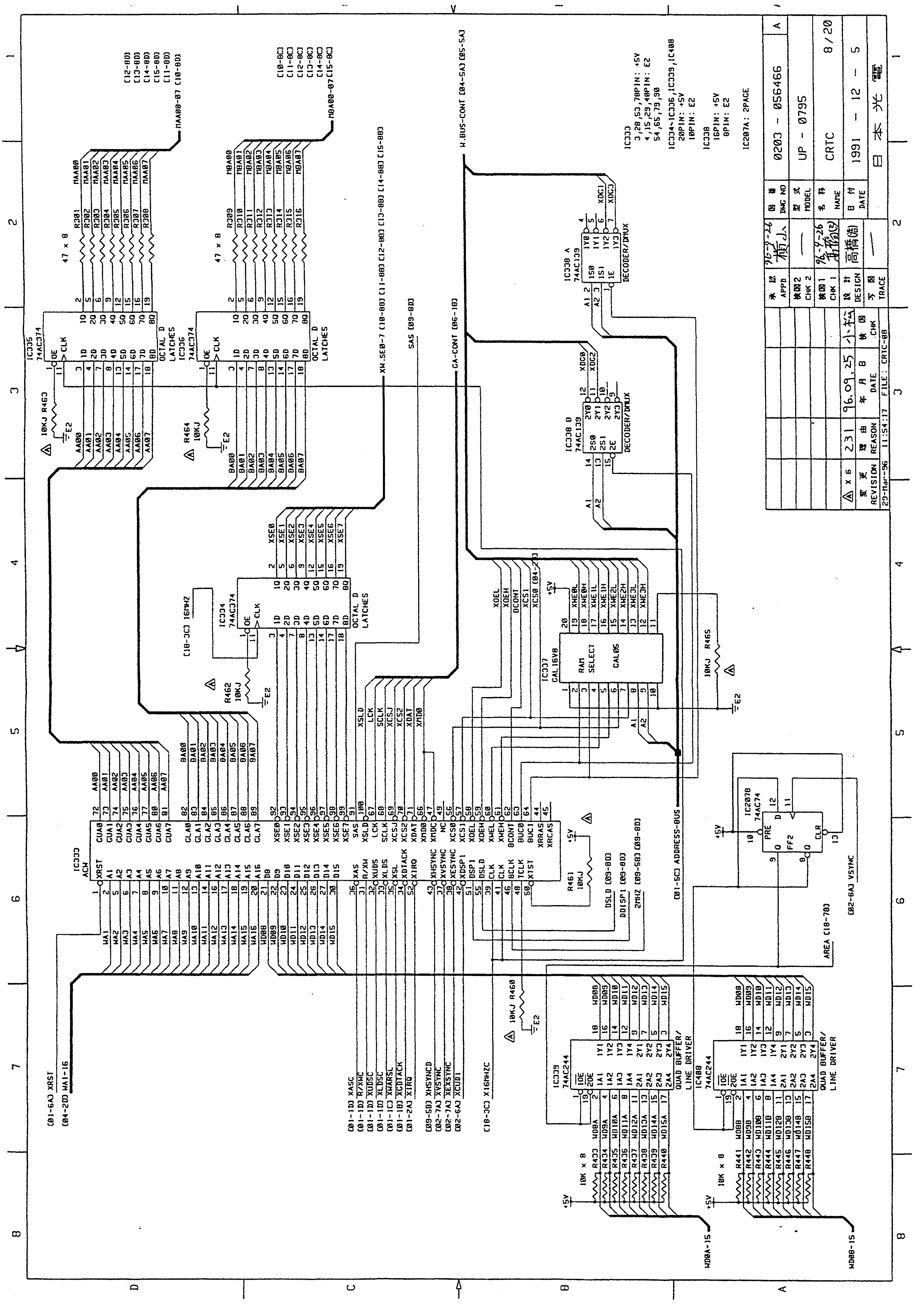

IC316
74AC245
OCTAL BUS TRANSCEIVERS
IC318
74AC245
IC317
74AC245
IC308
HM62256
IC310
HM62256
IC307
HM62256
IC309
HM62256
XCS1
XOEL
XHE3L
XHE1L
XDC1
XDC3
XOEH
XHE3H
XHE1H
[065D] HD0C-15C
[064D] HD0D-15D
[015D] DATA-BUS
[082D] H.BUS-CONT
[042D] HA1-16
IC307-IC310 28PIN: +5V 14PIN: E2
IC315-IC318 20PIN: +5V 10PIN: E2
0203 - 056439
UP - 0795
CRTC
5/20
1991 - 12 - 5
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
FILE: CRTC-05

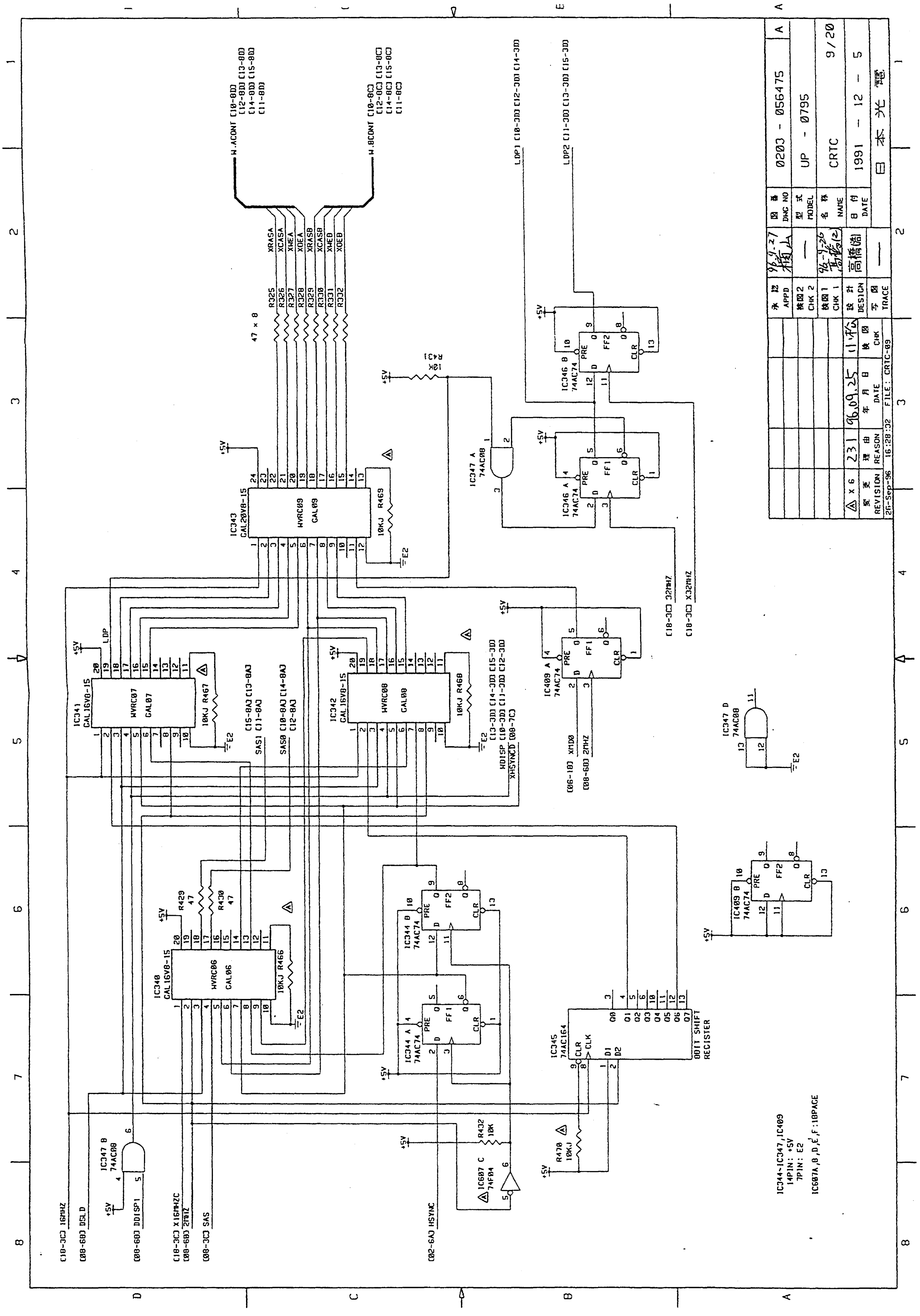
12. CIRCUIT DIAGRAM


IC319
IC320
IC321
IC322
DCH
XRST
SCLK
LCK
XSLD
XDAT
XCS2
XCSJ
XMD0
A1SD0-3 [070D]
01SD0-3 [070D]
C1SD0-3 [070D]
A2SD0-3 [070C]
02SD0-3 [070C]
C2SD0-3 [070C]
A3SD0-3 [070D]
03SD0-3 [070D]
C3SD0-3 [070A]
A4SD0-3 [070A]
04SD0-3 [074D]
C4SD0-3 [074A]
GA-CONT [003D]
[042D] HD0A-15
[042D] HD0B-15
[052D] HD0C-15C
[052D] HD0D-15D
[016A] XHST
IC319-IC322
26,50PIN: +5V
10,25,42,57PIN: E2
0203 - 05G448
UP - 0795
CRTC
6/20
1991 - 12 - 5
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
5-Dec-91
11:24:05
FILE: CRTC-06

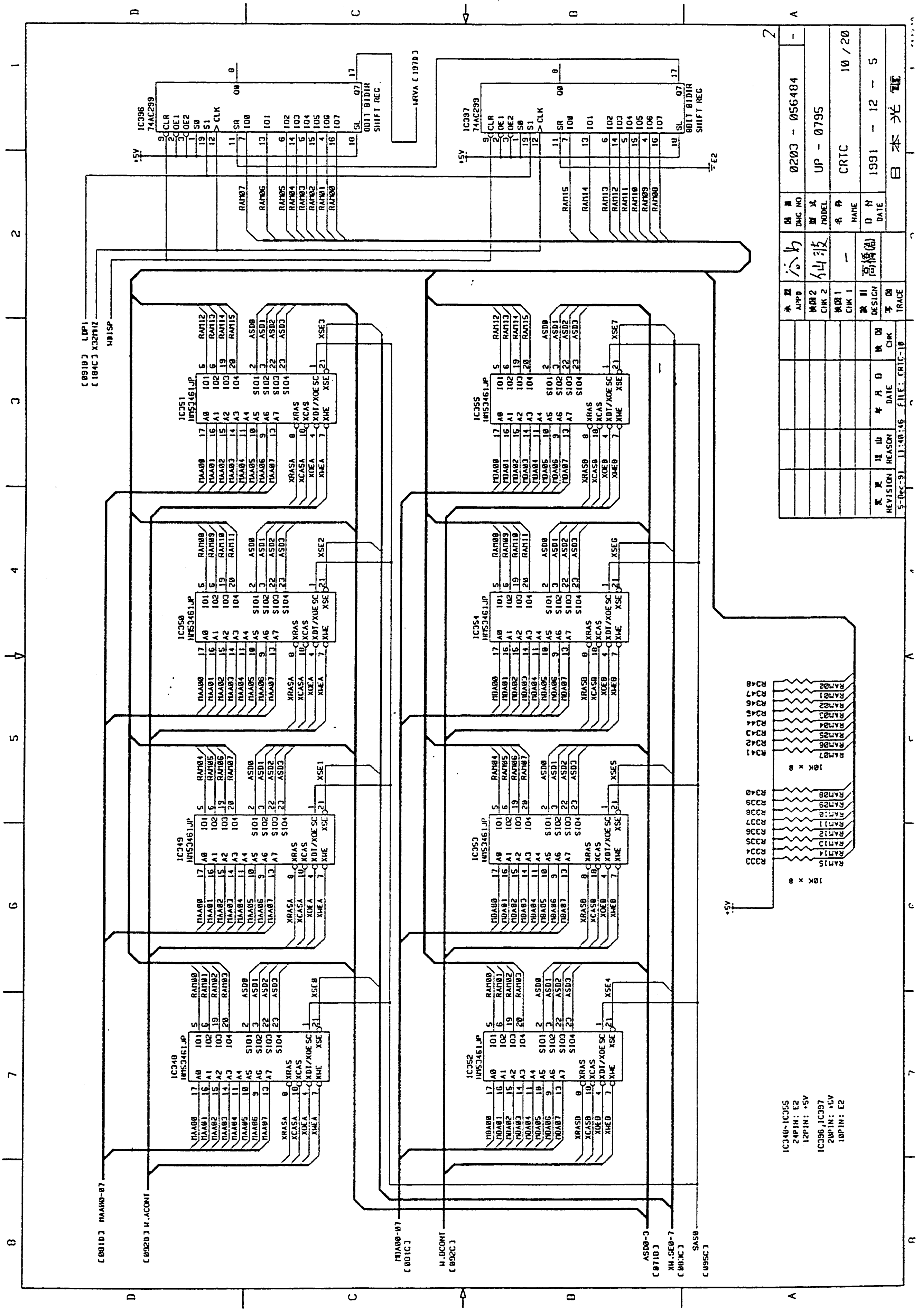

IC323 74AC374 OCTAL D LATCHES
IC324 74AC374 OCTAL D LATCHES
IC325 74AC374 OCTAL D LATCHES
IC326 74AC374 OCTAL D LATCHES
IC327 74AC374 OCTAL D LATCHES
IC328 74AC374 OCTAL D LATCHES
IC329 GAL20V8-15 ENCODER GAL04
IC330 GAL20V8-15 ENCODER GAL04
IC331 GAL20V8-15 ENCODER GAL04
IC332 GAL20V8-15 ENCODER GAL04
IC323~IC328 20PIN: +5V 10PIN: E2
R450 10KJ
R451 10KJ
R452 10KJ
R453 10KJ
R454 10KJ
R455 10KJ
10KJ R456
10KJR457
10KJ R458
10KJ R459
+5V
E2
ASD0-3 [10-8B]
HBSD0-3 [12-8B]
CSD0-3 [14-8B]
DASD0-3 [11-8B]
DBSD0-3 [13-8B]
DCSD0-3 [15-8B]
[06-6D] A1SD0-3
[06-6C] B1SD0-3
[06-6C] C1SD0-3
[06-4D] A2SD0-3
[06-4C] B2SD0-3
[06-4C] C2SD0-3
[06-3D] A3SD0-3
[06-3C] B3SD0-3
[06-3C] C3SD0-3
[06-1C] A4SD0-3
[06-1C] B4SD0-3
[06-1C] C4SD0-3
[18-3C] 16MHZC
[18-3C] X16MHZC
0203 - 056457
UP - 0795
CRTC
7/20
1991 - 12 - 5
日本光電
図番 DWG NO
型式 MODEL
名称 NAME
日付 DATE
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
变更 REVISION
理由 REASON
年月日 DATE
検図 CHK
96.09.25 小松
231
29-Mar-96 11:45:07 FILE: CRTC-07
A B C D
1 2 3 4 5 6 7 8

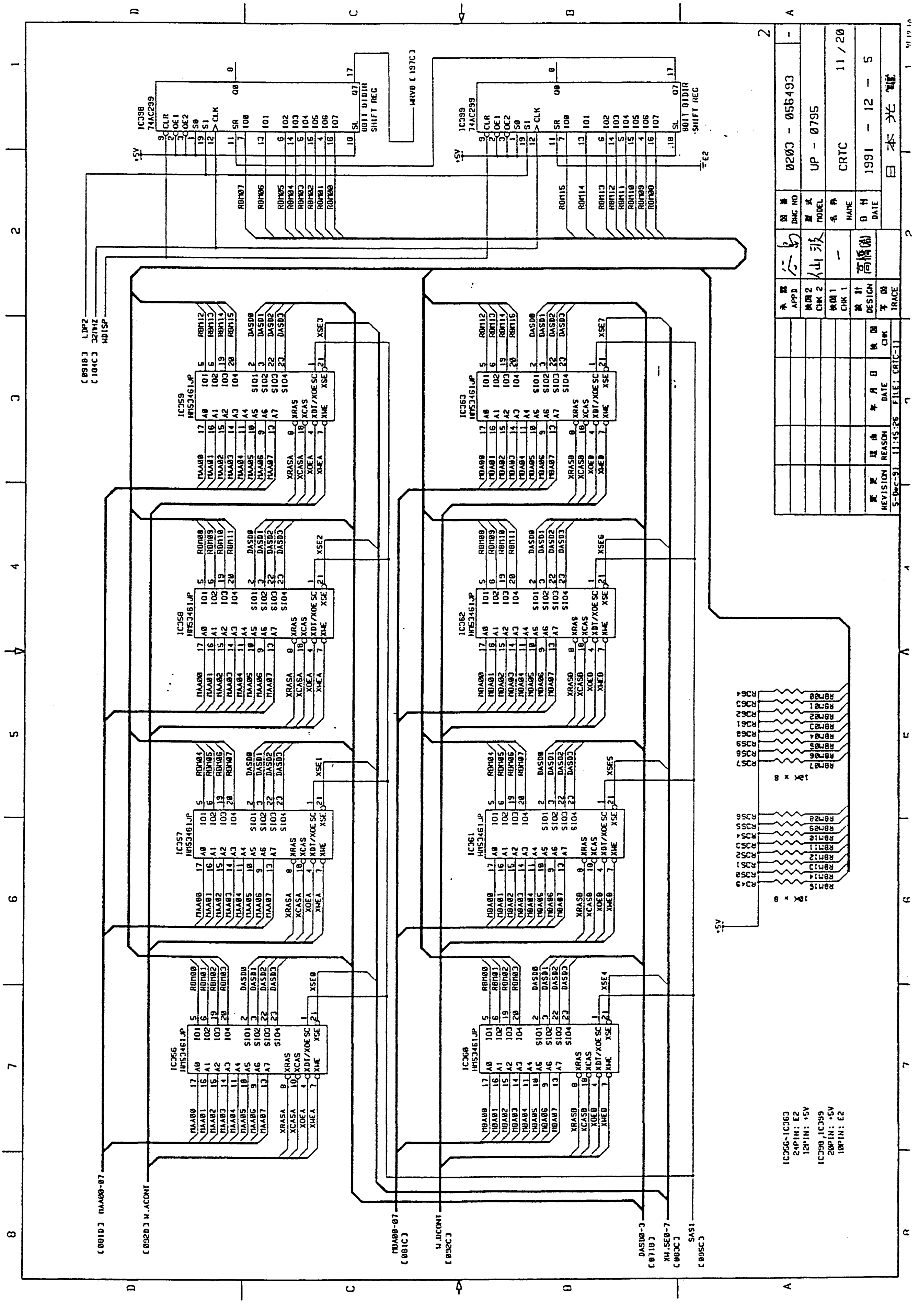
12. CIRCUIT DIAGRAM


0203 - 056466
UP - 0795
CRTC
8/20
1991 - 12 - 5
日本光電
IC33 ACH
IC35 74AC374
IC36 74AC374
IC34 74AC374
IC37 CAL16V8
IC38 A 74AC139
IC38 B 74AC139
IC39 74AC244
IC400 74AC244
IC207B 74AC74
OCTAL D LATCHES
DECODER/DMUX
QUAD BUFFER/ LINE DRIVER
[01-5C] ADDRESS-BUS
H.BUS-CONT
CA-CONT
AREA
VSYNC
29-Mar-96 11:54:17 FILE: CRTC-08


0203 - 056475
UP - 0795
CRTC
9/20
1991 - 12 - 5
日本光電
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
231
96.09.25
FILE: CRTC-09
26-Sep-96 16:28:32
IC340 CAL16V8-15 HVRC06 GAL06
IC341 CAL16V8-15 HVRC07 GAL07
IC342 CAL16V8-15 HVRC08 GAL08
IC343 CAL20V8-15 HVRC09 GAL09
IC344 A 74AC74
IC344 B 74AC74
IC345 74AC164 8BIT SHIFT REGISTER
IC346 A 74AC74
IC346 B 74AC74
IC347 A 74AC08
IC347 B 74AC08
IC347 D 74AC08
IC409 A 74AC74
IC409 B 74AC74
IC687 C 74F04
R325–R332 47 x 8
R431 10K
R432 10K
R429 47
R430 47
R466 10KJ
R467 10KJ
R468 10KJ
R469 10KJ
R470 10KJ
XRASA XCASA XWEA XOEA XRASB XCASB XWEB XOEB
W.ACONT
W.BCONT
LDP1
LDP2
LDP
SAS0
SAS1
HDISP
XHSYNCD
XMD0
2MHZ
32MHZ
X32MHZ
16MHZ
DSLD
DDISP1
X16MHZC
2MHZ
SAS
HSYNC
+5V
E2
IC344~IC347,IC409
14PIN: +5V
7PIN: E2
IC687A,B,E,F:10PAGE

12. CIRCUIT DIAGRAM


IC396 74AC299
IC397 74AC299
8BIT BIDIR SHIFT REG
HRVA [197D]
IC348 HM53461JP
IC349 HM53461JP
IC350 HM53461JP
IC351 HM53461JP
IC352 HM53461JP
IC353 HM53461JP
IC354 HM53461JP
IC355 HM53461JP
[091D] LDP1
[184C] X32MHZ
HBISP
[081D] MAA00-07
[092D] H.ACONT
MDA00-07 [081C]
H.DCONT [092C]
ASD0-3 [071D]
XH.SE0-7 [083C]
SAS0 [095C]
10K x 8
IC348~IC355 24PIN: E2 12PIN: +5V
IC396,IC397 20PIN: +5V 10PIN: E2
0203 - 056484
UP - 0795
CRTC
10 / 20
1991 - 12 - 5
5-Dec-91 11:40:46 FILE: CRTC-10


IC398
74AC299
8BIT BIDIR SHIFT REG
IC399
74AC299
8BIT BIDIR SHIFT REG
CLR
OE1
OE2
S0
S1
CLK
SR
SL
Q0
Q7
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
+5V
E2
WRVO [197C]
ROM00
ROM01
ROM02
ROM03
ROM04
ROM05
ROM06
ROM07
ROM08
ROM09
ROM10
ROM11
ROM12
ROM13
ROM14
ROM15
[091B] LDP2
[104C] 32MHZ
HDISP
IC356
IC357
IC358
IC359
IC360
IC361
IC362
IC363
HM53461JP
A0
A1
A2
A3
A4
A5
A6
A7
IO1
IO2
IO3
IO4
SIO1
SIO2
SIO3
SIO4
XRAS
XCAS
XDT/XOE
XWE
SC
XSE
MAA00
MAA01
MAA02
MAA03
MAA04
MAA05
MAA06
MAA07
MDA00
MDA01
MDA02
MDA03
MDA04
MDA05
MDA06
MDA07
XRASA
XCASA
XOEA
XWEA
XRASB
XCASB
XOEB
XWEB
DASD0
DASD1
DASD2
DASD3
XSE0
XSE1
XSE2
XSE3
XSE4
XSE5
XSE6
XSE7
RS49
RS50
RS51
RS52
RS53
RS54
RS55
RS56
RS57
RS58
RS59
RS60
RS61
RS62
RS63
RS64
10K × 8
[081D] MAA00-07
[082D] W.ACONT
MDA00-07
[081C]
W.BCONT
[082C]
DASD0-3
[071D]
XW.SE0-7
[003C]
SAS1
[095C]
IC356-IC363
24PIN: E2
12PIN: +5V
IC398, IC399
20PIN: +5V
10PIN: E2
図番 DWG NO
0203 - 056493
型式 MODEL
UP - 0795
名称 NAME
CRTC
11 / 20
日付 DATE
1991 - 12 - 5
日本光電
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
5-Dec-91
11:45:26
FILE: CRTC-11
A
B
C
D
1
2
3
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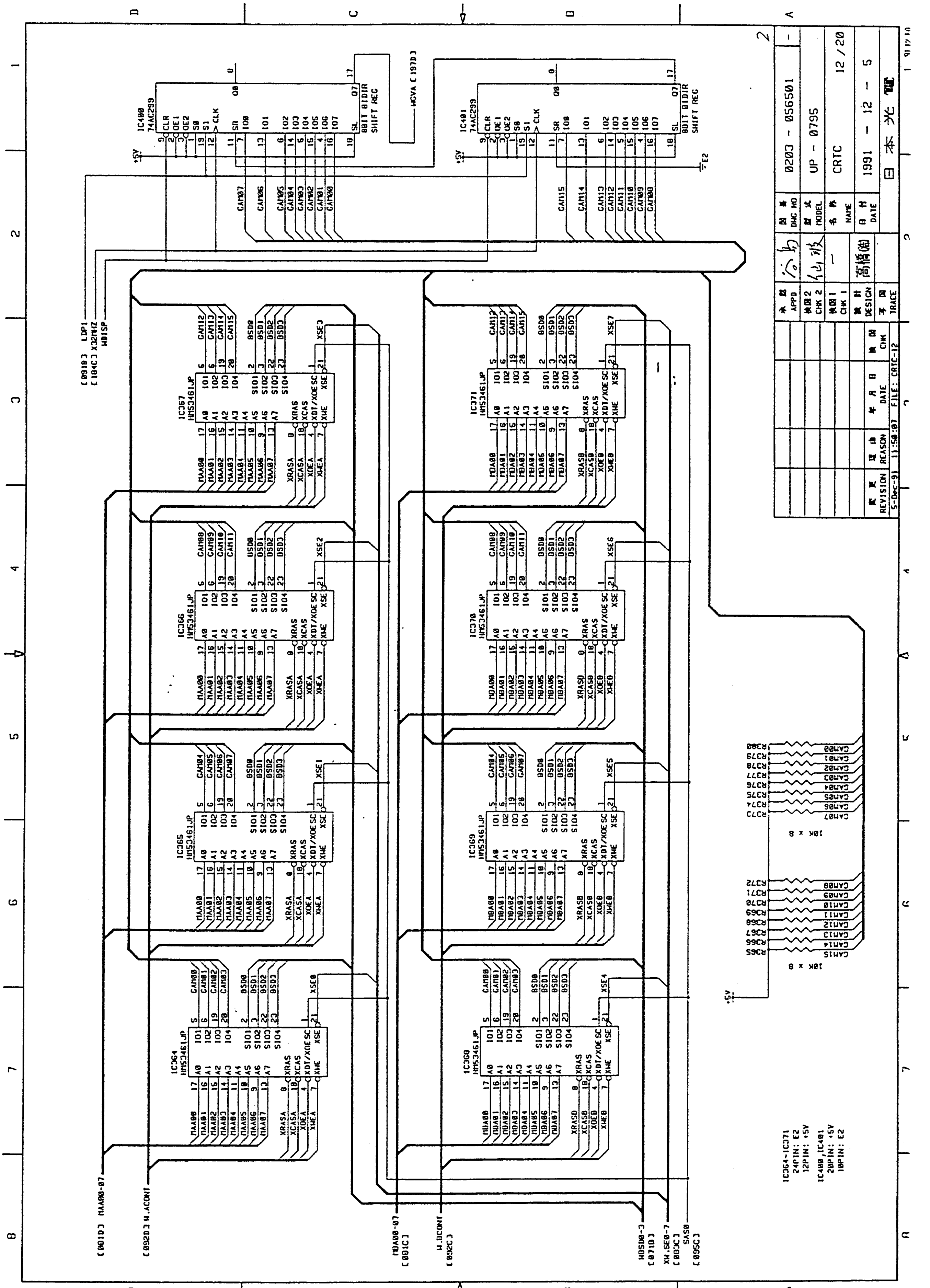
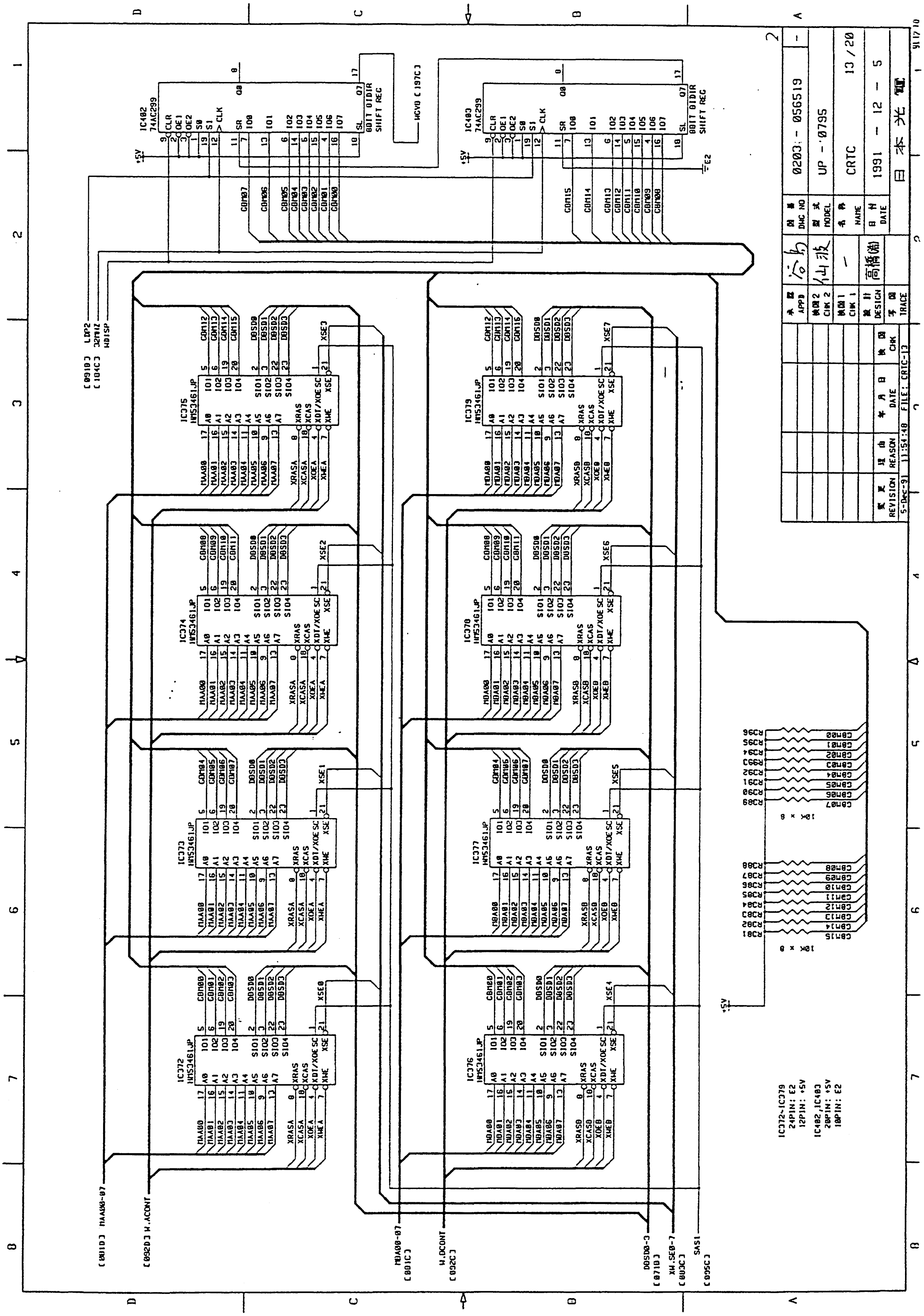
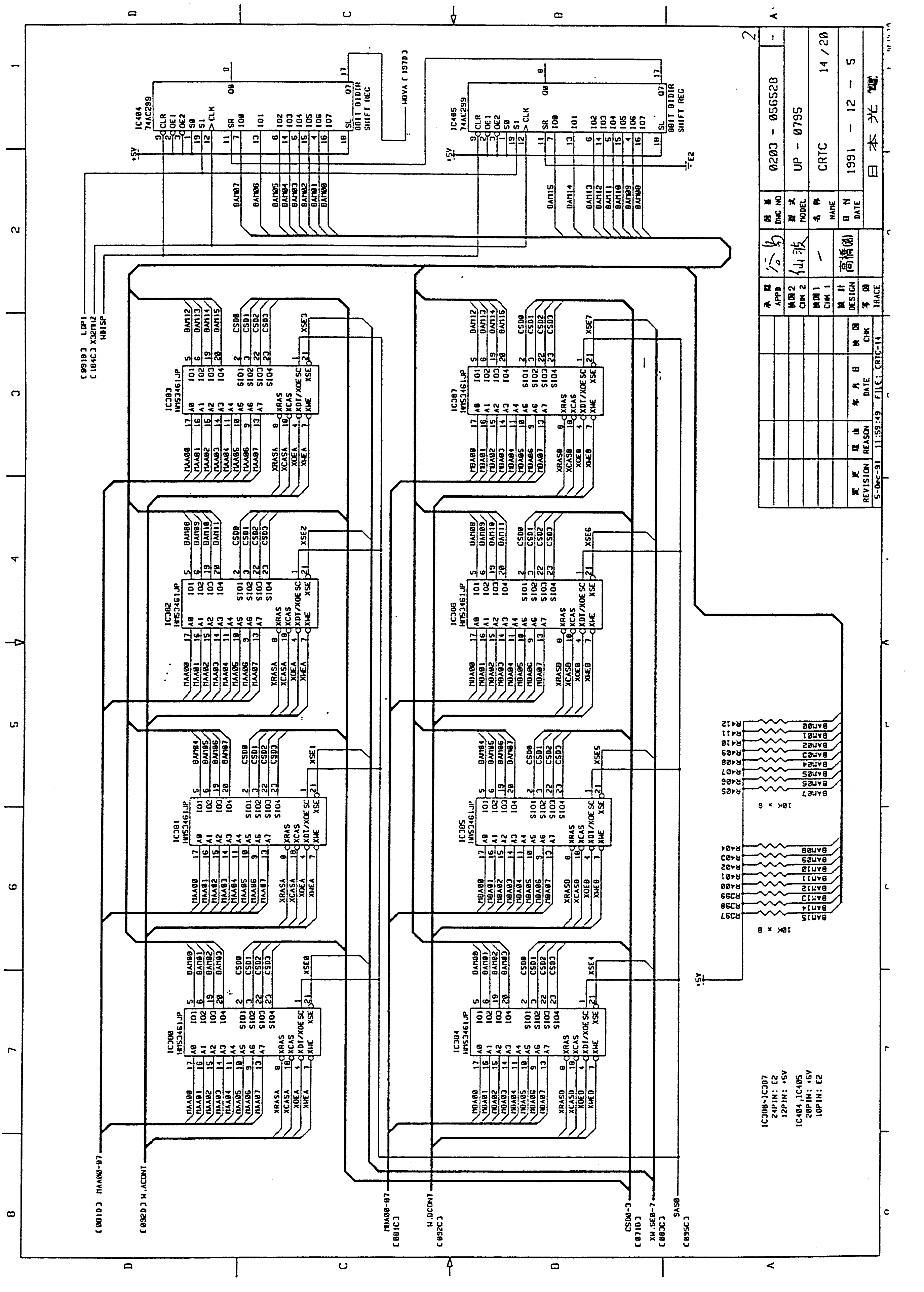
7
8

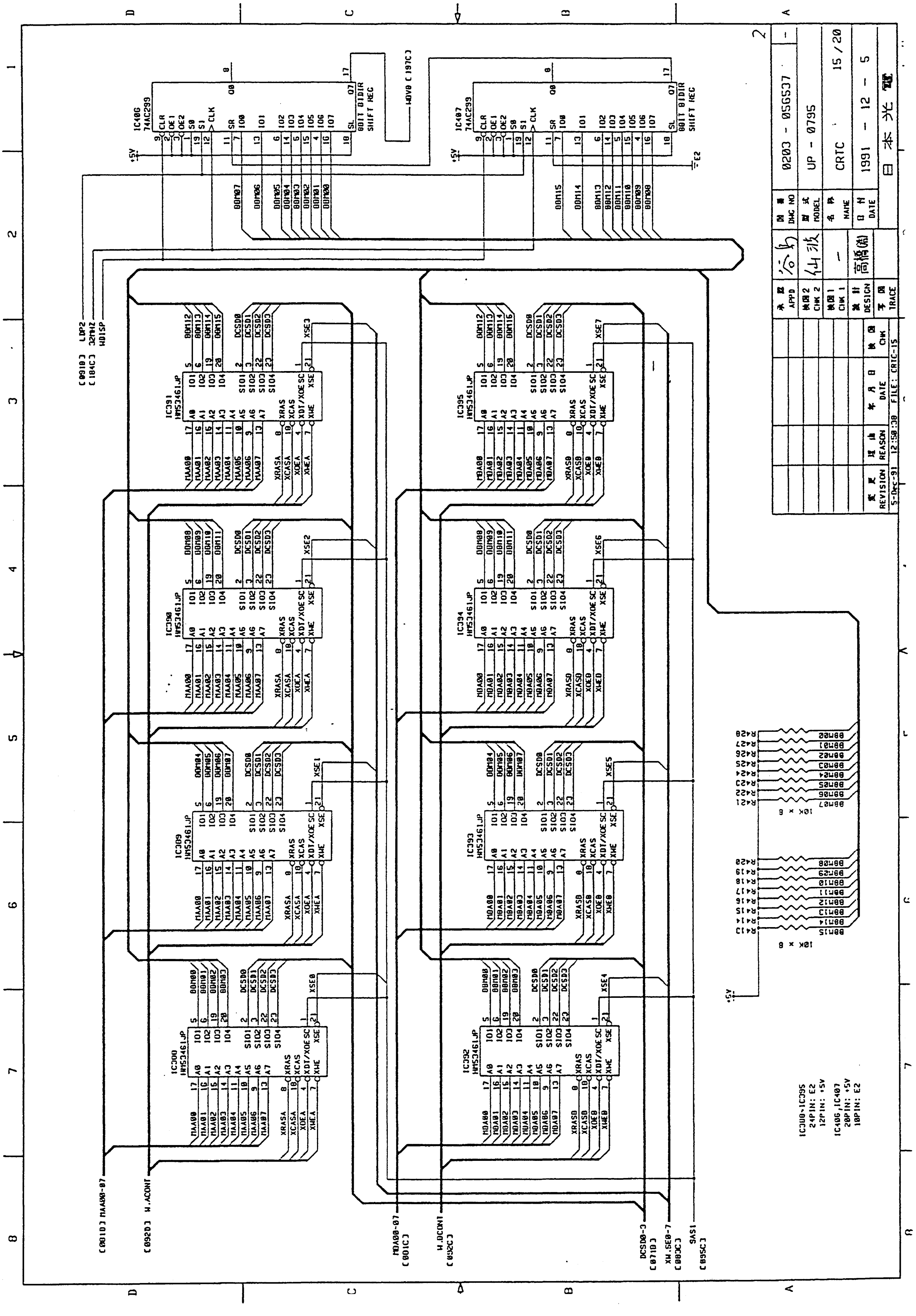
12. CIRCUIT DIAGRAM


IC400 74AC299 8BIT BIDIR SHIFT REG
IC401 74AC299 8BIT BIDIR SHIFT REG
IC364 HM53461JP
IC365 HM53461JP
IC366 HM53461JP
IC367 HM53461JP
IC368 HM53461JP
IC369 HM53461JP
IC370 HM53461JP
IC371 HM53461JP
HGVA [197D]
[091B] LDP1
[104C] X32MHZ
H01SP
[001D] MAA00-07
[092D] H.ACONT
MDA00-07 [001C]
H.DCONT [092C]
HOSD0-3 [071D]
XH.SE0-7 [003C]
SASB [095C]
10K x 8
IC364-IC371 24PIN: E2 12PIN: +5V
IC400,IC401 20PIN: +5V 10PIN: E2
0203 - 056501
UP - 0795
CRTC
12 / 20
1991 - 12 - 5
日本光電
5-Dec-91 11:50:07 FILE: CRTC-12

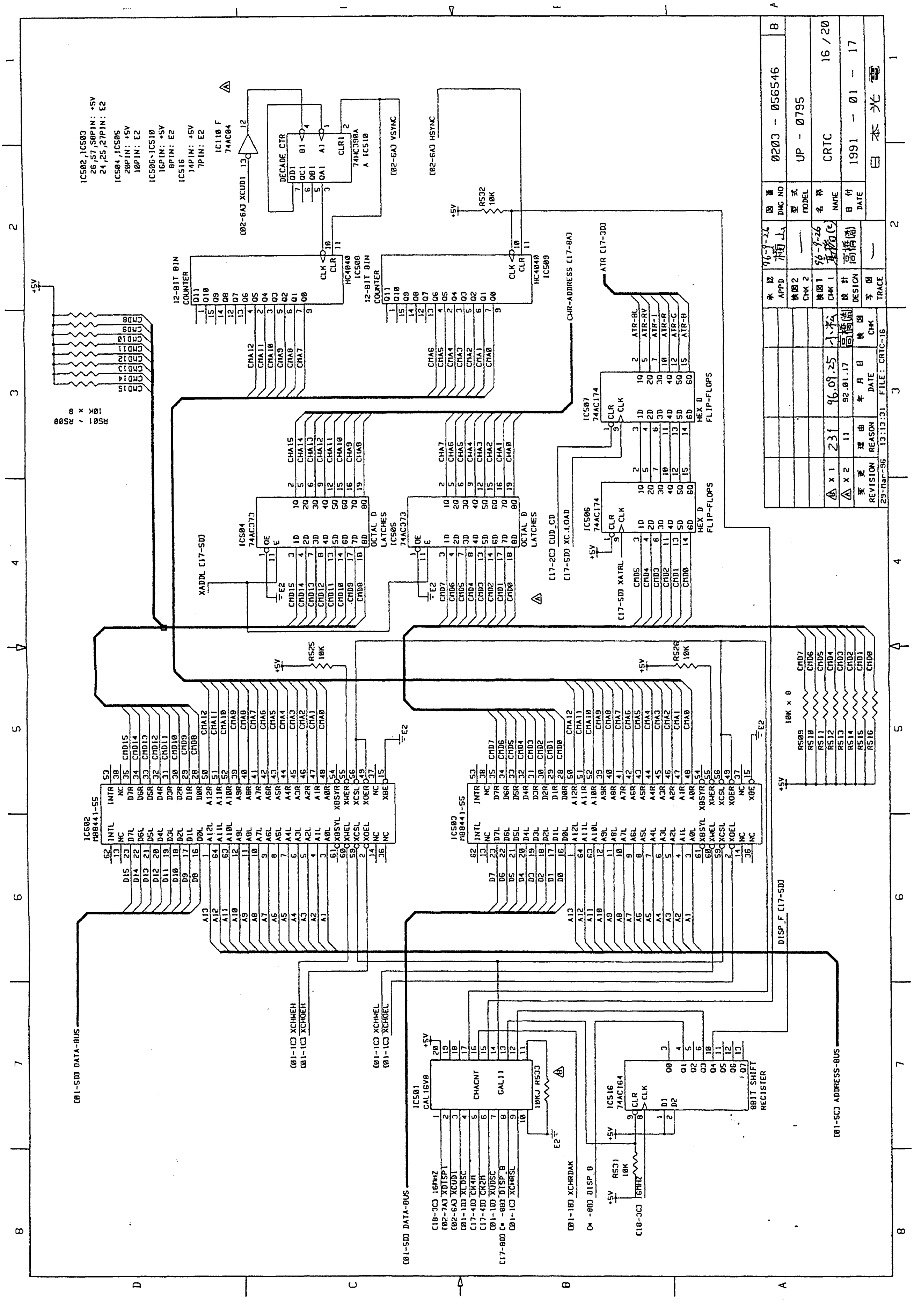

IC402
74AC299
8BIT DIDIR SHIFT REG
IC403
74AC299
8BIT DIDIR SHIFT REG
HCVD [197C]
LDP2 [091B]
32MHZ [104C]
HDISP
IC372 HM53461JP
IC373 HM53461JP
IC374 HM53461JP
IC375 HM53461JP
IC376 HM53461JP
IC377 HM53461JP
IC378 HM53461JP
IC379 HM53461JP
XSE0
XSE1
XSE2
XSE3
XSE4
XSE5
XSE6
XSE7
CDM00–CDM15
DOSD0–DOSD3
MAA00–MAA07
MDA00–MDA07
XRASA
XCASA
XOEA
XWEA
XRASB
XCASB
XOEB
XWEB
10K × 8
RC381–RC396
CBM00–CBM15
+5V
E2
[081D] MAA00-07
[092D] W.ACONT
MDA00-07 [081C]
W.DCONT [092C]
DOSD0-3 [071D]
XW.SE0-7 [080C]
SAS1 [095C]
IC372~IC379
24PIN: E2
12PIN: +5V
IC402,IC403
20PIN: +5V
10PIN: E2
図番 DWG NO 0203 - 056519
型式 MODEL UP-0795
名称 NAME CRTC 13/20
日付 DATE 1991 - 12 - 5
日本光電
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
手図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
5-Dec-91 11:54:48 FILE: CRTC-13

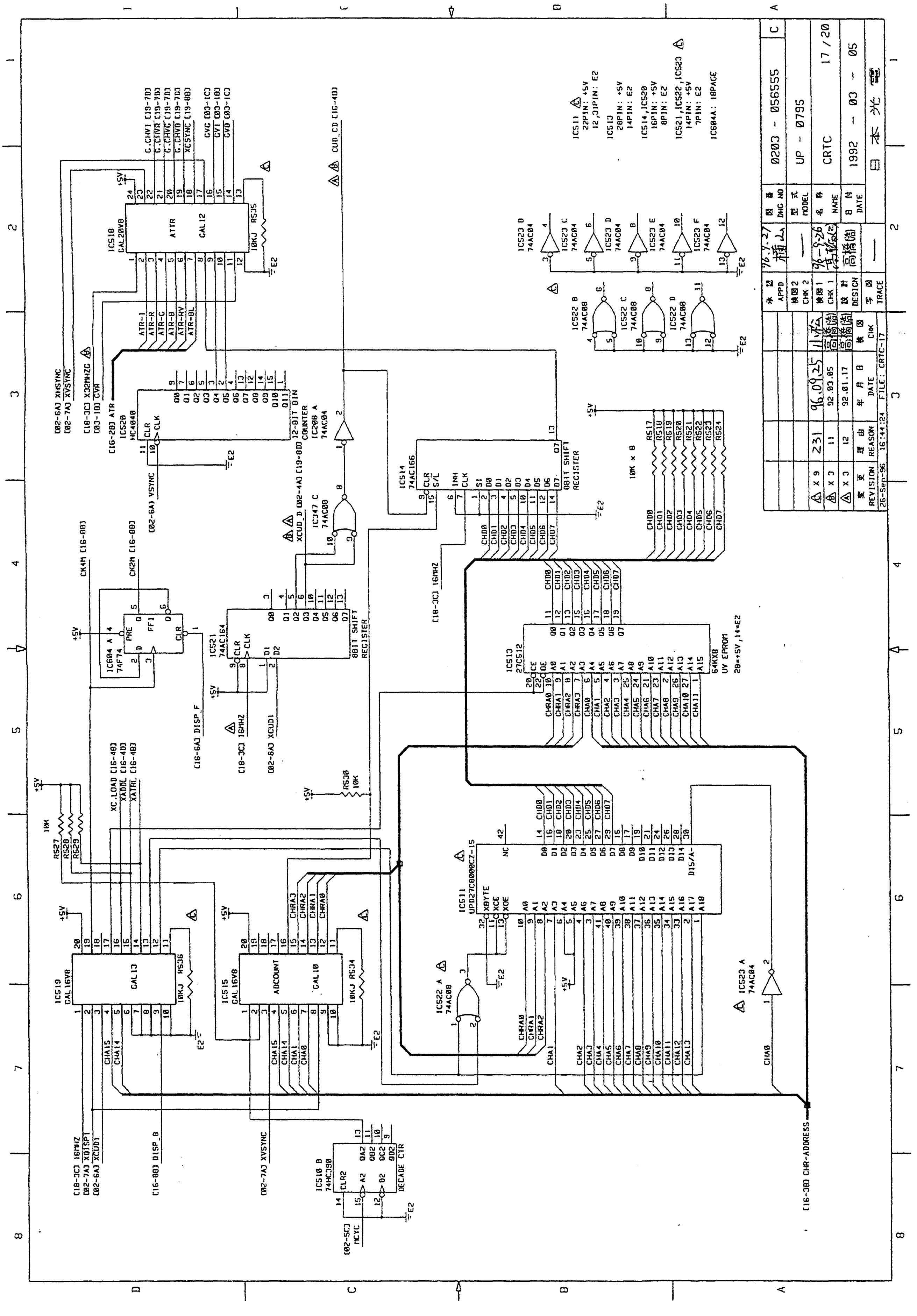
12. CIRCUIT DIAGRAM


IC404
74AC299
8BIT BIDIR SHIFT REG
IC405
74AC299
8BIT BIDIR SHIFT REG
HDVA [197D]
IC300
HM53461JP
IC301
HM53461JP
IC302
HM53461JP
IC303
HM53461JP
IC304
HM53461JP
IC305
HM53461JP
IC306
HM53461JP
IC307
HM53461JP
XSE0
XSE1
XSE2
XSE3
XSE4
XSE5
XSE6
XSE7
CSD0
CSD1
CSD2
CSD3
[091B] LDP1
[184C] X32MHZ
HDISP
[001D] MAA00-07
[092D] H.ACONT
MDA00-07 [081C]
H.DCONT [092C]
CSD0-3 [071D]
XH.SE0-7 [083C]
SAS0 [095C]
10K × 8
+5V
E2
IC300-IC307
24PIN: E2
12PIN: +5V
IC404,IC405
20PIN: +5V
10PIN: E2
0203 - 056528
UP - 0795
CRTC
14/20
1991 - 12 - 5
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
高橋
REVISION
REASON
DATE
CHK
5-Dec-91 11:59:49 FILE: CRTC-14
A
B
C
D
1
2
3
4
5
6
7
8

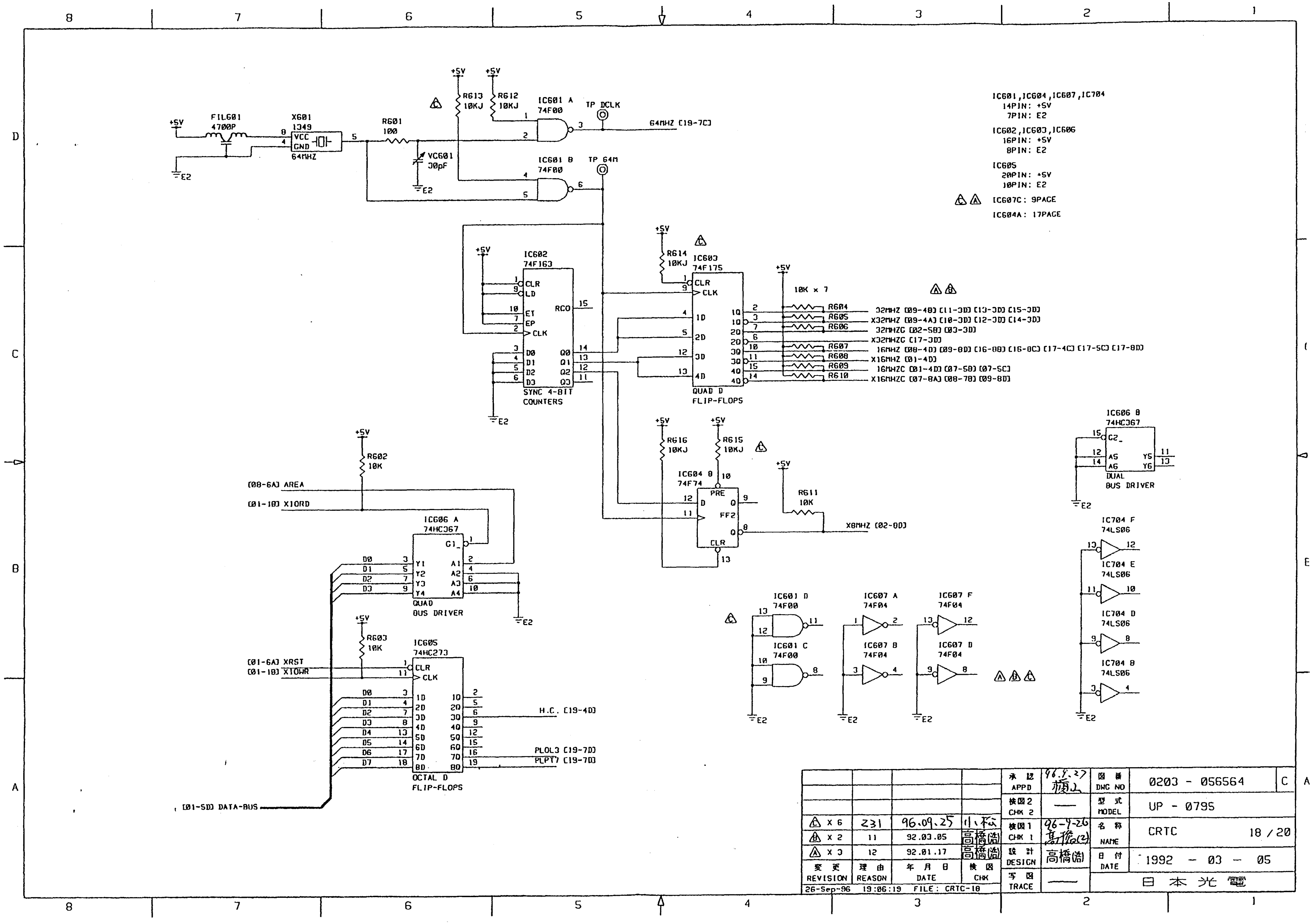

IC406 74AC299
IC407 74AC299
8BIT BIDIR SHIFT REG
IC300 HM53461JP
IC391 HM53461JP
IC390 HM53461JP
IC389 HM53461JP
IC392 HM53461JP
IC393 HM53461JP
IC394 HM53461JP
IC395 HM53461JP
HDVO [197C]
[0910] LDP2
[184C] 32MHZ
HDISP
[001D] MAA00-07
[092D] W.ACONT
MDA00-07 [001C]
W.DCON1 [052C]
DCSD0-3 [071B]
XW.SE0-7 [080C]
SAS1 [095C]
10K × 8
IC300-IC395 24PIN: E2 12PIN: +5V
IC406,IC407 20PIN: +5V 10PIN: E2
0203 - 05G537
UP - 0795
CRTC
15 / 20
1991 - 12 - 5
5-Dec-91 12:58:38 FILE: CRTC-15

12. CIRCUIT DIAGRAM

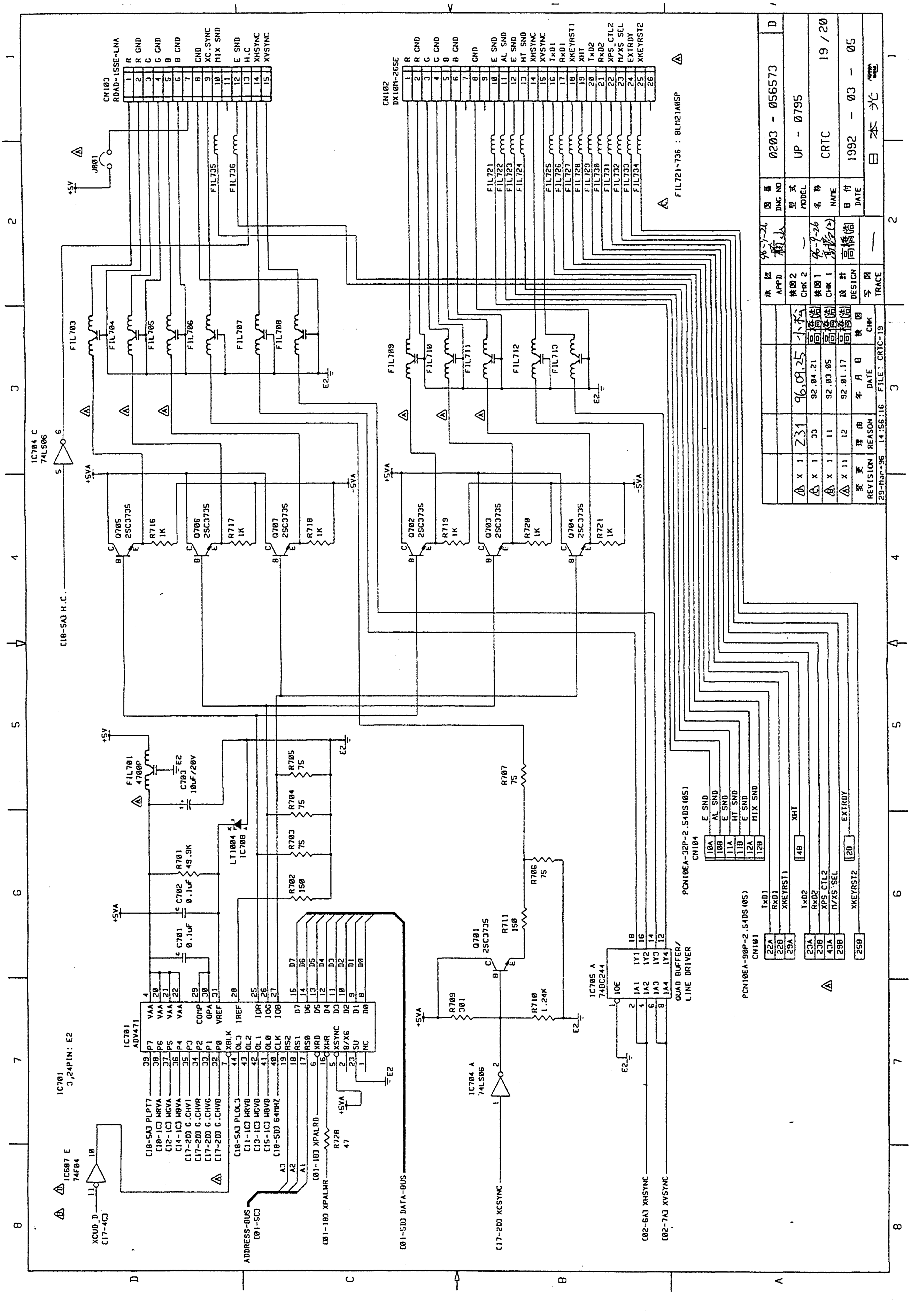

0203 - 056546
UP - 0795
CRTC
16 / 20
1991 - 01 - 17
日本光電
FILE: CRTC-16
IC502 MB8441-55
IC503 MB8441-55
IC504 74AC373
IC505 74AC373
IC506 74AC174
IC507 74AC174
IC508 HC4040
IC509 HC4040
IC510 74HC390A
IC110 F 74AC04
IC501 GAL16V8
IC516 74AC164
12-BIT BIN COUNTER
OCTAL D LATCHES
HEX D FLIP-FLOPS
DECADE CTR
8BIT SHIFT REGISTER
RS01 - RS08 10K x 8
RS09 - RS16 10K x 8
R525 10K
R526 10K
R531 10K
R532 10K
R533 10K
(01-5D) DATA-BUS
(01-5C) ADDRESS-BUS
(02-6A) VSYNC
(02-6A) HSYNC
(02-6A) XCUD1
CHR-ADDRESS (17-8A)
ATR (17-3D)
XADDL (17-5D)
(17-2C) CUD_CD
(17-5D) XC.LOAD
(17-5D) XATRL
DISP_F (17-5D)
(01-1C) XCHWEH
(01-1C) XCHOEH
(01-1C) XCHWEL
(01-1C) XCHOEL
(01-1B) XCHRDAK
DISP 0


0203 - 056555
C
UP - 0795
CRTC
17 / 20
1992 - 03 - 05
日本光電
IC511 22PIN: +5V 12,31PIN: E2
IC513 28PIN: +5V 14PIN: E2
IC514,IC520 16PIN: +5V 8PIN: E2
IC521,IC522,IC523 14PIN: +5V 7PIN: E2
IC604A: 18PAGE
IC518 GAL20V8 ATTR GAL12
IC520 HC4040 12-BIT BIN COUNTER
IC208 A 74AC04
IC514 74AC166 8BIT SHIFT REGISTER
IC521 74AC164 8BIT SHIFT REGISTER
IC347 C 74AC08
IC604 A 74F74 FF1
IC513 27C512 64KX8 UV EPROM 28=+5V,14=E2
IC511 UPD27C8000CZ-15
IC519 GAL16V8 GAL13
IC515 GAL16V8 ADCOUNT GAL10
IC510 B 74HC390 DECADE CTR
IC522 A 74AC08
IC522 B 74AC08
IC522 C 74AC08
IC522 D 74AC08
IC523 A 74AC04
IC523 B 74AC04
IC523 C 74AC04
IC523 D 74AC04
IC523 E 74AC04
IC523 F 74AC04
R517 R518 R519 R520 R521 R522 R523 R524 10K x 8
R527 R528 R529 10K
R530 10K
R534 10KJ
R535 10KJ
R536 10KJ
[16-3B] CHR-ADDRESS
CUD_CD [16-4D]
XCUD_D [02-4A]
[16-2B] ATR
[18-3C] X32MHZG
[03-1D] CVR
[02-6A] XHSYNC
[02-7A] XVSYNC
[02-6A] VSYNC
[16-6A] DISP_F
[18-3C] 16MHZ
[02-6A] XCUD1
XC.LOAD [16-4B]
XADDL [16-4D]
XATRL [16-4B]
CK4H [16-8B]
CK2H [16-8B]
[16-8B] DISP_B
[02-7A] XVSYNC
[02-5C] NCYC
[02-7A] XDISP1
G.CHV1 [19-7D]
G.CHVR [19-7D]
G.CHVC [19-7D]
G.CHVB [19-7D]
XCSYNC [19-8B]
CVC [03-1C]
CV1 [03-1B]
CV0 [03-1C]
ATR-1 ATR-R ATR-C ATR-B ATR-HV ATR-BL
CHD0 CHD1 CHD2 CHD3 CHD4 CHD5 CHD6 CHD7
CHRA0 CHRA1 CHRA2 CHRA3
CHA0 CHA1 CHA2 CHA3 CHA4 CHA5 CHA6 CHA7 CHA8 CHA9 CHA10 CHA11 CHA12 CHA13 CHA14 CHA15
+5V
E2
REVISION
REASON
DATE
26-Sep-96 16:44:24 FILE: CRTC-17
92.01.17
92.03.05
96.09.25
DESIGN
TRACE
APPD
CHK 1
CHK 2
DWG NO
MODEL
NAME
A B C D
1 2 3 4 5 6 7 8

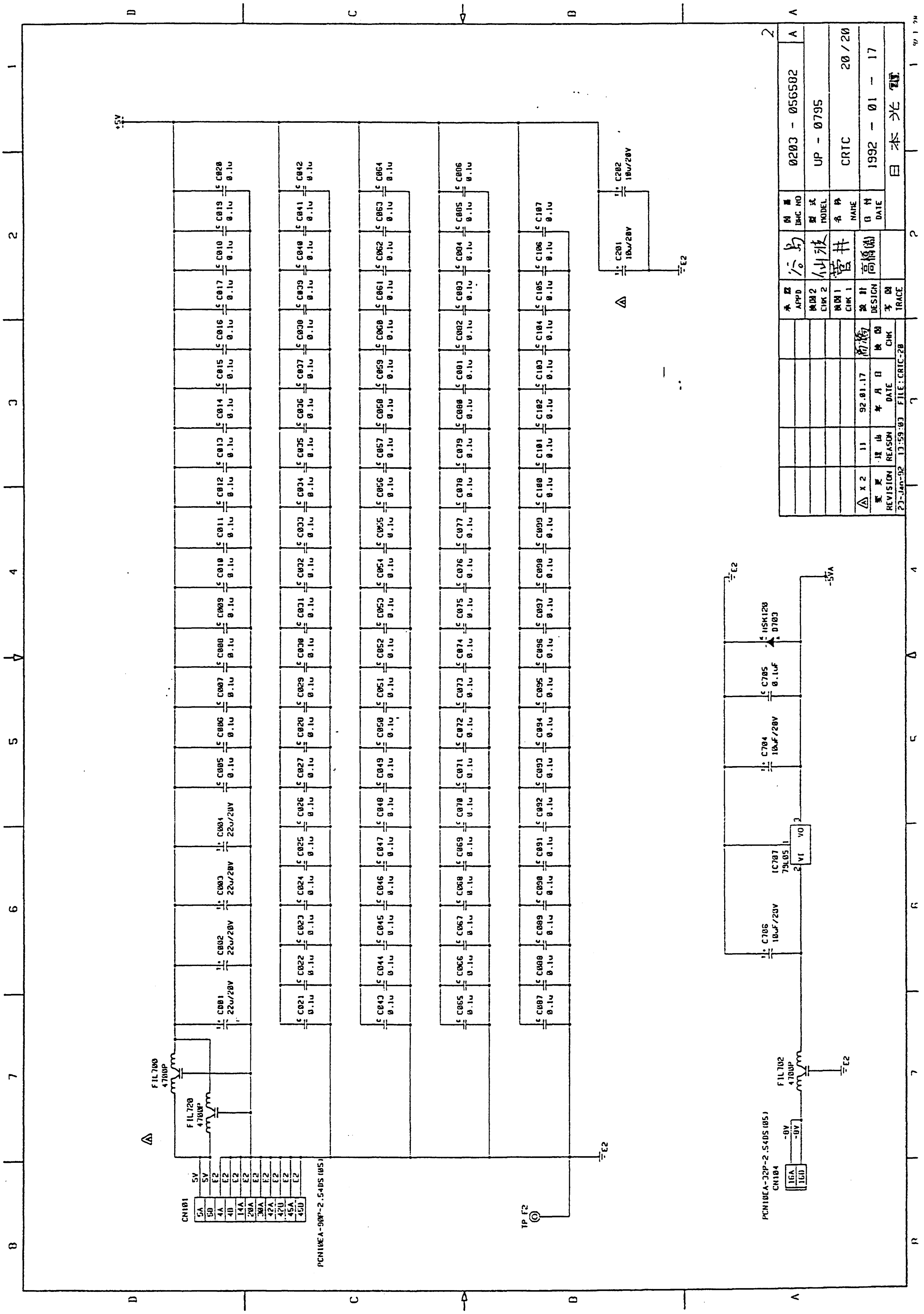
12. CIRCUIT DIAGRAM

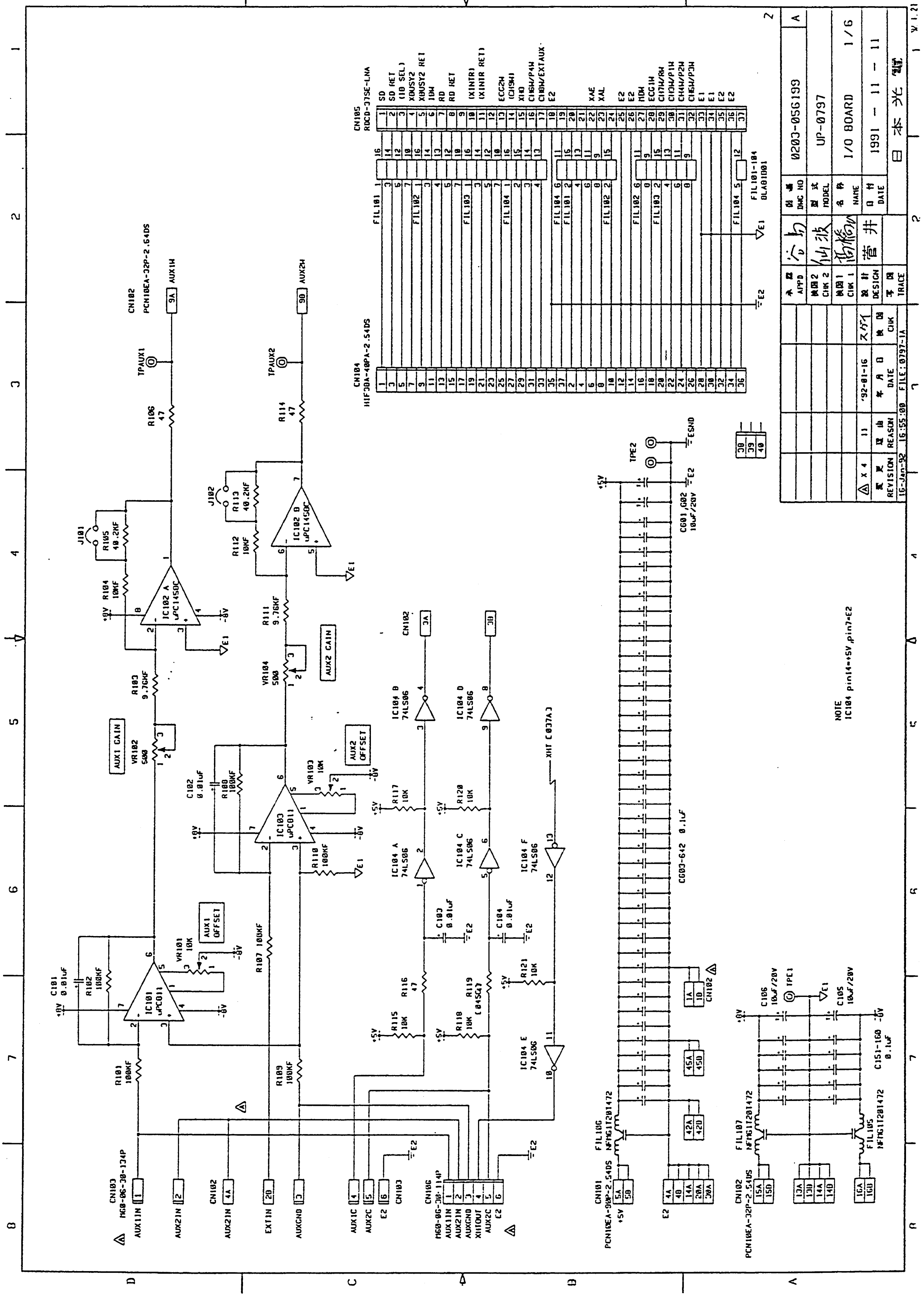


IC601,IC604,IC607,IC704
14PIN: +5V
7PIN: E2
IC602,IC603,IC606
16PIN: +5V
8PIN: E2
IC605
20PIN: +5V
10PIN: E2
IC607C: 9PAGE
IC604A: 17PAGE
FIL601 4700P
X601 1349 VCC GND 64MHZ
R601 100
VC601 30pF
R613 10KJ
R612 10KJ
IC601 A 74F00
IC601 B 74F00
TP DCLK
TP 64M
64MHZ [19-7C]
IC602 74F163 CLR LD ET EP CLK RCO D0 D1 D2 D3 Q0 Q1 Q2 Q3
SYNC 4-BIT COUNTERS
R614 10KJ
IC603 74F175 CLR CLK 1D 2D 3D 4D 1Q 2Q 3Q 4Q
QUAD D FLIP-FLOPS
10K × 7
R604
R605
R606
R607
R608
R609
R610
32MHZ [09-4B] [11-3D] [13-3D] [15-3D]
X32MHZ [09-4A] [10-3D] [12-3D] [14-3D]
32MHZC [02-5B] [03-3D]
X32MHZC [17-3D]
16MHZ [08-4D] [09-8D] [16-8B] [16-8C] [17-4C] [17-5C] [17-8D]
X16MHZ [01-4D]
16MHZC [01-4D] [07-5B] [07-5C]
X16MHZC [07-8A] [08-7B] [09-8D]
R616 10KJ
R615 10KJ
IC604 B 74F74 PRE D FF2 CLR Q
R611 10K
X8MHZ [02-0D]
IC606 B 74HC367 G2_ A5 A6 Y5 Y6
DUAL BUS DRIVER
R602 10K
[08-6A] AREA
[01-1B] XIORD
IC606 A 74HC367 G1_ Y1 Y2 Y3 Y4 A1 A2 A3 A4
QUAD BUS DRIVER
D0 D1 D2 D3
R603 10K
[01-6A] XRST
[01-1B] XIOWR
IC605 74HC273 CLR CLK 1D 2D 3D 4D 5D 6D 7D 8D 1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
OCTAL D FLIP-FLOPS
D0 D1 D2 D3 D4 D5 D6 D7
H.C. [19-4D]
PLOL3 [19-7D]
PLPT7 [19-7D]
[01-5D] DATA-BUS
IC601 D 74F00
IC601 C 74F00
IC607 A 74F04
IC607 B 74F04
IC607 F 74F04
IC607 D 74F04
IC704 F 74LS06
IC704 E 74LS06
IC704 D 74LS06
IC704 B 74LS06
+5V
E2
C × 6 | 231 | 96.09.25 | 小松
B × 2 | 11 | 92.03.05 | 高橋(浩)
A × 3 | 12 | 92.01.17 | 高橋(浩)
変更 REVISION | 理由 REASON | 年月日 DATE | 検図 CHK
26-Sep-96 19:06:19 FILE: CRTC-18
承認 APPD 96.9.27 楯山
検図2 CHK 2 —
検図1 CHK 1 96-9-26 高橋(2)
設計 DESIGN 高橋(浩)
写図 TRACE —
図番 DWG NO 0203 - 056564 C
型式 MODEL UP - 0795
名称 NAME CRTC 18 / 20
日付 DATE 1992 - 03 - 05
日本光電

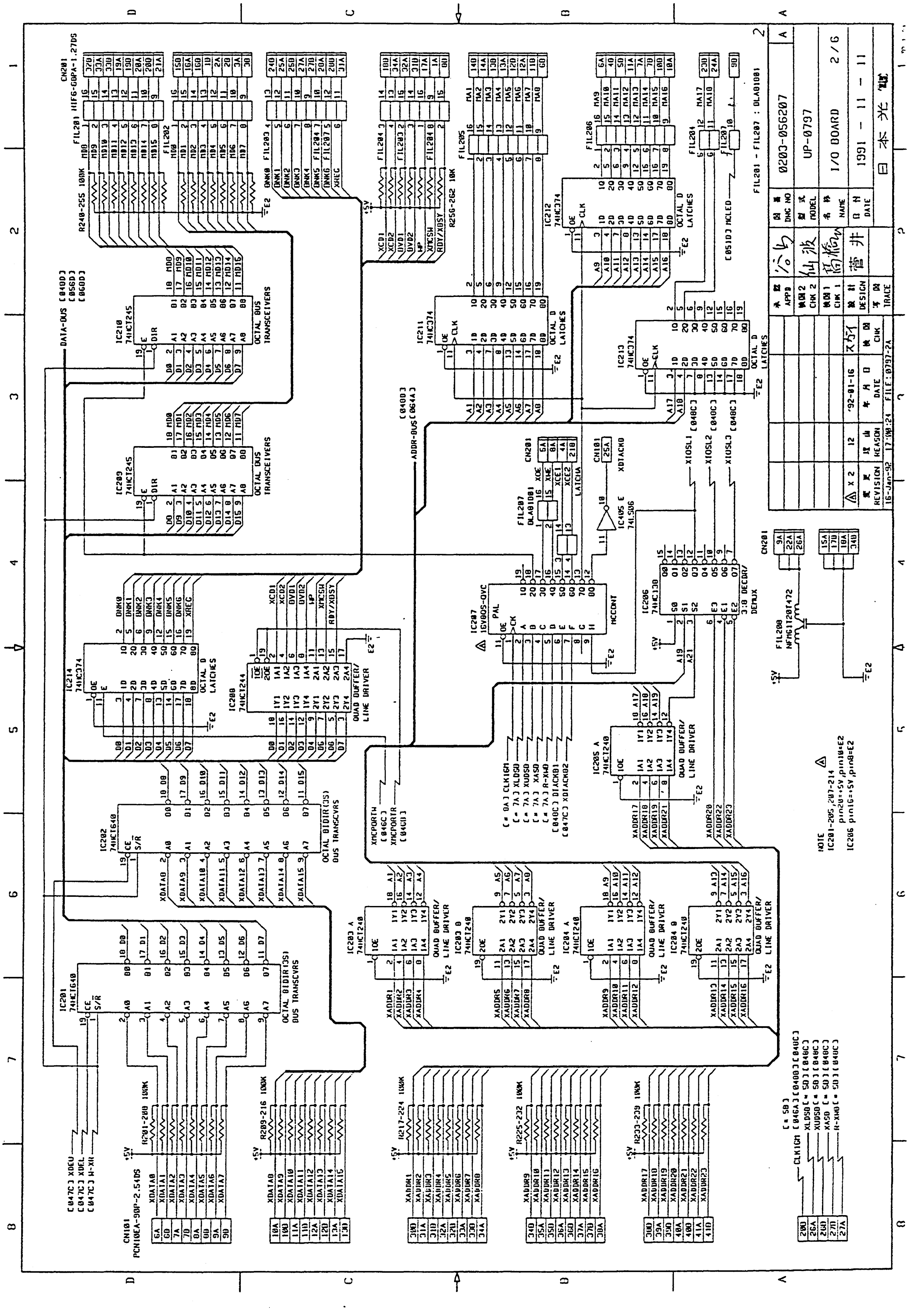

CN103 RDAD-15SE-LNA
CN102 DX10M-26SE
R
R GND
G
G GND
B
B GND
GND
XC.SYNC
MIX SND
E SND
H.C
XHSYNC
XVSYNC
AL SND
HT SND
TxD1
RxD1
XKEYRST1
XHT
TxD2
RxD2
XPS CTL2
M/XS SEL
EXTRDY
XKEYRST2
J801
+5V
FIL735
FIL736
FIL721-736 : BLM21A05P
FIL721
FIL722
FIL723
FIL724
FIL725
FIL726
FIL727
FIL728
FIL729
FIL730
FIL731
FIL732
FIL733
FIL734
FIL703
FIL704
FIL705
FIL706
FIL707
FIL708
FIL709
FIL710
FIL711
FIL712
FIL713
E2
IC704 C
74LS06
[18-5A] H.C.
+5VA
-5VA
Q705 2SC3735
Q706 2SC3735
Q707 2SC3735
Q702 2SC3735
Q703 2SC3735
Q704 2SC3735
R716 1K
R717 1K
R718 1K
R719 1K
R720 1K
R721 1K
FIL701 4700P
C703 10uF/20V
C702 0.1uF
C701 0.1uF
R701 49.9K
LT1004 IC708
R702 150
R703 75
R704 75
R705 75
R706 75
R707 75
R711 150
R709 301
R710 1.24K
Q701 2SC3735
IC704 A 74LS06
IC701 ADV471
IC701 3,24PIN: E2
VAA
COMP
OPA
VREF
IREF
IOR
IOG
IOB
P7
P6
P5
P4
P3
P2
P1
P0
XBLK
OL3
OL2
OL1
OL0
CLK
RS2
RS1
RS0
XRD
XWR
XSYNC
8/X6
SU
NC
D7
D6
D5
D4
D3
D2
D1
D0
[18-5A] PLPT7
[10-1C] WRVA
[12-1C] WGVA
[14-1C] WBVA
[17-2D] C.CHV1
[17-2D] C.CHVG
[17-2D] C.CHV0
[18-5A] PLOL3
[11-1C] WRV0
[13-1C] WGV0
[15-1C] WBV0
[18-5D] 64MHZ
A3
A2
A1
[01-18] XPALRD
R728 47
IC607 E 74F04
XCUD_D [17-4C]
ADDRESS-BUS [01-5C]
[01-18] XPALWR
[01-5D] DATA-BUS
[17-2D] XCSYNC
IC705 A 74BC244
QUAD BUFFER/ LINE DRIVER
1OE
1A1
1A2
1A3
1A4
1Y1
1Y2
1Y3
1Y4
[02-6A] XHSYNC
[02-7A] XVSYNC
PCN10EA-32P-2.54DS(05) CN104
10A
10B
11A
11B
12A
12B
PCN10EA-90P-2.54DS(05) CN101
22A
22B
29A
23A
23B
43A
29B
25B
14B
28B
0203 - 056573
D
UP - 0795
CRTC
19 / 20
1992 - 03 - 05
日本光電
図番 DWG NO
型式 MODEL
名称 NAME
日付 DATE
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
検図 CHK
96-9-26
96-9-26
年月日 DATE
理由 REASON
変更 REVISION
231
33
11
12
96.09.25
92.04.21
92.03.05
92.01.17
FILE: CRTC-19
14:56:16
29-Mar-96
A
B
C
D
1
2
3
4
5
6
7
8

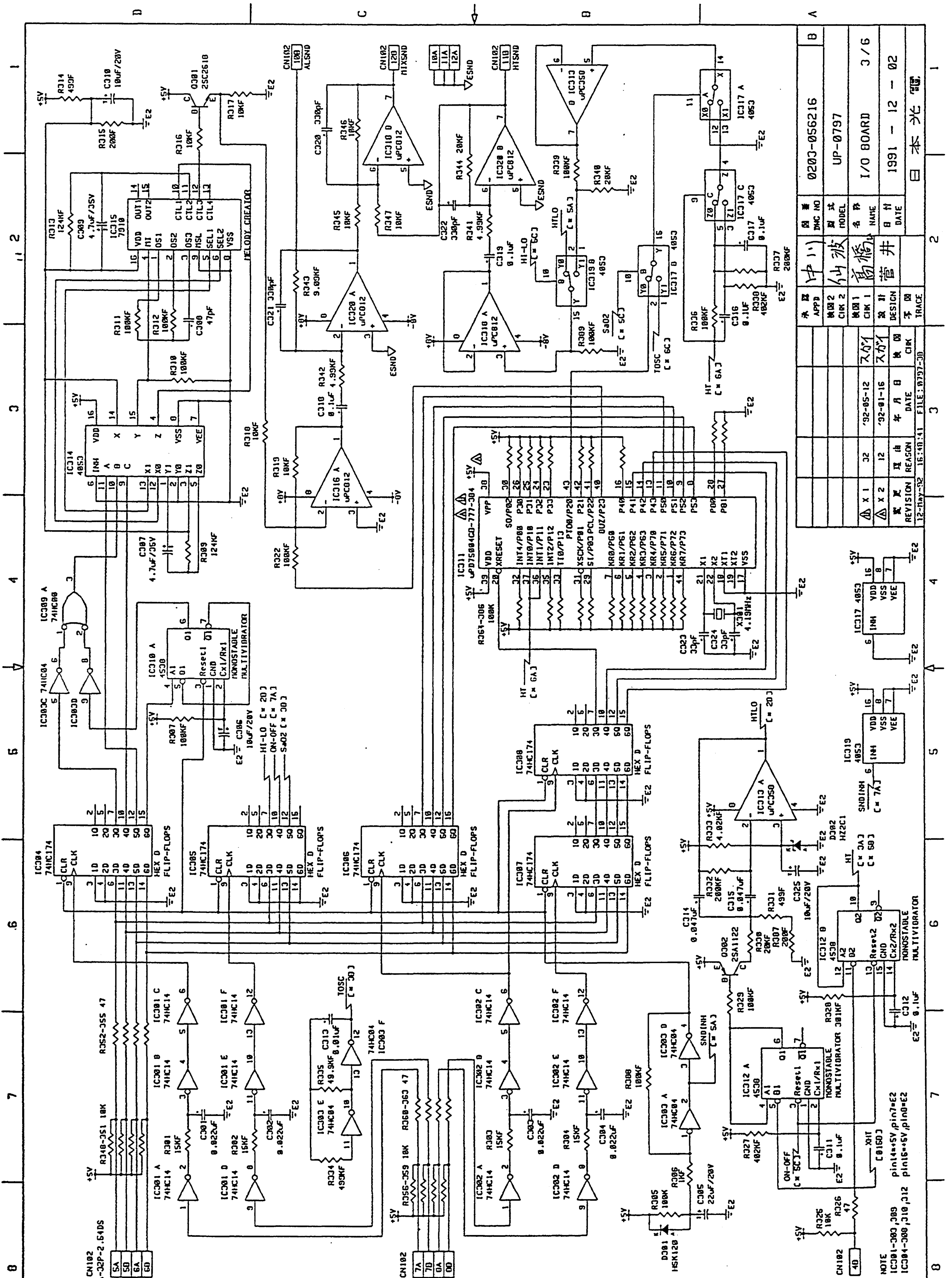
12. CIRCUIT DIAGRAM


+5V
C001 22u/20V
C002 22u/20V
C003 22u/20V
C004 22u/20V
C005 0.1u
C006 0.1u
C007 0.1u
C008 0.1u
C009 0.1u
C010 0.1u
C011 0.1u
C012 0.1u
C013 0.1u
C014 0.1u
C015 0.1u
C016 0.1u
C017 0.1u
C018 0.1u
C019 0.1u
C020 0.1u
C021 0.1u … C042 0.1u
C043 0.1u … C064 0.1u
C065 0.1u … C086 0.1u
C087 0.1u … C107 0.1u
C201 10u/20V
C202 10u/20V
FIL700 470UP
FIL720 470UP
FIL702 470UP
CN101
PCN10EA-90P-2.54DS(05)
5A 5V
5D 5V
4A E2
4D E2
14A E2
20A E2
30A E2
42A E2
42D E2
45A E2
45D E2
TP F2
E2
-5VA
11SK120 D703
C705 0.1uF
C704 10uF/20V
IC707 79L05
VI VO
C706 10uF/20V
CN104
PCN10EA-32P-2.54DS(05)
16A -8V
16D -8V
0203 - 056502
UP - 0795
CRTC
20/20
1992 - 01 - 17
日本光電
DWG NO
MODEL
NAME
DATE
APP'D
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
92.01.17
23-Jan-92 13:59:03
FILE:CRTC-20
A B C D
1 2 3 4 5 6 7 8

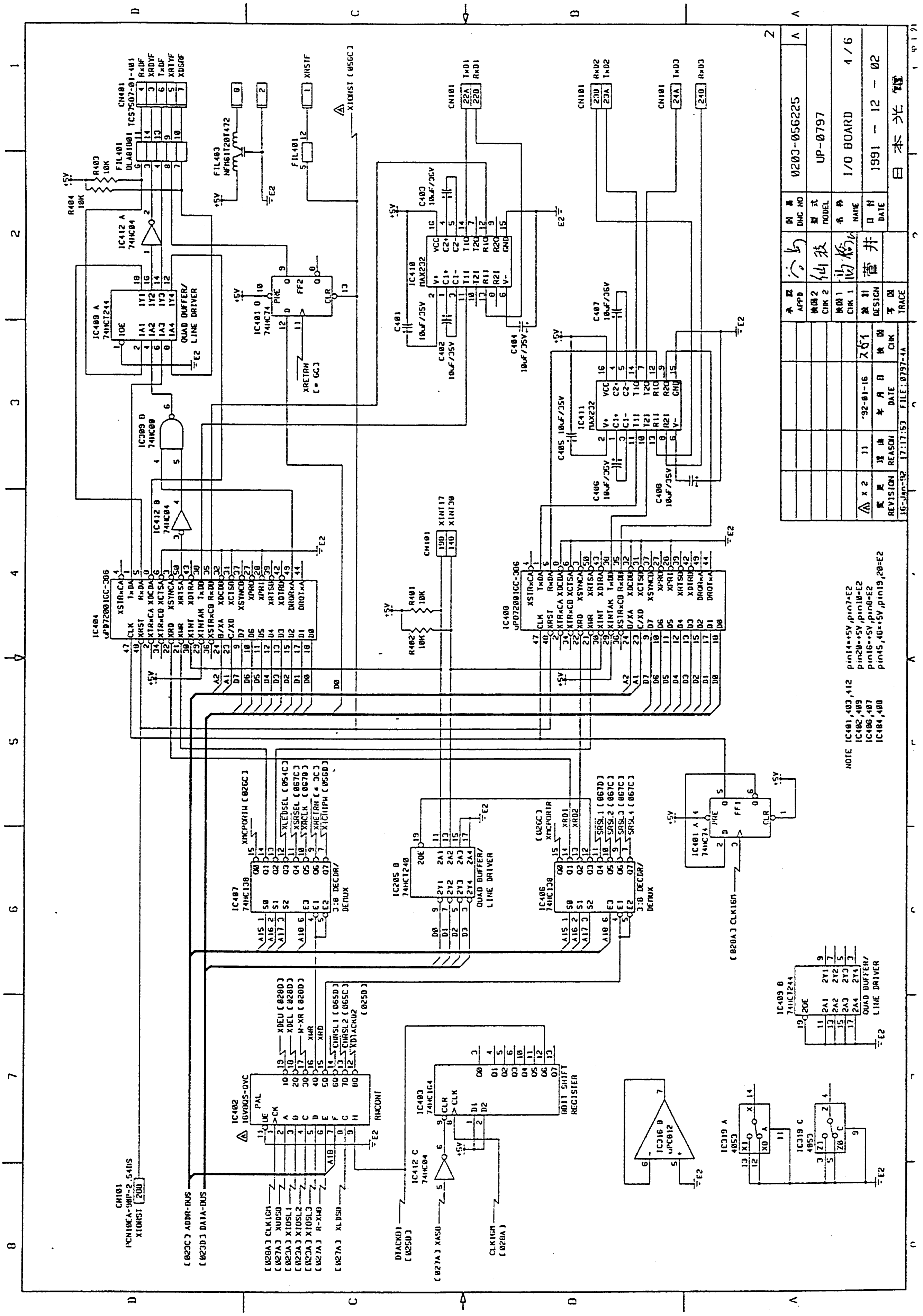

0203-05G199
UP-0797
I/O BOARD
1/6
1991 - 11 - 11
APPD
CHK 2
CHK 1
DESIGN
TRACE
DWG NO
MODEL
NAME
DATE
REVISION
REASON
DATE
CHK
'92-01-16
16-Jan-92 16:55:00 FILE:0797-1A
CN105
RDCD-37SE-LNA
CN104
HIF3DA-40PA-2.54DS
CN102
PCN10EA-32P-2.54DS
AUX1W
AUX2W
TPAUX1
TPAUX2
R106 47
R114 47
J101
J102
R105 40.2KF
R113 40.2KF
R104 10KF
R112 10KF
IC102 A uPC1450C
IC102 B uPC1450C
R103 9.76KF
R111 9.76KF
VR102 500
VR104 500
AUX1 GAIN
AUX2 GAIN
AUX1 OFFSET
AUX2 OFFSET
VR101 10K
VR103 10K
IC101 uPC811
IC103 uPC811
C101 0.01uF
C102 0.01uF
R102 100KF
R100 100KF
R101 100KF
R107 100KF
R109 100KF
R110 100KF
IC104 A 74LS06
IC104 B 74LS06
IC104 C 74LS06
IC104 D 74LS06
IC104 E 74LS06
IC104 F 74LS06
R115 10K
R116 47
R117 10K
R118 10K
R119
R120 10K
R121 10K
C103 0.01uF
C104 0.01uF
XHT
CG01,G02 10uF/20V
CG03-642 0.1uF
TPE2
ESND
NOTE
IC104 pin14=+5V,pin7=E2
FIL101-104
DLA01001
FIL106 NFM61T201472
FIL107 NFM61T201472
FIL105 NFM61T201472
C106 10uF/20V
C105 10uF/20V
TPE1
C151-160 0.1uF
CN103
MG0-06-30-134P
AUX1IN
AUX2IN
EXTIN
AUXGND
AUX1C
AUX2C
CN106
MG0-06-30-114P
XHTOUT
CN101
PCN10EA-90P-2.54DS
+5V
E2
E1
-8V
+8V

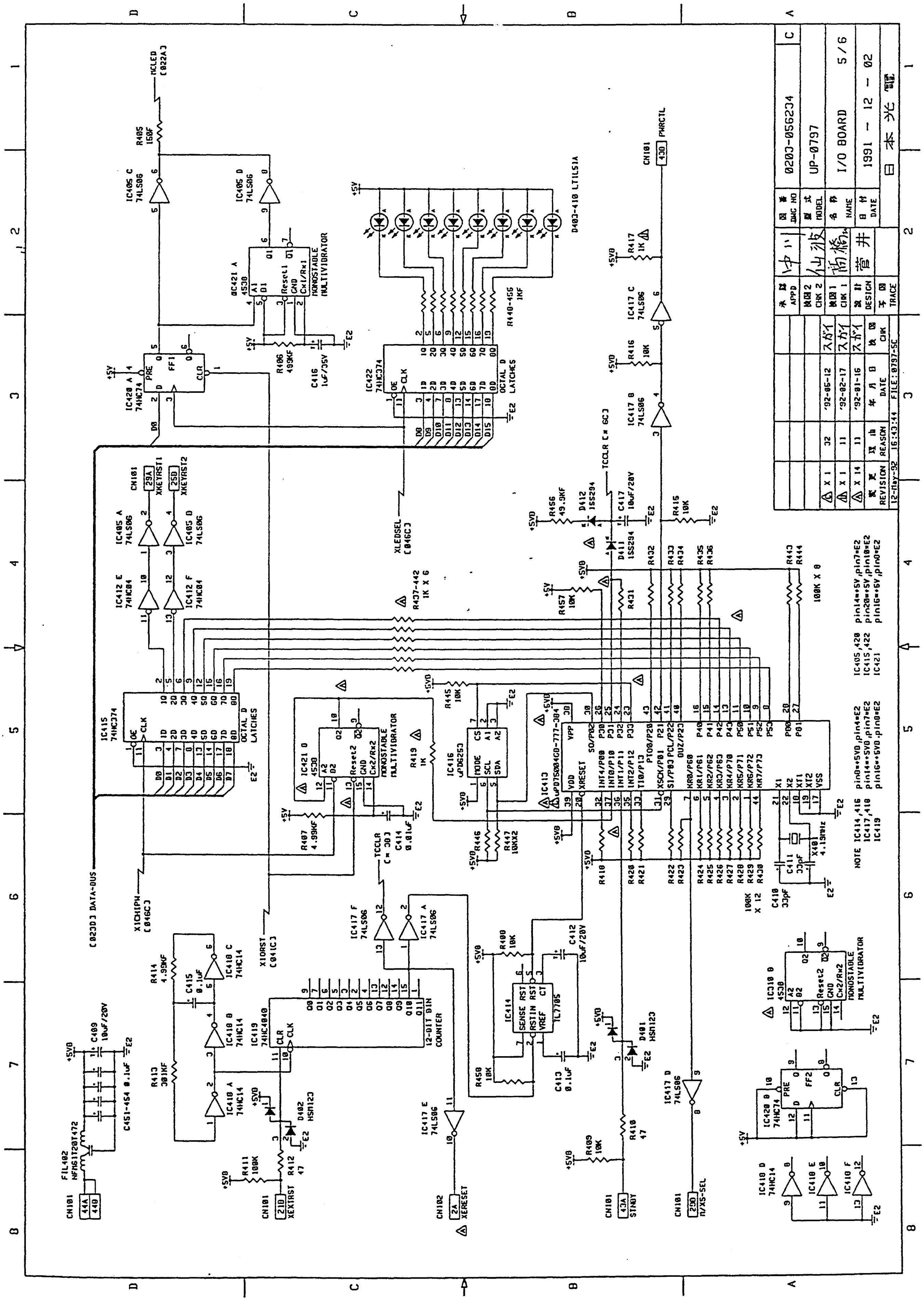
12. CIRCUIT DIAGRAM


0203-056207
UP-0797
I/O BOARD 2/6
1991 - 11 - 11
FIL201 - FIL207 : DLA8108I
DATA-BUS
ADDR-BUS
IC201 74HCT640
IC202 74HCT640
IC203 A 74HCT240
IC203 B 74HCT240
IC204 A 74HCT240
IC204 B 74HCT240
IC205 A 74HCT240
IC206 74HC138
IC207 15V80S-QVC
IC208 74HC244
IC209 74HCT245
IC210 74HCT245
IC211 74HC374
IC212 74HC374
IC213 74HC374
IC214 74HC374
CN101 PCN10EA-90P-2.54DS
CN201 HIF6-60PA-1.27DS

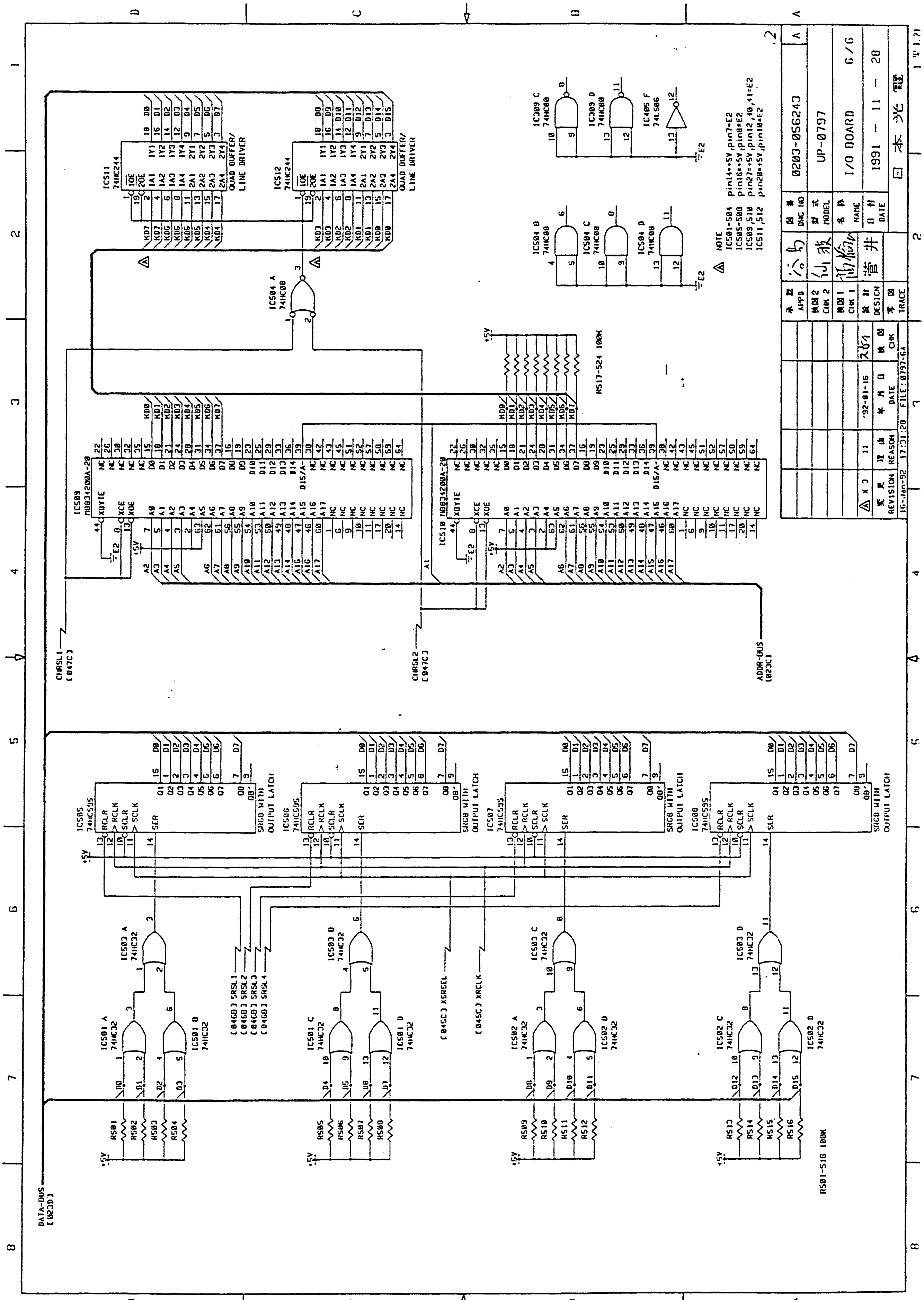

0203-056216
UP-0797
I/O BOARD
3/6
1991 - 12 - 02
日本光電
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
12-May-92
16:10:41
FILE: 0797-30
'92-05-12
'92-01-16
MELODY CREATOR
IC315 7910
IC314 4053
IC311 uPD7508HCD-777-304
IC304 74HC174 HEX D FLIP-FLOPS
IC305 74HC174 HEX D FLIP-FLOPS
IC306 74HC174 HEX D FLIP-FLOPS
IC307 74HC174 HEX D FLIP-FLOPS
IC308 74HC174 HEX D FLIP-FLOPS
IC310 A 4538 MONOSTABLE MULTIVIBRATOR
IC312 A 4538 MONOSTABLE MULTIVIBRATOR
IC312 B 4538 MONOSTABLE MULTIVIBRATOR
IC309 A 74HC08
IC313 A uPC358
IC313 B uPC358
IC316 A uPC812
IC320 A uPC812
IC320 B uPC812
IC310 D uPC812
IC318 A uPC812
IC317 A 4053
IC317 B 4053
IC317 C 4053
IC319 B 4053
Q301 2SC2610
Q302 2SA1122
X301 4.19MHz
CN102 PCN10EA-32P-2.54DS
OUT00
OUT01
OUT02
OUT03
SL0
SL1
SL2
SL3
NOTE
IC301-303,309 pin14=+5V,pin7=E2
IC304-308,310,312 pin16=+5V,pin8=E2

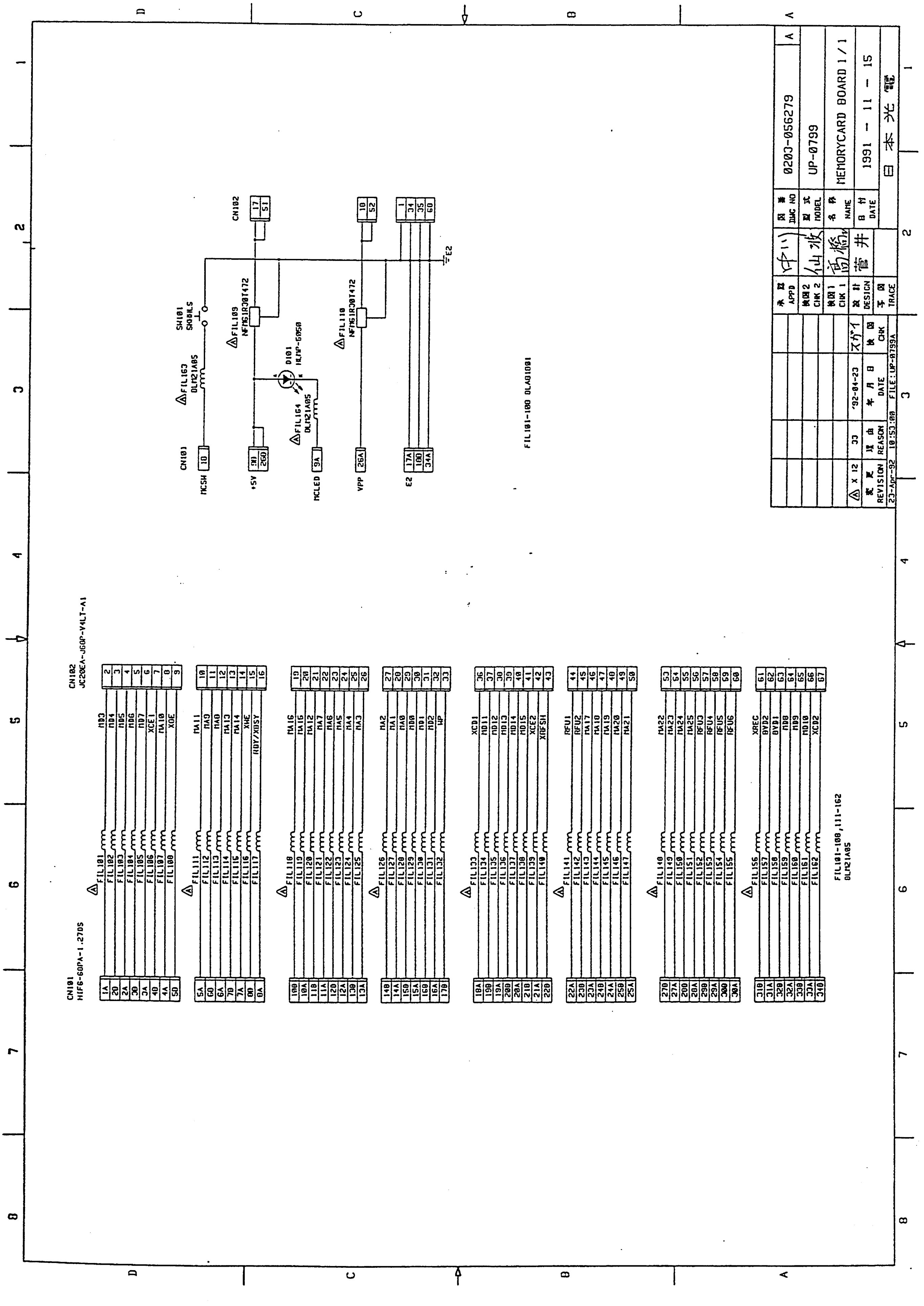
12. CIRCUIT DIAGRAM


0203-056225
UP-0797
I/O BOARD
4/6
1991 - 12 - 02
IC404 uPD72001GC-306
IC408 uPD72001GC-306
IC410 MAX232
IC411 MAX232
IC402 16V8QS-0VC PAL
IC407 74HC138 3:8 DECDR/DEMUX
IC406 74HC138 3:8 DECDR/DEMUX
IC205 B 74HC1240 QUAD BUFFER/LINE DRIVER
IC409 A 74HC1244 QUAD BUFFER/LINE DRIVER
IC409 B 74HC1244 QUAD BUFFER/LINE DRIVER
IC403 74HC164 8BIT SHIFT REGISTER
IC401 A 74HC74
IC401 D 74HC74
IC412 A 74HC04
IC412 B 74HC04
IC412 C 74HC04
IC309 D 74HC00
IC316 D uPC812
IC319 A 4053
IC319 C 4053
CN101 PCN10EA-96P-2.54DS
CN401 TCS7507-01-401
FIL401 DLA81001
FIL403 NFM61T20T472
ADDR-BUS
DATA-BUS
NOTE IC401,403,412 pin14=+5V,pin7=E2
IC402,409 pin20=+5V,pin10=E2
IC406,407 pin16=+5V,pin8=E2
IC404,408 pin15,40=+5V,pin19,20=E2
'92-01-16
16-Jan-92 17:17:53 FILE:0797-4A

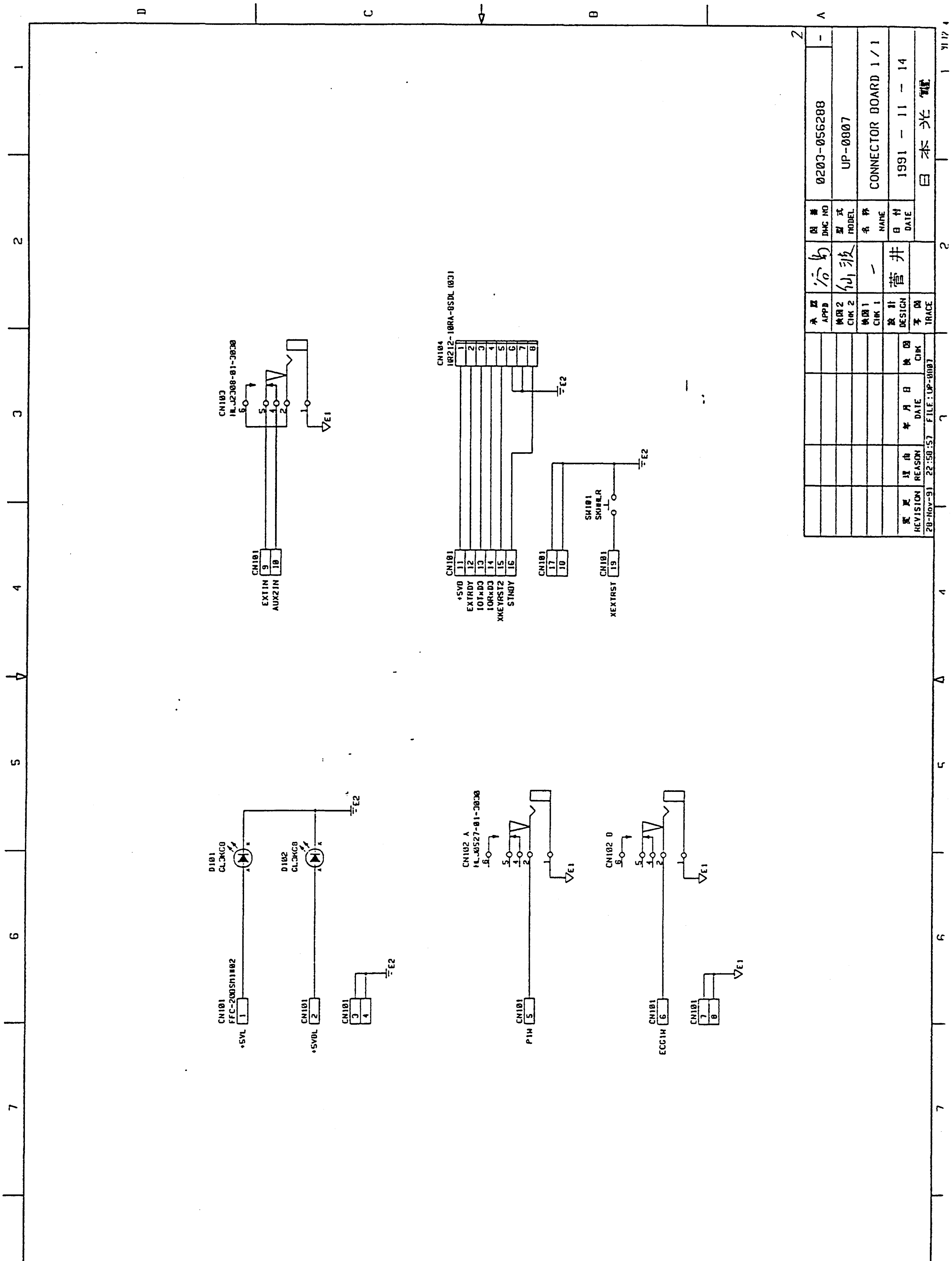

0203-056234
UP-0797
I/O BOARD 5/6
1991 - 12 - 02
IC415 74HC374 OCTAL D LATCHES
IC422 74HC374 OCTAL D LATCHES
IC413 uPD75004GD-777-3B4
IC414 TL7705
IC416 uPD6253
IC419 74HC4040 12-BIT BIN COUNTER
IC421 A 4538 MONOSTABLE MULTIVIBRATOR
IC421 B 4538 MONOSTABLE MULTIVIBRATOR
IC310 B 4538 MONOSTABLE MULTIVIBRATOR
IC420 A 74HC74
IC420 B 74HC74
IC405 74LS06
IC417 74LS06
IC418 74HC14
IC412 74HC04
D403-410 LT1L51A
R440-455 1KF
R437-442 1K X 6
100K X 8
100K X 12
X401 4.19MHz
CN101
CN102
MCLED (022A)
PWRCTL
XKEYRST1
XKEYRST2
XLEDSEL (046C)
X1CHIPH (046C)
X1ORST (041C)
(020D) DATA-BUS
TCCLR (= 6C)
XERESET
XEXTRST
STNBY
M/XS-SEL
FIL402 NFM61R20T472
C451-454 0.1uF
NOTE IC414,416 pin8=+5VD,pin4=E2
IC417,418 pin14=+5VD,pin7=E2
IC419 pin16=+5VD,pin8=E2
IC405,420 pin14=+5V,pin7=E2
IC415,422 pin20=+5V,pin10=E2
IC421 pin16=+5V,pin8=E2
12-May-92 16:43:44 FILE:0797-5C

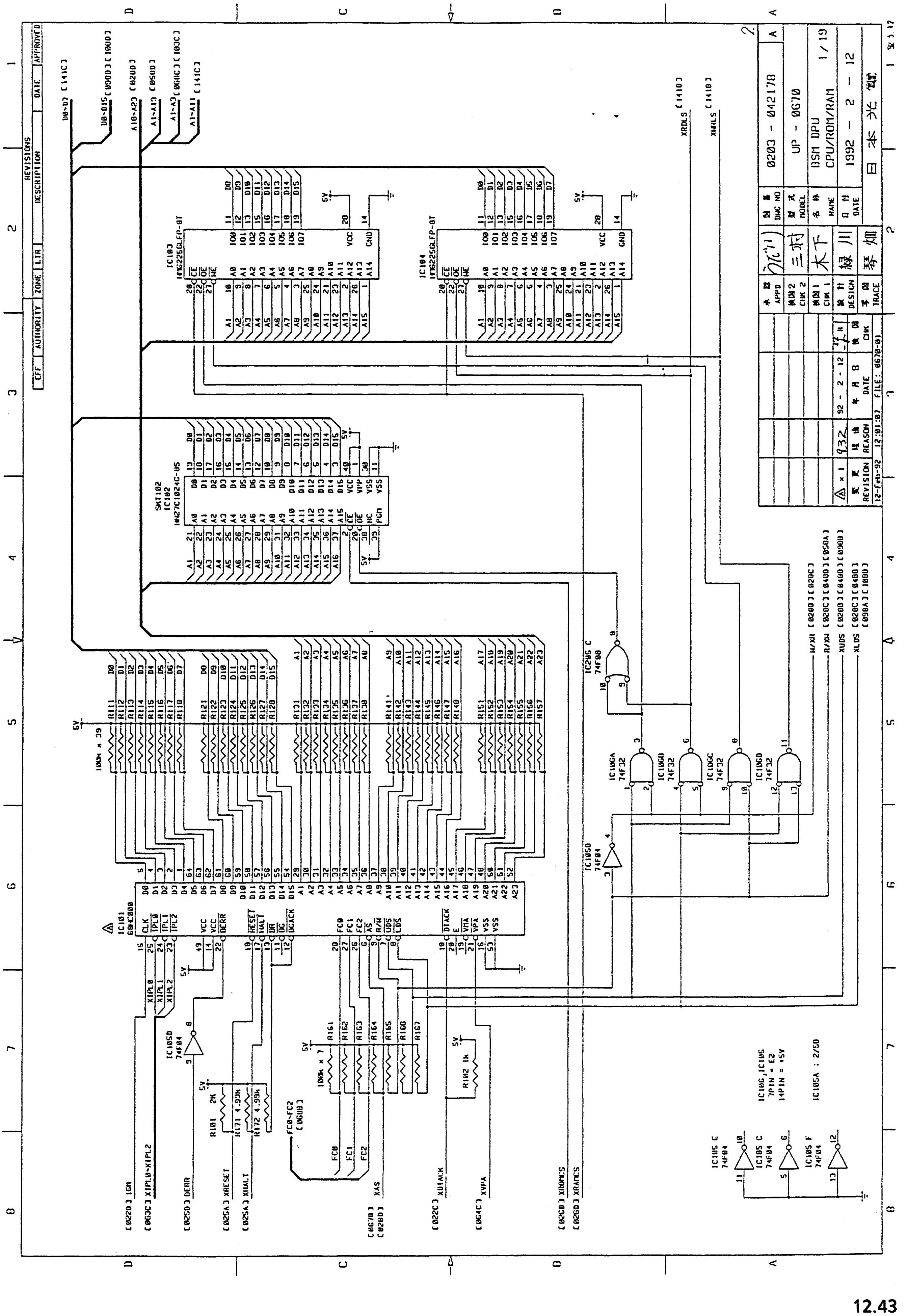
12. CIRCUIT DIAGRAM


0203-056243
UP-0797
I/O BOARD 6/6
1991 - 11 - 28
IC509 MB834200A-20
IC510 MB834200A-20
IC511 74HC244 QUAD BUFFER/LINE DRIVER
IC512 74HC244 QUAD BUFFER/LINE DRIVER
IC504 A 74HC08
IC505 74HC595 SRG8 WITH OUTPUT LATCH
IC506 74HC595 SRG8 WITH OUTPUT LATCH
IC507 74HC595 SRG8 WITH OUTPUT LATCH
IC508 74HC595 SRG8 WITH OUTPUT LATCH
IC503 A 74HC32
IC503 B 74HC32
IC503 C 74HC32
IC503 D 74HC32
IC501 A 74HC32
IC501 B 74HC32
IC501 C 74HC32
IC501 D 74HC32
IC502 A 74HC32
IC502 B 74HC32
IC502 C 74HC32
IC502 D 74HC32
IC309 C 74HC00
IC309 D 74HC00
IC405 F 74LS06
IC504 B 74HC08
IC504 C 74HC08
IC504 D 74HC08
RS17-524 100K
RS01-516 100K
CHRSL1 [047C]
CHRSL2 [047C]
ADDR-BUS [023C]
DATA-BUS [023D]
[046D] SRSL1
[046D] SRSL2
[046D] SRSL3
[046D] SRSL4
[045C] XSRSEL
[045C] XRCLK
NOTE
IC501-504 pin14=+5V,pin7=E2
IC505-508 pin16=+5V,pin8=E2
IC509,510 pin27=+5V,pin12,40,41=E2
IC511,512 pin20=+5V,pin10=E2
REVISION
16-Jan-92 17:31:20
FILE:0797-6A
'92-01-16
DHC NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE

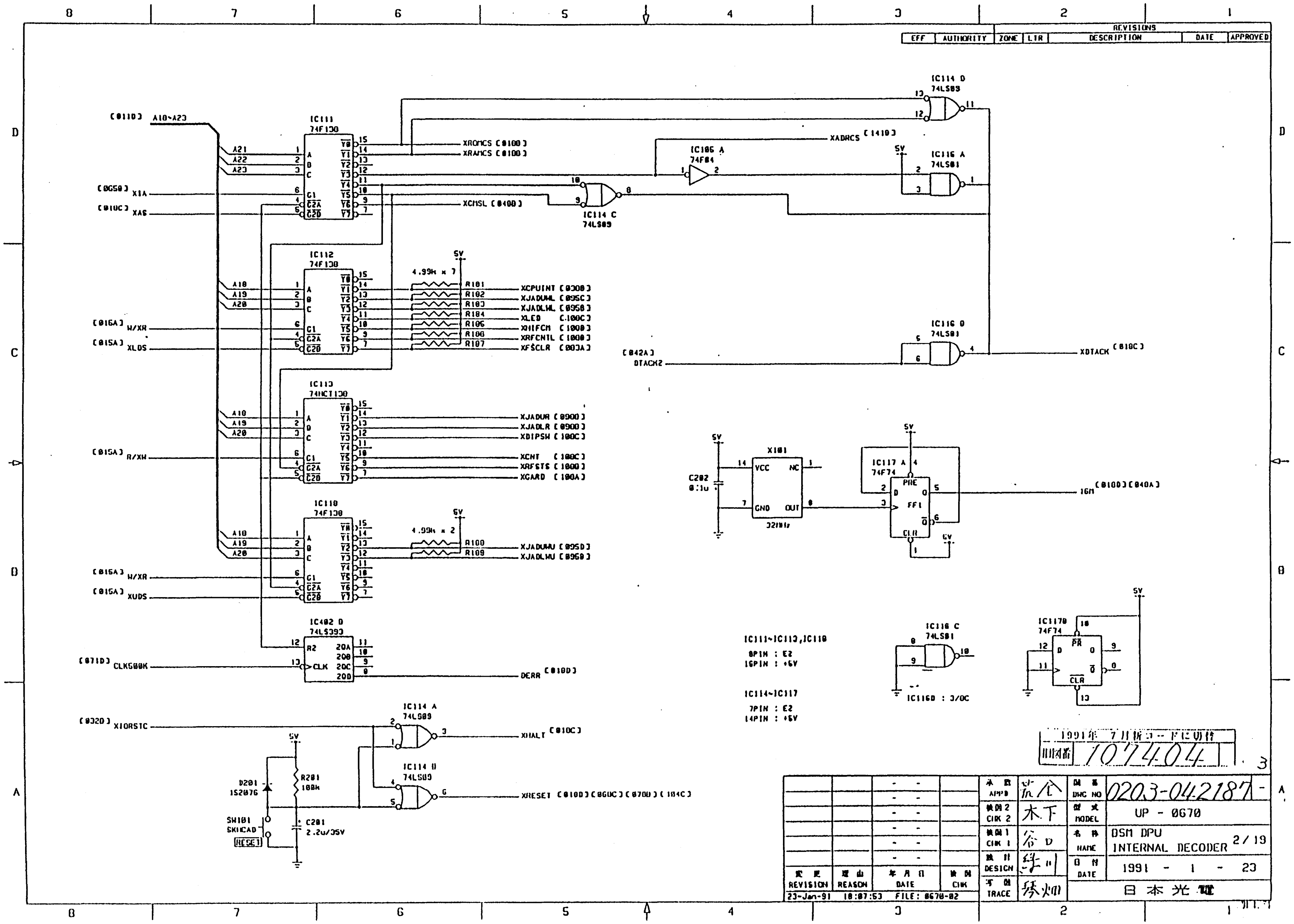

0203-056279
UP-0799
MEMORYCARD BOARD 1/1
1991 - 11 - 15
日本光電
CN101
HIF6-60PA-1.27DS
CN102
JC20EA-J60P-V4LT-A1
FIL101-108,111-162
DLM21A05
FIL101-180 DLA01D91
SH101
FIL109
NFM61R30T472
FIL110
NFM61R30T472
FIL163
DLM21A05
FIL164
DLM21A05
D101
MCSH
+5V
MCLED
VPP
E2
'92-04-23
FILE:UP-0799A

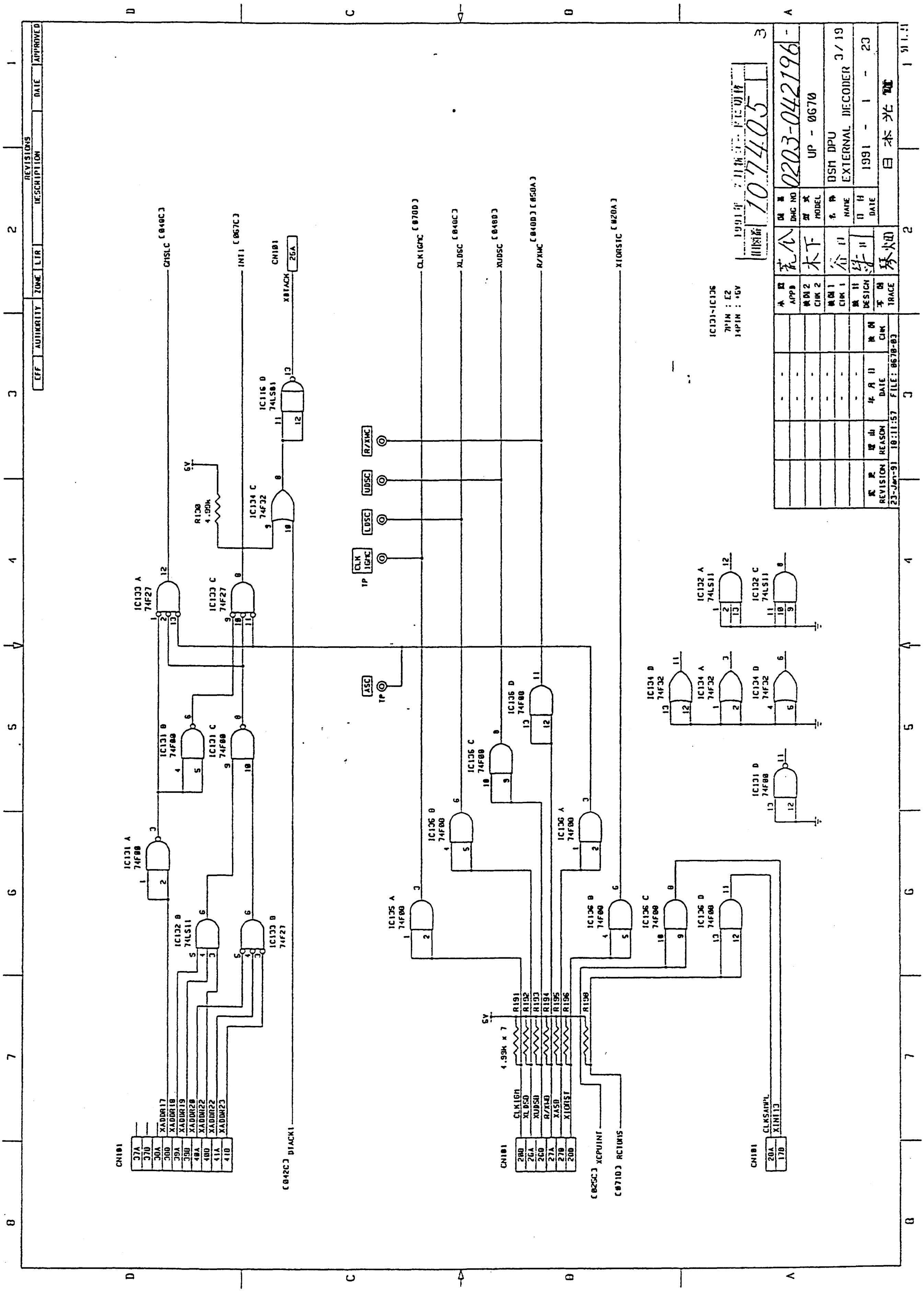
12. CIRCUIT DIAGRAM


CN103
HLJ2308-01-3030
CN104
IQ212-10RA-0SDL(03)
CN101
EXTIN
AUX2IN
+5VD
EXTRDY
IOTxD3
IORxD3
XKEYRST2
STNDY
SW101
SKHHLR
XEXTRST
E1
E2
D101
GL3KG8
D102
GL3KG8
FFC-20DSM1102
+5VL
+5VDL
CN102 A
HLJ0527-01-3030
CN102 D
P1H
ECG1H
0203-056288
UP-0807
CONNECTOR BOARD 1/1
1991 - 11 - 14
日本光電
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
20-Nov-91 22:50:57
FILE:UP-0807

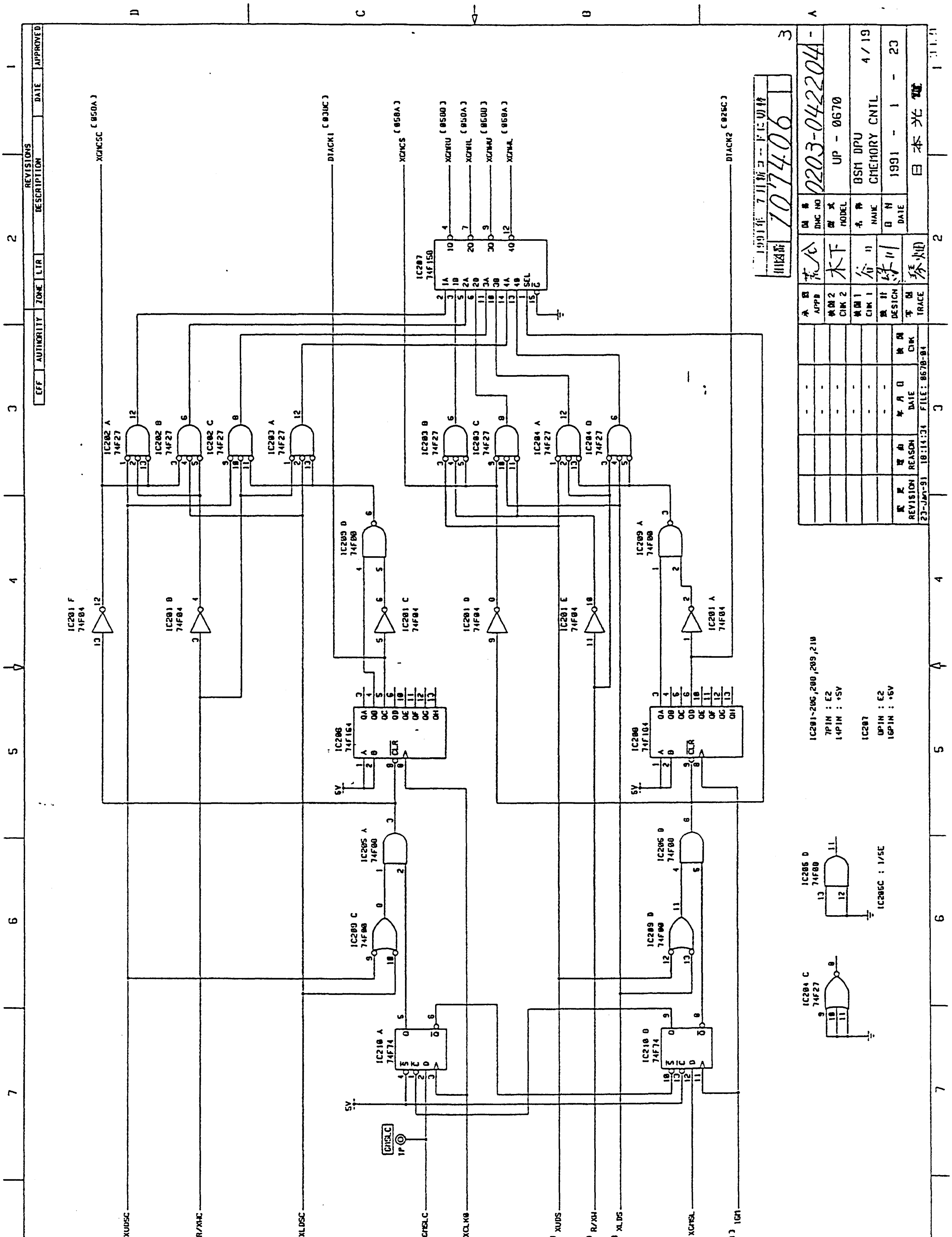

0203 - 042178
UP - 0670
DSM DPU
CPU/ROM/RAM
1/19
1992 - 2 - 12
IC101 68HC000
SKT102 IC102 HN27C1024G-05
IC103 HM6225GLFP-8T
IC104 HM6225GLFP-8T
IC205 C 74F00
IC106A 74F32
IC106B 74F32
IC106C 74F32
IC106D 74F32
IC105B 74F04
IC105D 74F04
IC105 E 74F04
IC105 C 74F04
IC105 F 74F04
IC106,IC105 7PIN = E2 14PIN = +5V
IC105A : 2/5D
100K x 39
100K x 7
R101 2K
R171 4.99K
R172 4.99K
R102 1K
REVISIONS
REVISION
REASON
DATE
FILE: 0670-01
12-Feb-92 12:01:07

12. CIRCUIT DIAGRAM


REVISIONS
EFF
AUTHORITY
ZONE
LTR
DESCRIPTION
DATE
APPROVED
[0110] A10~A23
IC111 74F138
IC112 74F138
IC113 74HCT138
IC110 74F138
IC402 D 74LS393
A21
A22
A23
A18
A19
A20
[0G50] X1A
[010C] XAS
[016A] W/XR
[015A] XLDS
[015A] R/XW
[016A] W/XR
[015A] XUDS
[071D] CLK500K
[0320] XIORSTC
XROMCS [0100]
XRAMCS [0100]
XCMSL [0400]
4.99k × 7
5V
R101
R102
R103
R104
R105
R106
R107
XCPUINT [0300]
XJADUML [095C]
XJADLML [0950]
XLED [100C]
XHIFCM [1000]
XRFCNTL [1000]
XFSCLR [003A]
XJADUR [0900]
XJADLR [0900]
XDIPSW [100C]
XCNT [100C]
XRFSTS [1000]
XGARD [100A]
4.99k × 2
R108
R109
XJADUWU [095D]
XJADLWU [0950]
DERR [010D]
IC114 D 74LS89
IC114 C 74LS89
IC106 A 74F04
XADRCS [1410]
IC116 A 74LS01
IC116 D 74LS01
[042A] DTACK2
XDTACK [010C]
X101
VCC
NC
GND
OUT
32MHz
C202 0.1u
IC117 A 74F74
PRE
FF1
CLR
16M [0100] [040A]
IC116 C 74LS01
IC116D : 3/OC
IC117B 74F74
PR
CLR
IC111~IC113,IC110
8PIN : E2
16PIN : +5V
IC114~IC117
7PIN : E2
14PIN : +5V
IC114 A 74LS89
IC114 B 74LS89
XHALT [010C]
XRESET [0100] [060C] [070D] [104C]
D201 1S2076
R201 100k
C201 2.2u/35V
SW101 SKHCAD
RESET
1991年 7月新コードに切替
旧図番 107404
3
承認 APP'D 森
検図2 CHK 2 木下
検図1 CHK 1 谷口
設計 DESIGN
写図 TRACE 藤畑
図番 DWG NO 0203-042187 -
型式 MODEL UP - 0670
名称 NAME DSM DPU INTERNAL DECODER 2/19
日付 DATE 1991 - 1 - 23
日本光電
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
23-Jan-91 18:07:53 FILE: 0670-02


0203-042196
1074205
UP - 0670
DSM DPU
EXTERNAL DECODER 3/19
1991 - 1 - 23
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
23-Jan-91 10:11:57 FILE: 0670-03
REVISIONS
EFF
AUTHORITY
ZONE
LTR
DESCRIPTION
DATE
APPROVED
IC131-IC136
7PIN : E2
14PIN : +5V
CN101
XADDR17
XADDR18
XADDR19
XADDR20
XADDR21
XADDR22
XADDR23
DTACK1
CLK16M
XLDSD
XUDSD
R/XWD
XASD
XIORST
XCPUINT
RCTRIS
CLKSAMPL
XINT13
CMSLC
INT1
XDTACK
CLK16MC
XLDSC
XUDSC
R/XWC
XIORSTC
R130 4.99k
4.99k x 7
R191
R192
R193
R194
R195
R196
R198
IC131 A 74F00
IC131 B 74F00
IC131 C 74F00
IC131 D 74F00
IC132 A 74LS11
IC132 B 74LS11
IC132 C 74LS11
IC133 A 74F27
IC133 B 74F27
IC133 C 74F27
IC134 A 74F32
IC134 B 74F32
IC134 C 74F32
IC134 D 74F32
IC135 A 74F00
IC136 A 74F00
IC136 B 74F00
IC136 C 74F00
IC136 D 74F00
IC116 D 74LS01
TP
CLK 16MC
LDSC
UDSC
R/XWC
ASC
5V

12. CIRCUIT DIAGRAM



REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
EFF
AUTHORITY
XCMCSC (050A)
DIACK1 (030C)
XCMCS (050A)
XCMHU (050D)
XCMHL (050A)
XCMWU (060D)
XCMWL (060A)
DIACK2 (020C)
IC207 74F158
IC202 A 74F27
IC202 B 74F27
IC202 C 74F27
IC203 A 74F27
IC203 B 74F27
IC203 C 74F27
IC204 A 74F27
IC204 D 74F27
IC209 D 74F00
IC209 A 74F00
IC201 F 74F04
IC201 B 74F04
IC201 C 74F04
IC201 D 74F04
IC201 E 74F04
IC201 A 74F04
IC208 74F164
IC208 74F164
IC205 A 74F00
IC206 B 74F00
IC209 C 74F00
IC209 D 74F00
IC210 A 74F74
IC210 B 74F74
5V
CMSLC
TP
(030D) XUDSC
(030D) R/XWC
(030D) XLDSC
(030D) CMSLC
(071D) XCLK0
(015A) XUDS
(015A) R/XW
(015A) XLDS
(020D) XCMSL
(022D) ICM
IC201-206,208,209,210
7PIN : E2
14PIN : +5V
IC207
8PIN : E2
16PIN : +5V
IC205 D 74F00
IC205C : 1/5E
IC204 C 74F27
1991年 7月15日
日図番
1074.06
3
図番 DWG NO
0203-042204
形式 MODEL
UP - 0670
名称 NAME
BSM DPU
CMEMORY CNTL
4/19
日付 DATE
1991 - 1 - 23
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
日本光電
変更 REVISION
理由 REASON
年月日 DATE
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23-Jan-91
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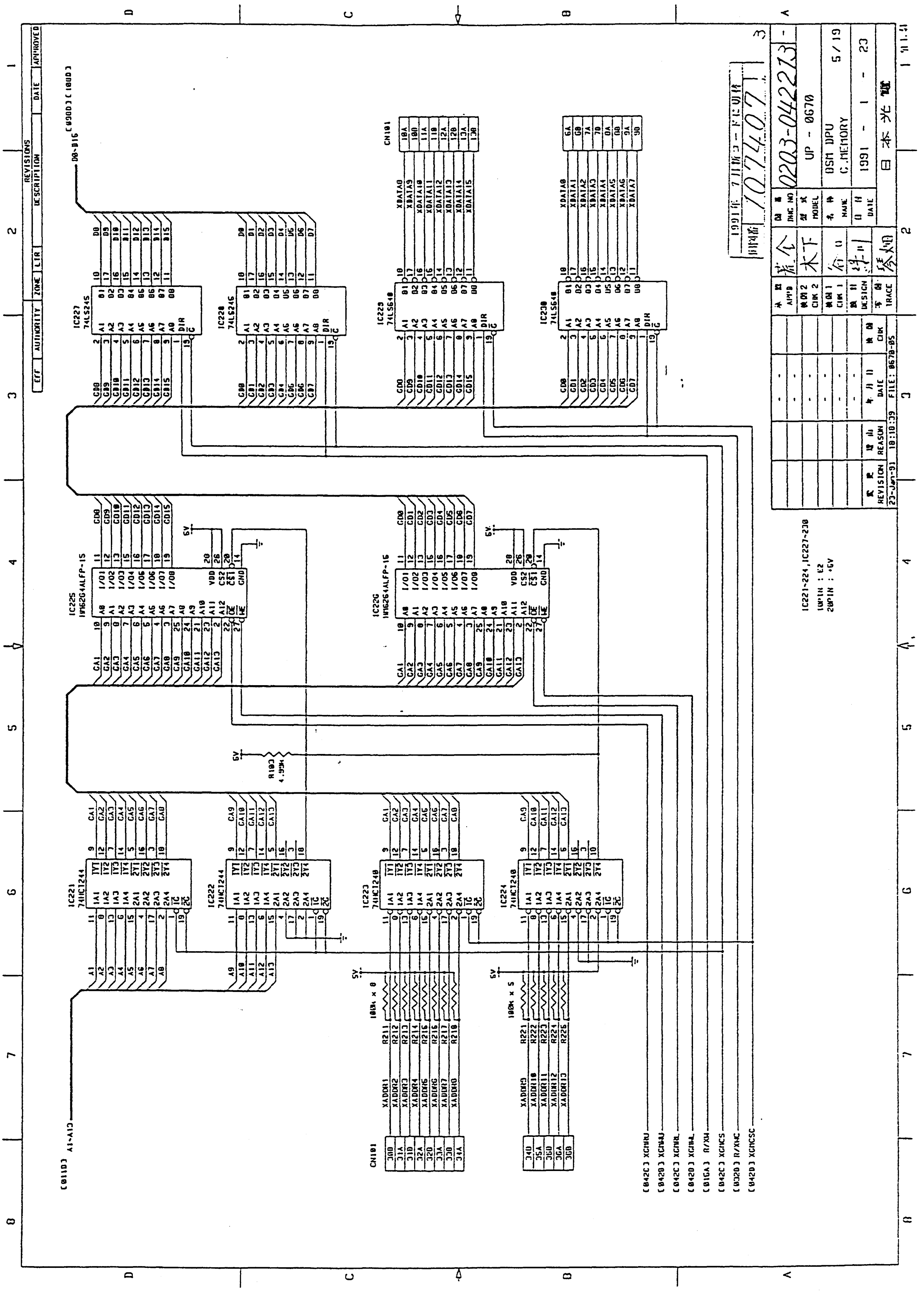
REVISIONS
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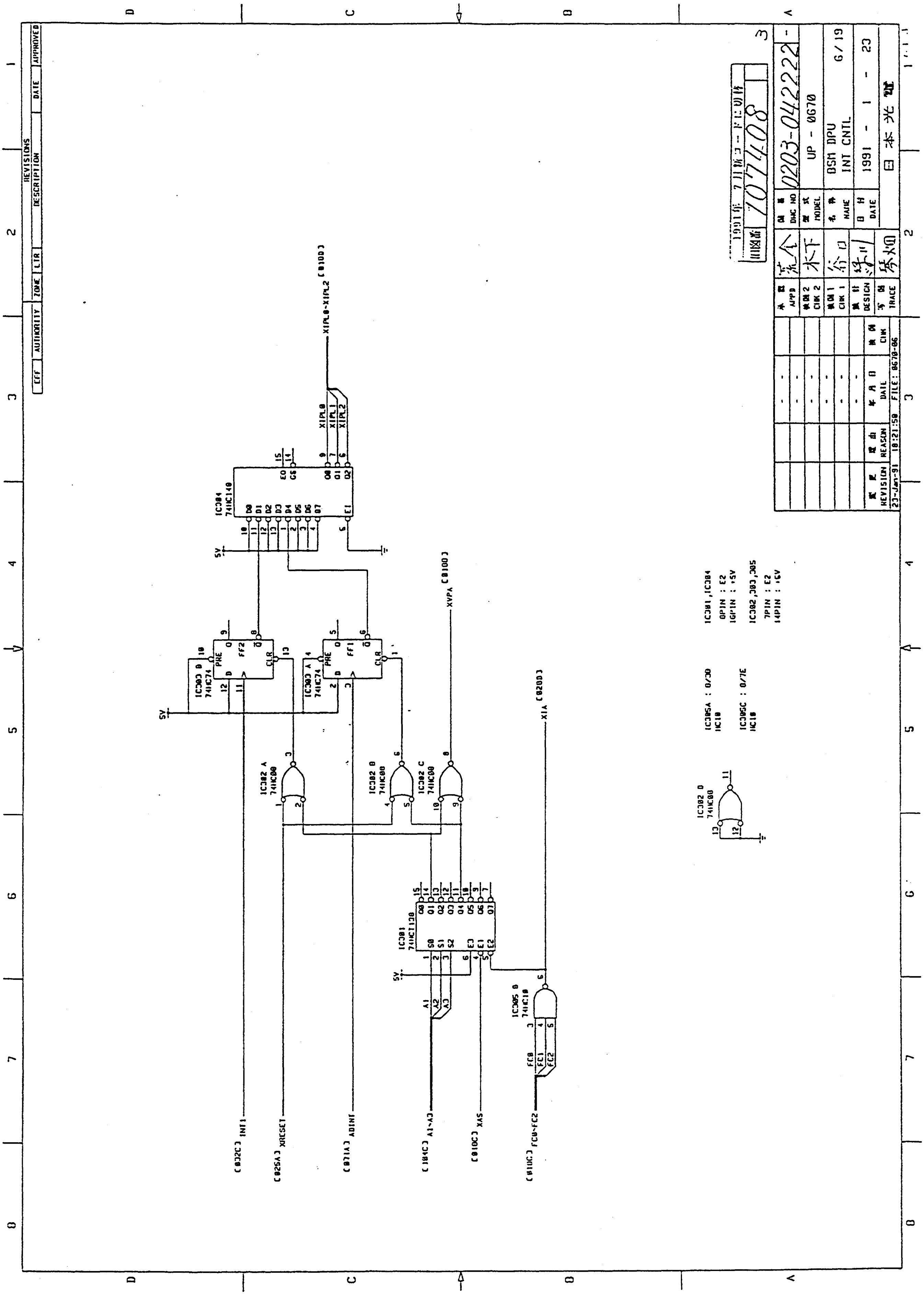
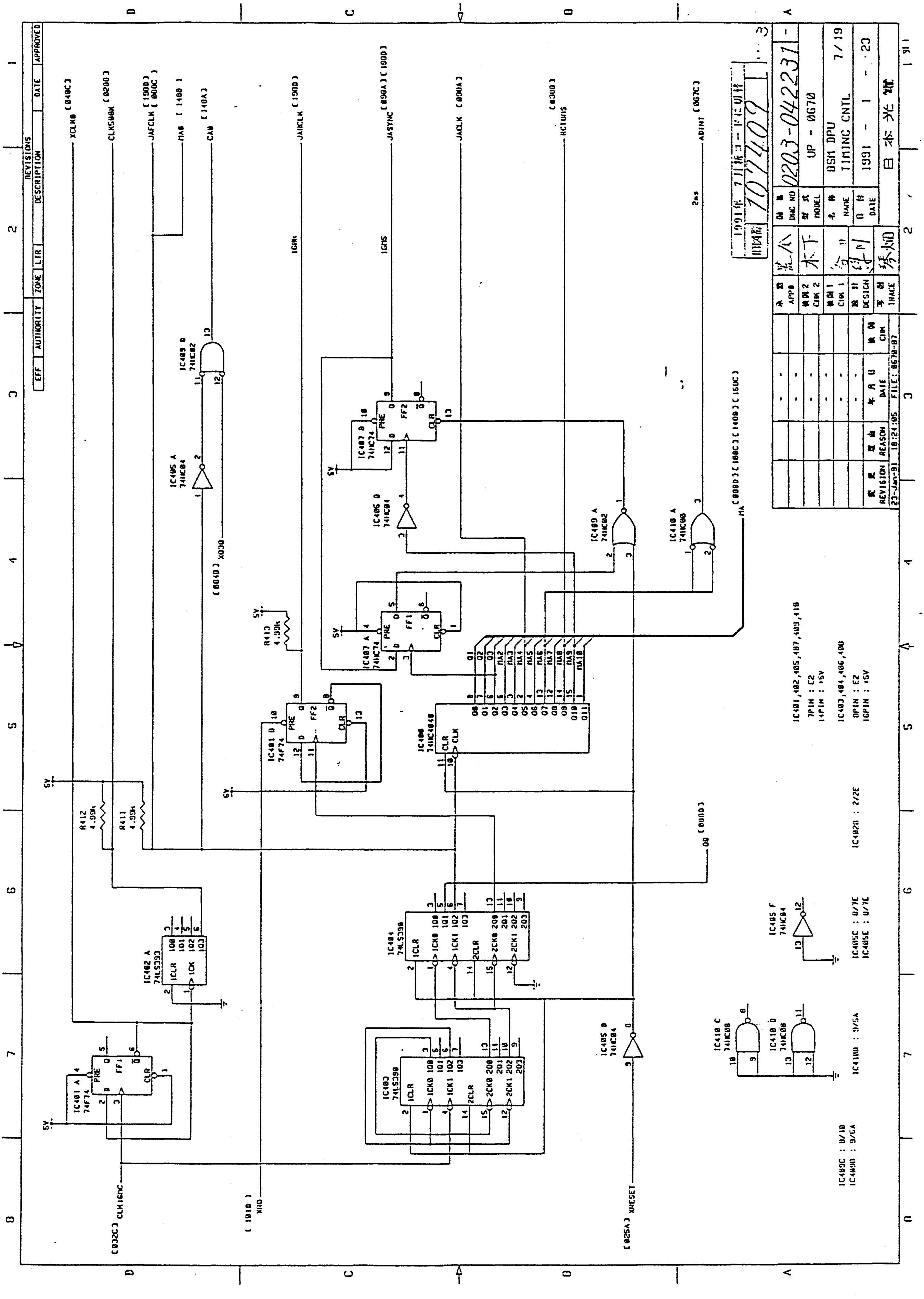
DESCRIPTION
DATE
APPROVED
D0-D16
IC227
74LS245
IC228
74LS245
IC229
74LS640
IC230
74LS640
CN101
XDATA0
XDATA1
XDATA2
XDATA3
XDATA4
XDATA5
XDATA6
XDATA7
XDATA8
XDATA9
XDATA10
XDATA11
XDATA12
XDATA13
XDATA14
XDATA15
IC225
HM6264ALFP-15
IC226
HM6264ALFP-15
5V
R103
4.99K
IC221
74HCT244
IC222
74HCT244
IC223
74HCT240
IC224
74HCT240
100K x 8
100K x 5
XADDR1
XADDR2
XADDR3
XADDR4
XADDR5
XADDR6
XADDR7
XADDR8
XADDR9
XADDR10
XADDR11
XADDR12
XADDR13
A1-A13
XCMRU
XCMWU
XCMRL
XCMWL
R/XW
XCMCS
R/XMC
XCMCSC
IC221-224,IC227-230
10PIN : E2
20PIN : +5V
DWG NO
0203-042273
MODEL
UP - 0670
NAME
DSM DPU
C.MEMORY
5/19
DATE
1991 - 1 - 23
APP'D
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
23-Jan-91
18:10:39
FILE: 0670-05

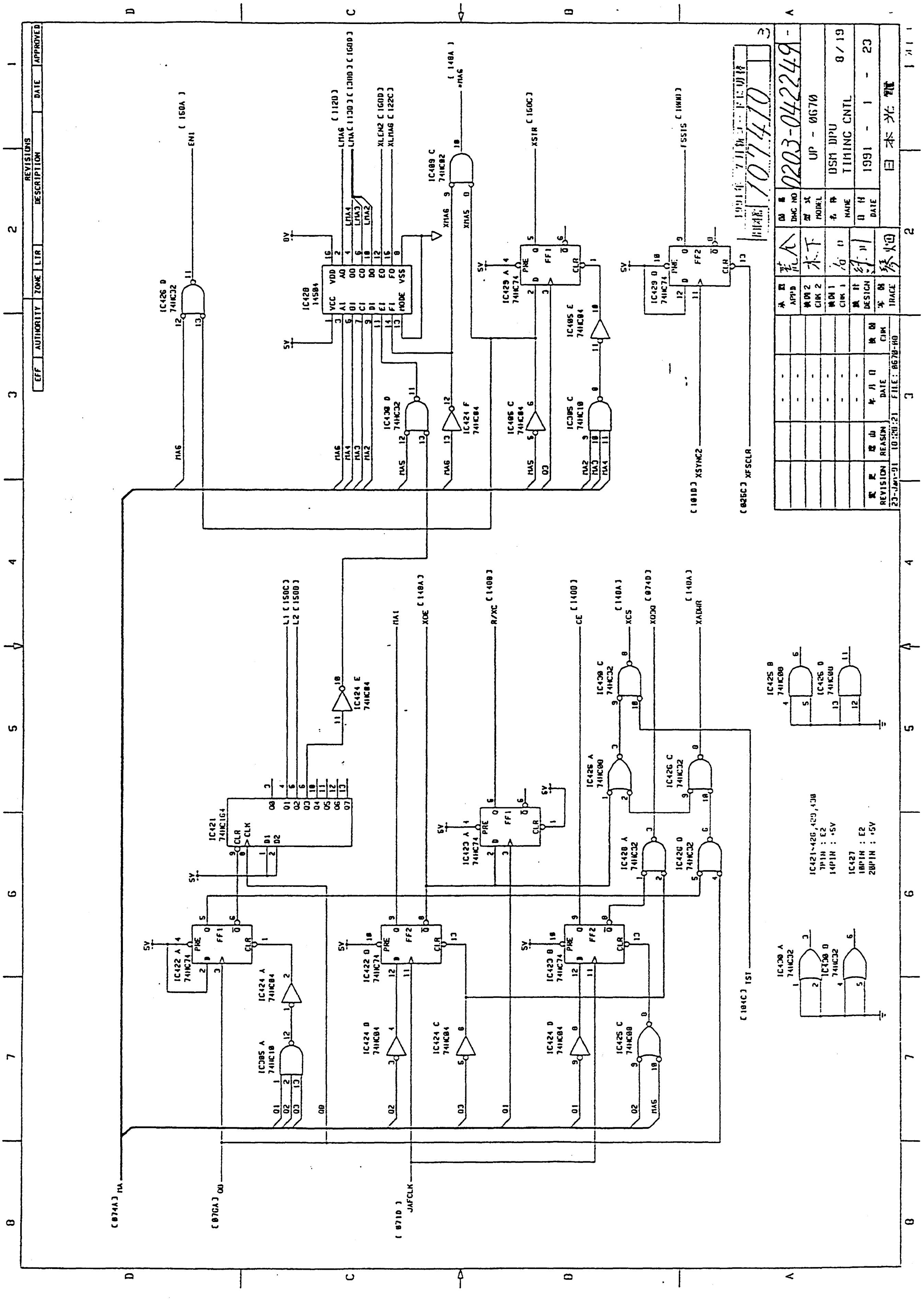
12. CIRCUIT DIAGRAM

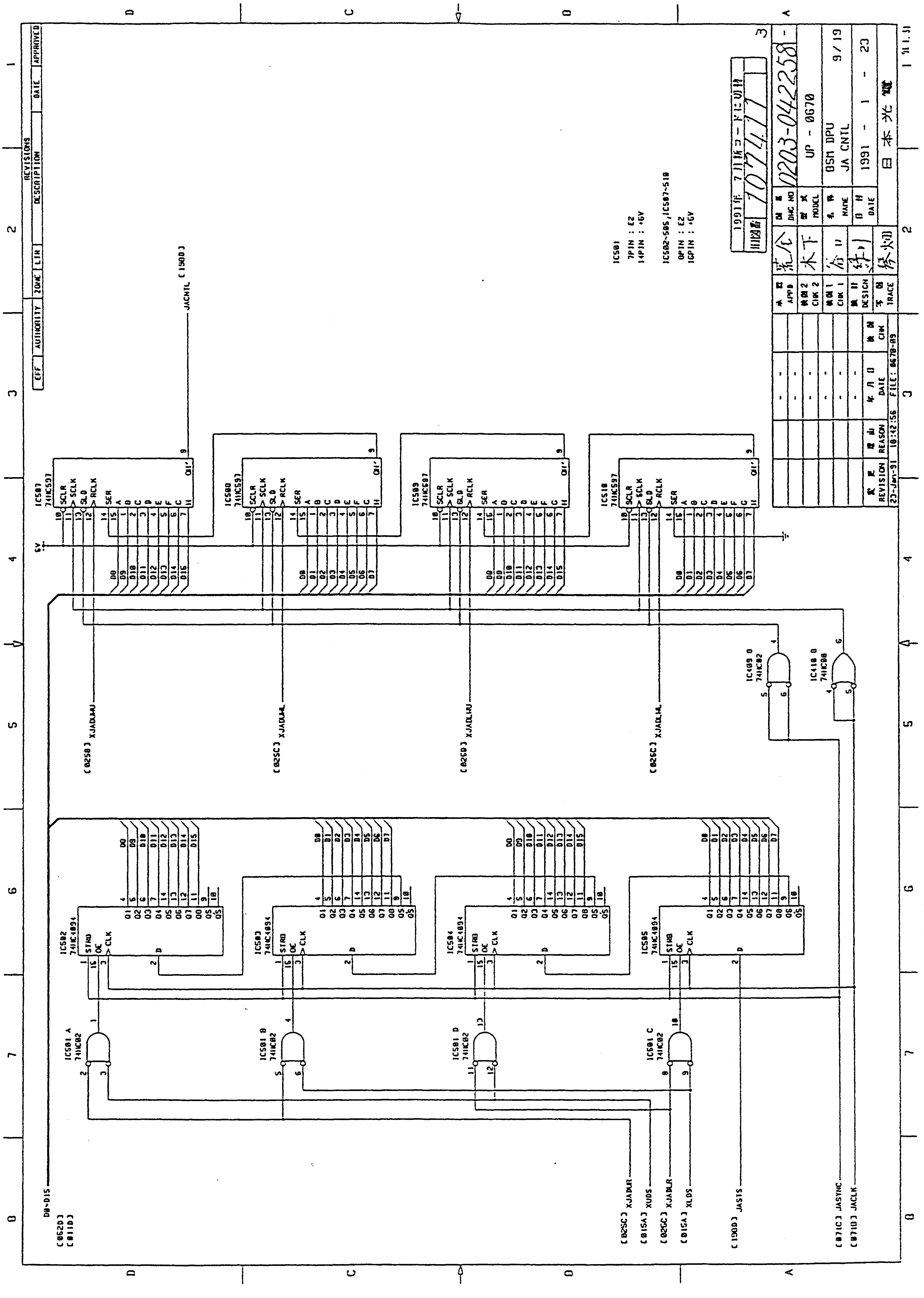


IC304 74HC148
D0 D1 D2 D3 D4 D5 D6 D7 EI
E0 GS Q0 Q1 Q2
XIPL0 XIPL1 XIPL2
XIPL0~XIPL2 (B10D)
IC303 B 74HC74
FF2
IC303 A 74HC74
FF1
PRE D CLR Q
5V
XVPA (B10D)
XIA (B20D)
IC302 A 74HC00
IC302 B 74HC00
IC302 C 74HC00
IC302 D 74HC00
IC301 74HCT138
S0 S1 S2 E3 E1 E2
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
A1 A2 A3
IC305 B 74C10
FC0 FC1 FC2
(B02C) INT1
(B25A) XRESET
(B71A) ADINT
(104C) A1~A3
(B10C) XAS
(B10C) FC0~FC2
IC301,IC304
8PIN : E2
16PIN : +5V
IC302,303,305
7PIN : E2
14PIN : +5V
IC305A : 0/30
HC10
IC305C : 0/7E
HC10
REVISIONS
EFF AUTHORITY ZONE LTR DESCRIPTION DATE APPROVED
707408
0203-042222
UP - 0670
BSM DPU
INT CNTL
6/19
1991 - 1 - 23
REVISION REASON DAIL CHK
23-Jan-91 10:21:50 FILE: 0670-06
APPD CHK 2 CHK 1 DESIGN TRACE
DWG NO MODEL NAME DATE

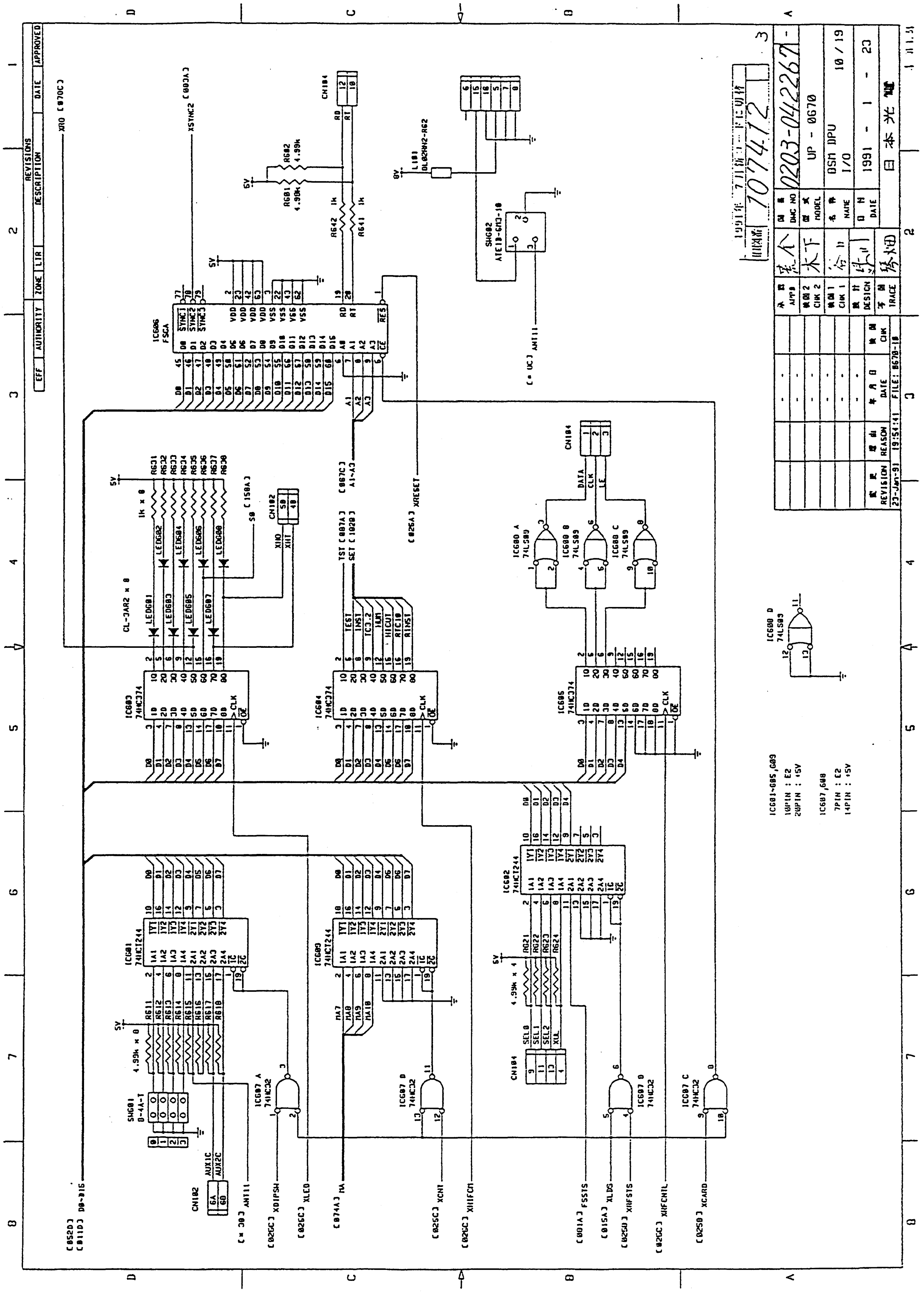

REVISIONS
EFF
AUTHORITY
ZONE
LTR
DESCRIPTION
DATE
APPROVED
XCLK0 [040C]
CLK500K [0200]
JAFCLK [190D] [0B0C]
MA0 [140D]
CA0 [140A]
JAFCLK [190D]
JASYNC [090A] [100D]
JACLK [090A]
HCTU15 [030D]
ADINT [067C]
IC409 D 74HC02
IC405 A 74HC04
IC407 B 74HC74
FF2
IC406 D 74HC04
IC409 A 74HC02
IC410 A 74HC00
IC407 A 74HC74
FF1
R413 4.99k
IC401 B 74F74
IC408 74HC4040
Q1 Q2 Q3 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA10
MA [080D] [10BC] [140D] [150C]
X030 [0040]
5V
R412 4.99k
R411 4.99k
IC402 A 74LS393
IC404 74LS390
IC403 74LS390
IC401 A 74F74
IC405 D 74HC04
IC405 F 74HC04
IC410 C 74HC00
IC410 D 74HC00
CLK16MC [032C]
X00 [1910]
XRESET [025A]
00 [080D]
IC401,402,405,407,409,410
7PIN : E2
14PIN : +5V
IC403,404,406,408
8PIN : E2
16PIN : +5V
IC402B : 2/2E
IC405C : 0/7E
IC405E : 0/7E
IC410B : 9/5A
IC409C : 0/10
IC409B : 9/6A
REVISION
REASON
DATE
CHK
APPD
CHK 2
CHK 1
DESIGN
TRACE
DWG NO
MODEL
NAME
DATE
0203-042231
UP - 0G70
BSM DPU
TIMING CNTL
7/19
1991 - 1 - 23
23-Jan-91 10:24:05 FILE: 0G70-07
107409
日 本 光 電

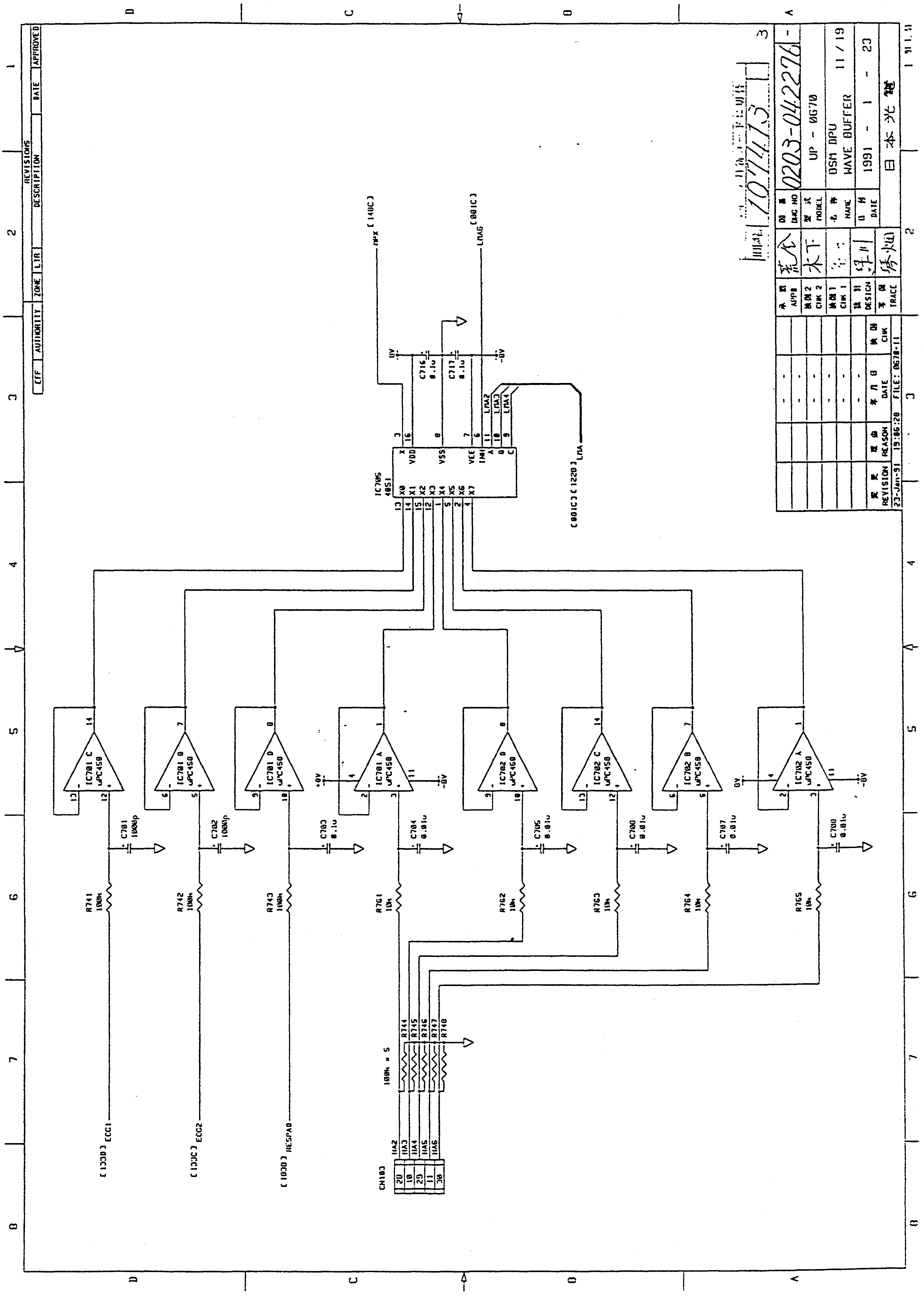
12. CIRCUIT DIAGRAM


UP - 0G70
DSM DPU
TIMING CNTL
8/19
1991 - 1 - 23
0203-042249
107470
IC420
14584
IC421
74HC164
IC422 A
74HC74
IC423 A
74HC74
IC429 A
74HC74
IC429 B
74HC74
FF1
FF2
EN1
XSTR
XSSTS
XCS
XDCK
XADWR
XOE
R/XC
CE
L1
L2
XSYNC2
XFSCLR
JAFCLK
TST
MA
Q0
5V
REVISION
REASON
DATE
FILE: 0G70-H0

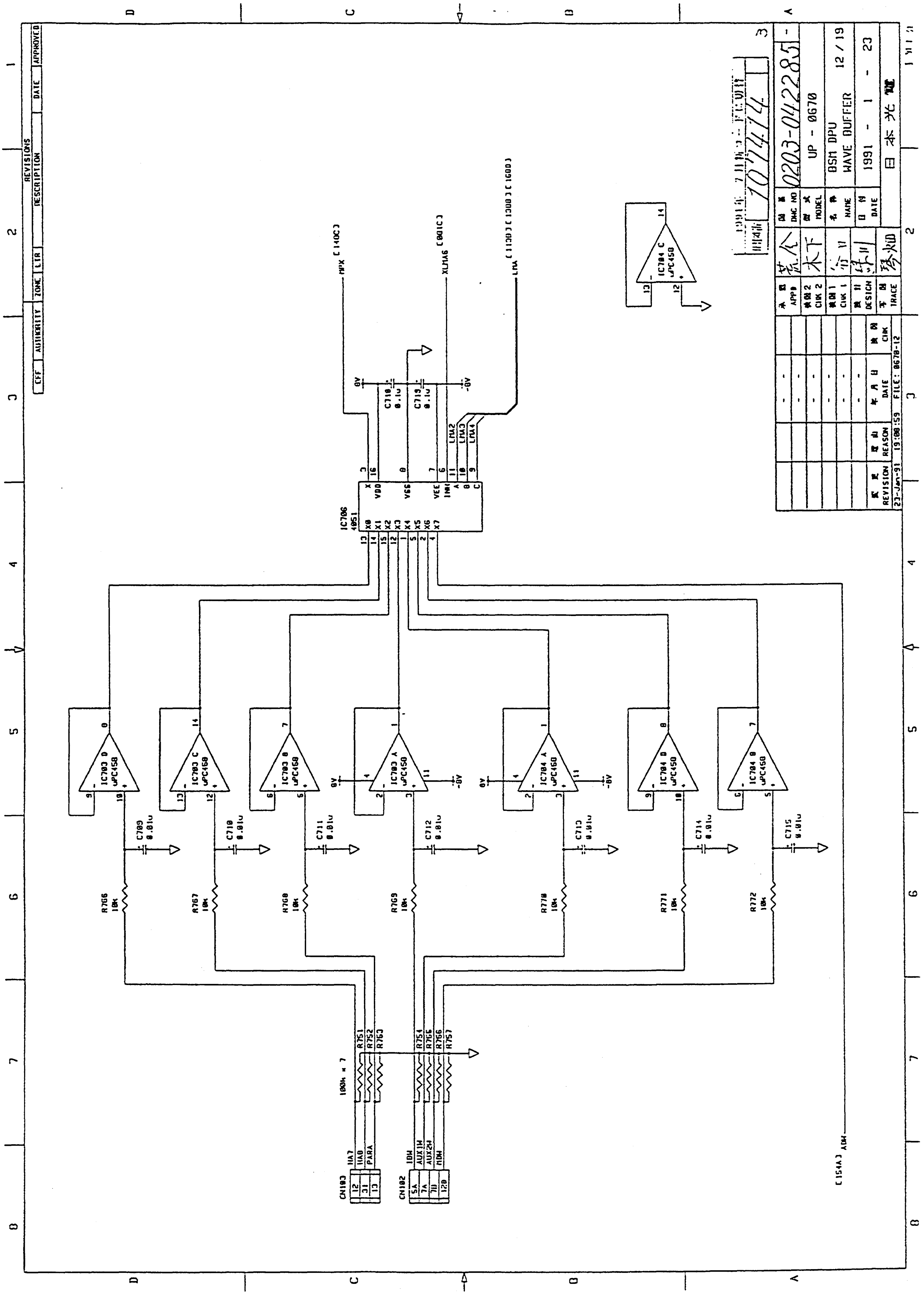

REVISIONS
EFF
AUTHORITY
ZONE
LTR
DESCRIPTION
DATE
APPROVED
JACNTL [1900]
IC501
7PIN : E2
14PIN : +5V
IC502~505, IC507~510
8PIN : E2
16PIN : +5V
IC507 74HC597
IC508 74HC597
IC509 74HC597
IC510 74HC597
SCLR
SCLK
SLD
RCLK
SER
QH'
5V
D0~D15
[025B] XJADUHU
[025C] XJADUAL
[025D] XJADLHU
[025C] XJADLHL
IC409 D 74HC02
IC410 D 74HC08
IC502 74HC4094
IC503 74HC4094
IC504 74HC4094
IC505 74HC4094
STRB
OE
CLK
IC501 A 74HC02
IC501 B 74HC02
IC501 D 74HC02
IC501 C 74HC02
D0~D15
[0520]
[011D]
[025C] XJADUR
[015A] XUDS
[026C] XJADLR
[015A] XLDS
[1900] JASTS
[071C] JASYNC
[071D] JACLK
1991年 7月16日 コード切替
旧図番 707477
3
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
手描 TRACE
図番 DWG NO 0203-042258 -
型式 MODEL UP - 0670
名称 NAME BSM DPU JA CNTL 9/19
日付 DATE 1991 - 1 - 23
日本光電
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
23-Jan-91 10:42:56 FILE: 0670-09

12. CIRCUIT DIAGRAM

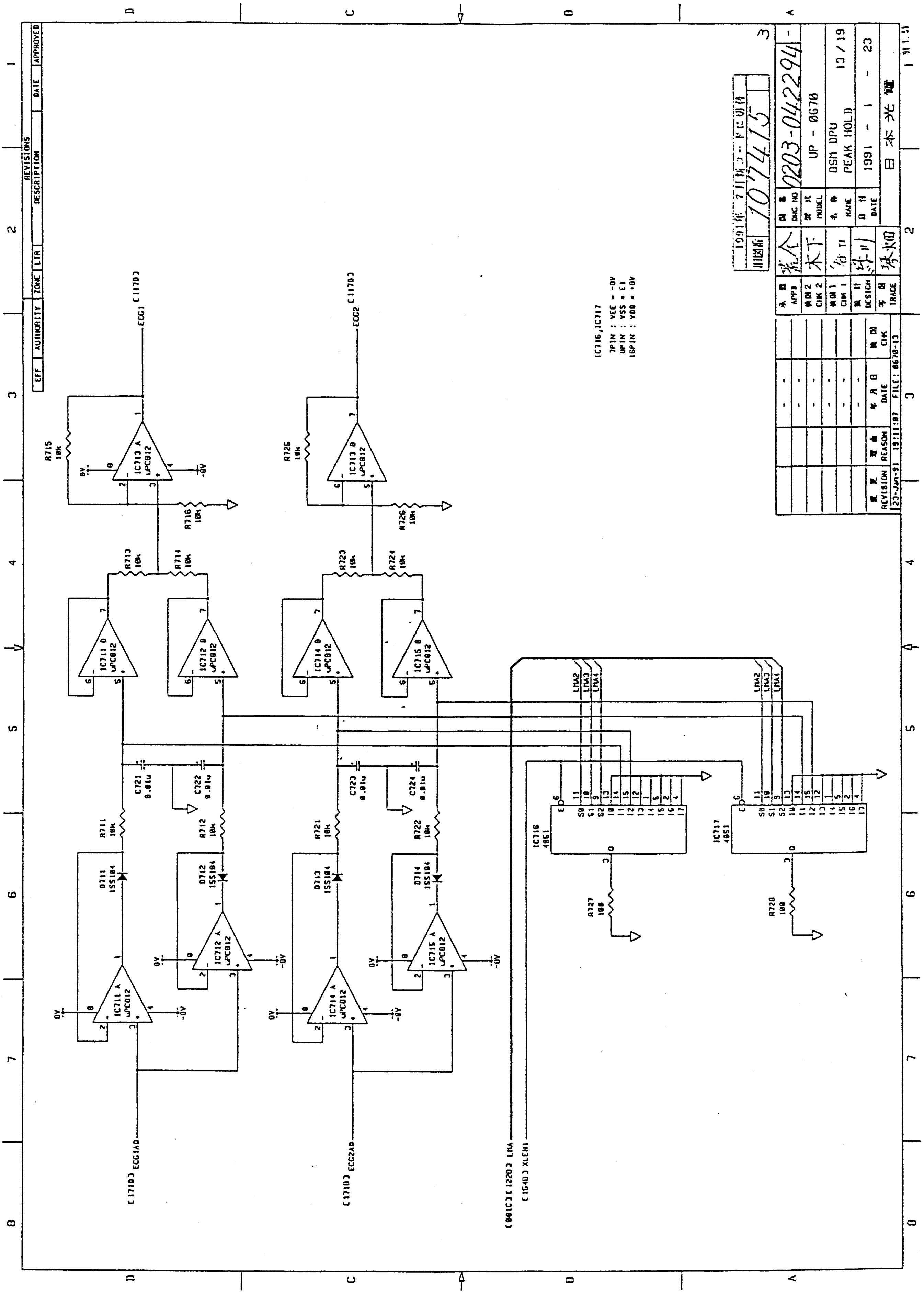

REVISIONS
EFF
AUTHORITY
ZONE
LTR
DESCRIPTION
DATE
APPROVED
IC606 FSGA
IC601 74HCT244
IC602 74HCT244
IC603 74HC374
IC604 74HC374
IC605 74HC374
IC609 74HCT244
IC607 A 74HC32
IC607 B 74HC32
IC607 C 74HC32
IC607 D 74HC32
IC608 A 74LS09
IC608 B 74LS09
IC608 C 74LS09
IC608 D 74LS09
CN102
CN104
SHG01 D-4A-T
SHG02 ATE1D-6M3-10
L101 DL02HM2-R62
R601 4.99k
R602 4.99k
R641 1k
R642 1k
1k x 8
4.99k x 8
4.99k x 4
CL-3AR2 x 8
LED601
LED602
LED603
LED604
LED605
LED606
LED607
LED608
XRO [070C]
XSYNC2 [003A]
XRESET [026A]
A1-A3 [067C]
TST [007A]
SET [102D]
S0 [158A]
XIO
XHT
[052D]
[011D] D0-D16
[* 3D] ANT11
[026C] XDIPSW
[026C] XLED
[074A] MA
[025C] XCNT
[026C] XHIFCNT
[001A] FSSTS
[015A] XLDS
[025D] XHFSTS
[002C] XHFCNTL
[025D] XCARD
[* UC] ANT11
SEL0
SEL1
SEL2
XUL
DATA
CLK
LE
RD
RT
TEST
INST
TC3.2
HUM
HICUT
RTC10
RINST
MA7
MA8
MA9
MA10
AUX1C
AUX2C
5V
8V
IC601~605,609
10PIN : E2
20PIN : +5V
IC607,608
7PIN : E2
14PIN : +5V
1991年 7月 日 ～ 月 日
107412
3
0203-042267
-
図番 DWG NO
UP - 0G70
型式 MODEL
DSM DPU
I/O
名称 NAME
10 / 19
1991 - 1 - 23
日付 DATE
日本光電
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
23-Jan-91
19:54:41
FILE: 0670-10


REVISIONS
EFF
AUTHORITY
ZONE
LTR
DESCRIPTION
DATE
APPROVED
IC705
4051
X
VDD
VSS
VEE
INH
A
B
C
X0
X1
X2
X3
X4
X5
X6
X7
MPX
[140C]
LMAG
[001C]
LMA
[001C] [122D]
LMA2
LMA3
LMA4
C716 0.1u
C717 0.1u
0V
-0V
+0V
IC701 A uPC458
IC701 B uPC458
IC701 C uPC458
IC701 D uPC458
IC702 A uPC458
IC702 B uPC458
IC702 C uPC458
IC702 D uPC458
C701 1000p
C702 1000p
C703 0.1u
C704 0.01u
C705 0.01u
C706 0.01u
C707 0.01u
C708 0.01u
R741 100k
R742 100k
R743 100k
R761 10k
R762 10k
R763 10k
R764 10k
R765 10k
R744
R745
R746
R747
R748
100k x 5
CN103
IIA2
IIA3
IIA4
IIA5
IIA6
ECG1
ECG2
RESPAD
[103D]
0203-042276
UP - 0G70
DSM DPU
WAVE BUFFER
11 / 19
1991 - 1 - 23
日本光電
DWG NO
MODEL
NAME
DATE
APPR
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
23-Jan-91
19:06:20
FILE: 0670-11
107415
A
B
C
D
1
2
3
4
5
6
7
8

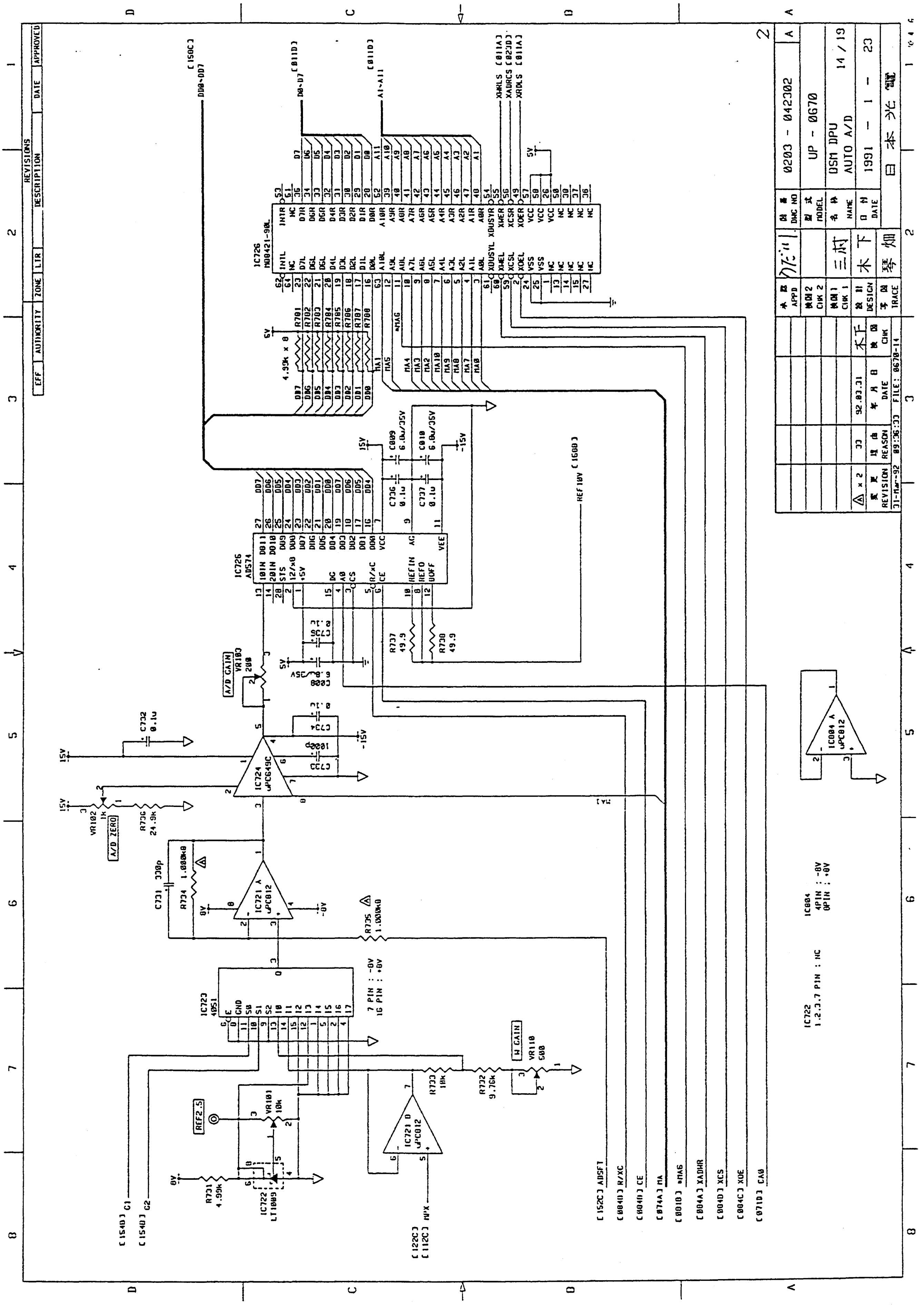
12. CIRCUIT DIAGRAM

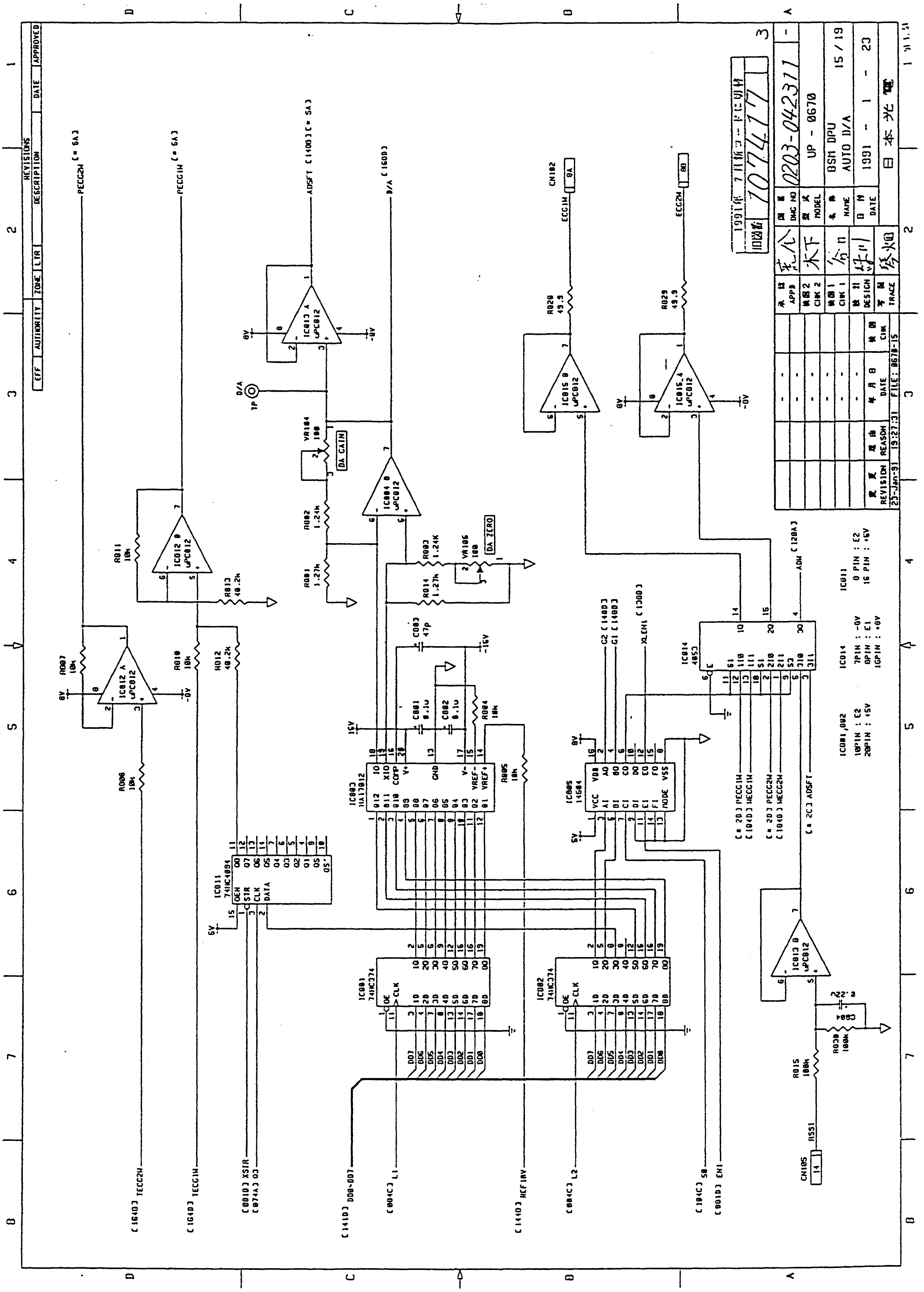


REVISIONS
EFF
AUTHORITY
ZONE
LTR
DESCRIPTION
DATE
APPROVED
0203-04228 5
UP - 0670
BSM DPU
WAVE BUFFER
12 / 19
1991 - 1 - 23
日本光電
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
23-Jan-91 19:08:59 FILE: 0670-12
IC706
4051
VDD
VSS
VEE
INH
X0
X1
X2
X3
X4
X5
X6
X7
MPX (14OC)
XLMA6 (8O1C)
LMA (112D)(130D)(160D)
LMA2
LMA3
LMA4
C718 0.1U
C719 0.1U
0V
-8V
IC703 D uPC450
IC703 C uPC450
IC703 B uPC450
IC703 A uPC450
IC704 A uPC450
IC704 D uPC450
IC704 B uPC450
IC704 C uPC450
C709 0.01U
C710 0.01U
C711 0.01U
C712 0.01U
C713 0.01U
C714 0.01U
C715 0.01U
R766 10K
R767 10K
R768 10K
R769 10K
R770 10K
R771 10K
R772 10K
R751
R752
R753
R754
R755
R756
R757
100K x 7
CN103
HA7
HAB
PARA
CN102
1DH
AUX1H
AUX2H
MDH
(154A) ADH

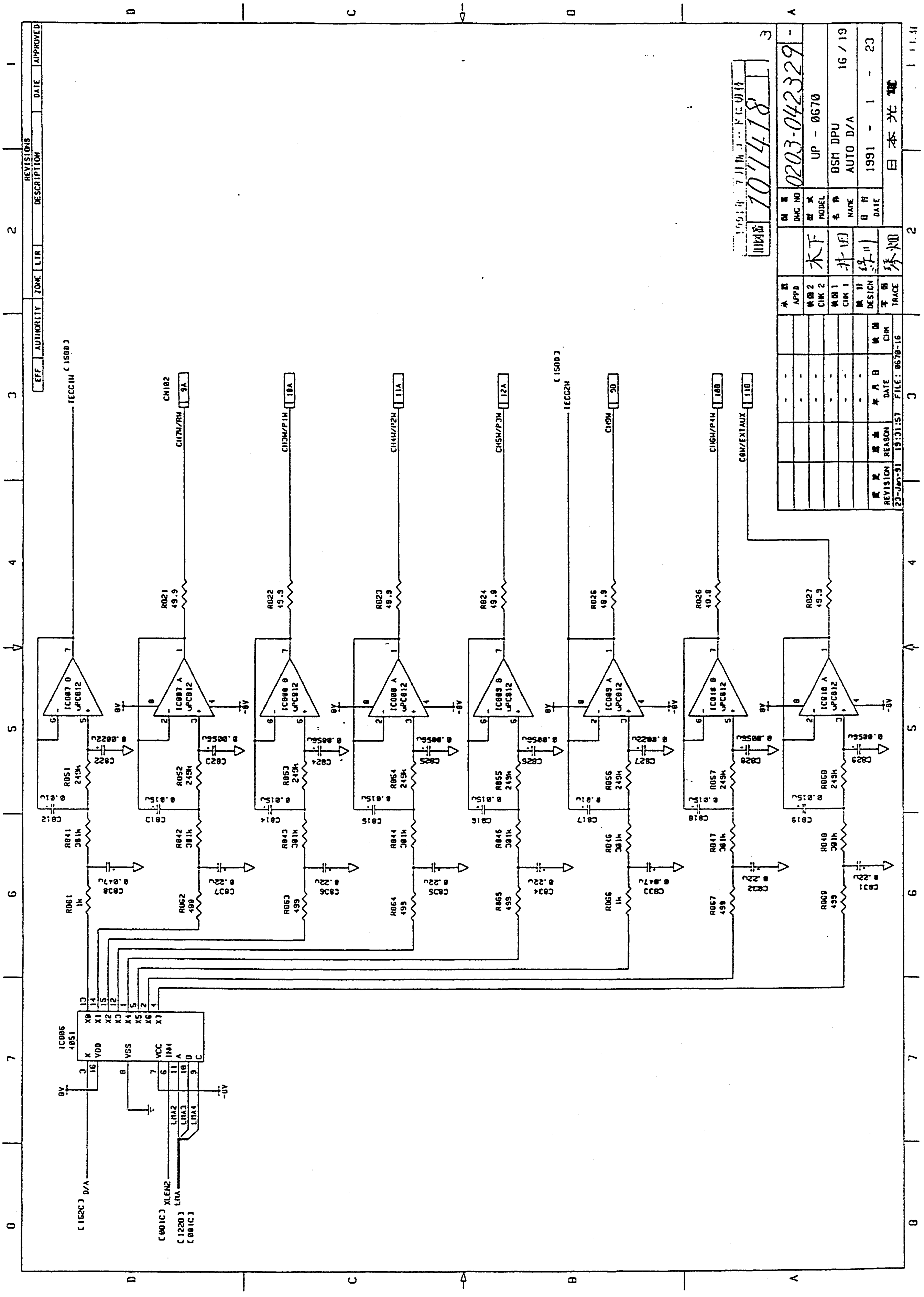

0203-042294
UP - 0670
OSM DPU
PEAK HOLD
13 / 19
1991 - 1 - 23
日本光電
1991年 7月
107415
23-Jan-91 19:11:07 FILE: 0670-13
REVISIONS
EFF
AUTHORITY
ZONE
LTR
DESCRIPTION
DATE
APPROVED
ECG1 [117D]
ECG2 [117D]
IC716, IC717
7PIN : VEE = -0V
8PIN : VSS = E1
16PIN : VDD = +0V
IC713 A uPC012
IC713 B uPC012
IC711 A uPC012
IC711 B uPC012
IC712 A uPC012
IC712 B uPC012
IC714 A uPC012
IC714 B uPC012
IC715 A uPC012
IC715 B uPC012
R715 10k
R716 10k
R725 10k
R726 10k
R713 10k
R714 10k
R723 10k
R724 10k
R711 10k
R712 10k
R721 10k
R722 10k
R727 100
R728 100
C721 0.01u
C722 0.01u
C723 0.01u
C724 0.01u
D711 1SS184
D712 1SS184
D713 1SS184
D714 1SS184
IC716 4051
IC717 4051
LMA2
LMA3
LMA4
[171D] ECG1AD
[171D] ECG2AD
[001C] [122D] LMA
[154D] XLEN1

12. CIRCUIT DIAGRAM


0203 - 042302
UP - 0670
DSM DPU
AUTO A/D
14 / 19
1991 - 1 - 23
日本光電
REVISIONS
IC726 MB8421-90L
IC726 AD574
IC724 μPC649C
IC721 A μPC812
IC721 D μPC812
IC723 4051
IC722 LT1009
IC804 A μPC812
A/D GAIN
A/D ZERO
H GAIN
REF2.5
DD0~DD7
D0~D7
A1~A11
XHRLS
XADRCS
XRDLS
REF10V
IC804 4PIN : -8V 8PIN : +8V
IC722 1,2,3,7 PIN : NC
7 PIN : -8V 16 PIN : +8V
ADSFT
R/XC
CE
HA
MAG
XADHR
XCS
XOE
CA0
G1
G2
HPX


0203-042311
UP - 0670
BSM DPU
AUTO D/A
15 / 19
1991 - 1 - 23
FILE: 0670-15
25-Jan-91 19:27:31
REVISIONS
IC001 11A17012
IC011 74HC4094
IC014 4053
IC005 14504
IC081 74HC374
IC082 74HC374
IC012 A uPC812
IC012 B uPC812
IC013 A uPC812
IC013 B uPC812
IC004 B uPC812
IC015 A uPC812
IC015 B uPC812
VR104 100
DA GAIN
VR105 100
DA ZERO
CN102
CN105
D/A
PECC2H
PECC1H
ADSFT
ECC1H
ECC2H
TECC2H
TECC1H
XSTR
DATA
DD0-DD7
L1
L2
REFINV
SB
EN1
RSS1
ADW
XLEN1

12. CIRCUIT DIAGRAM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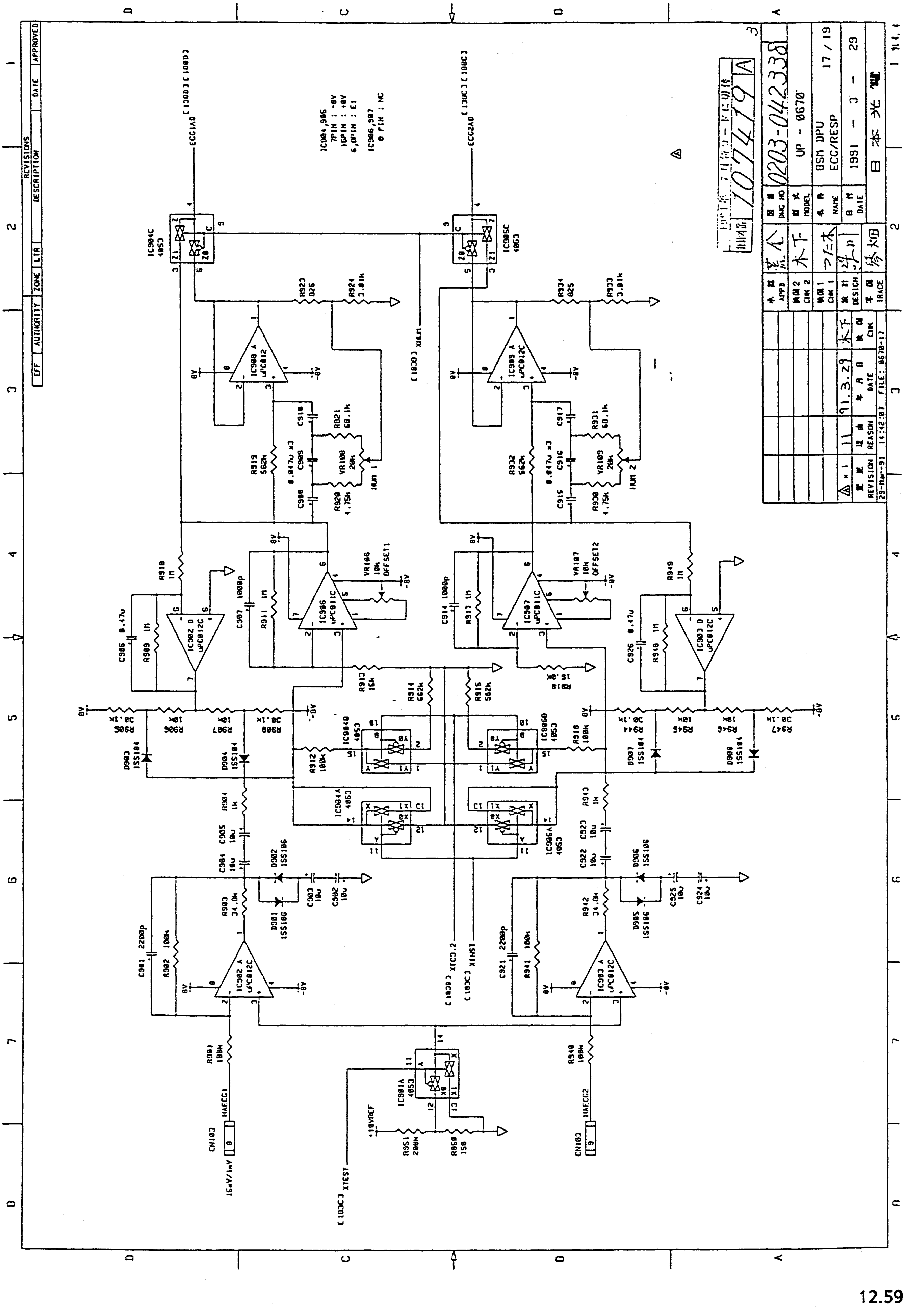
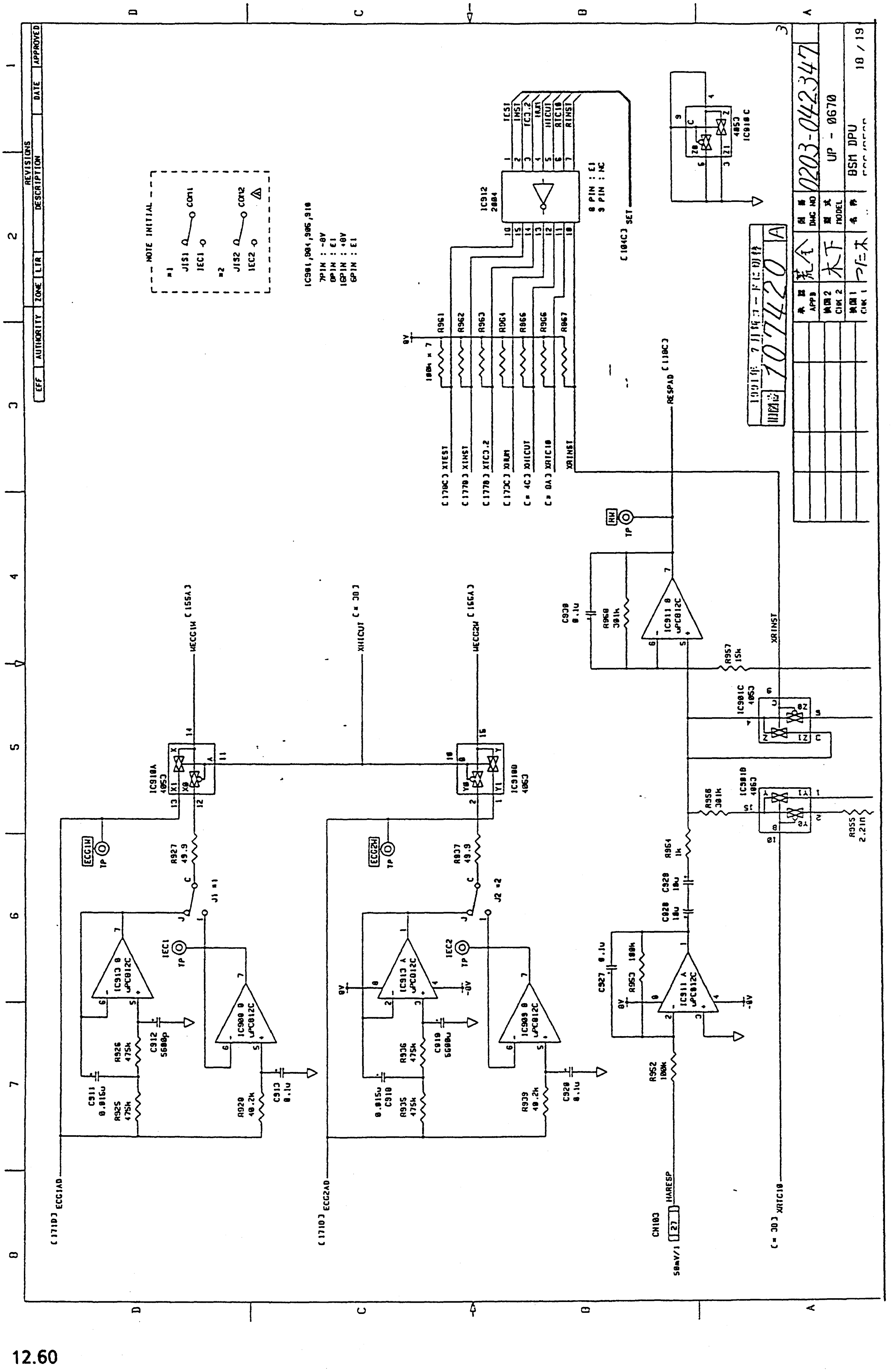
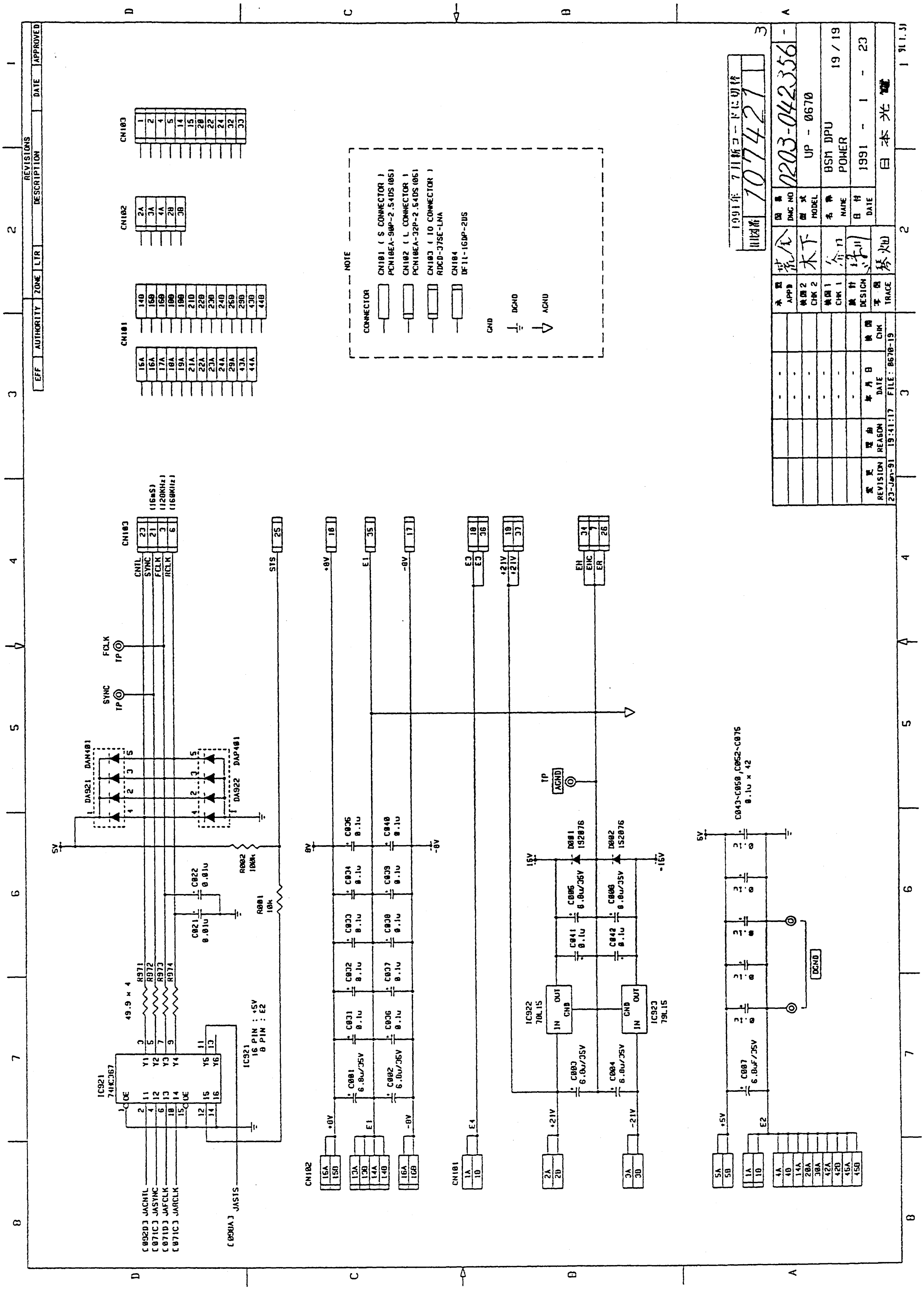
DSM DPU
AUTO D/A
16 / 19
1991 - 1 - 23
日本光電
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
23-Jan-91 19:31:57
FILE: 0G70-16
REVISIONS
EFF
AUTHORITY
ZONE
LTR
DESCRIPTION
DATE
APPROVED
TECC1H
TECC2H
CN102
CH7H/RH
CH3H/P1H
CH4H/P2H
CH5H/P3H
CH1H
CH6H/P4H
C0H/EXTAUX
9A
10A
11A
12A
9B
10B
11B
R021 49.9
R022 49.9
R023 49.9
R024 49.9
R025 49.9
R026 49.9
R027 49.9
IC087 B uPC812
IC087 A uPC812
IC088 B uPC812
IC088 A uPC812
IC089 B uPC812
IC089 A uPC812
IC010 B uPC812
IC010 A uPC812
8V
-8V
R051 249k
R052 249k
R053 249k
R054 249k
R055 249k
R056 249k
R057 249k
R060 249k
C822 0.0022u
C823 0.0056u
C824 0.0056u
C825 0.0056u
C826 0.0056u
C827 0.0022u
C828 0.0056u
C829 0.0056u
C812 0.01u
C813 0.015u
C814 0.015u
C815 0.015u
C816 0.015u
C817 0.01u
C818 0.015u
C819 0.015u
R041 301k
R042 301k
R043 301k
R044 301k
R045 301k
R046 301k
R047 301k
R040 301k
C838 0.047u
C837 0.22u
C836 0.22u
C835 0.22u
C834 0.22u
C833 0.047u
C832 0.22u
C831 0.22u
R061 1k
R062 499
R063 499
R064 499
R065 499
R066 1k
R067 499
R069 499
IC006 4051
X0 X1 X2 X3 X4 X5 X6 X7
X VDD VSS VCC INH A B C
0V
-8V
LMA2
LMA3
LMA4
D/A
XLEN2
LMA
[152C]
[150D]
[001C]
[122D]
[001C]

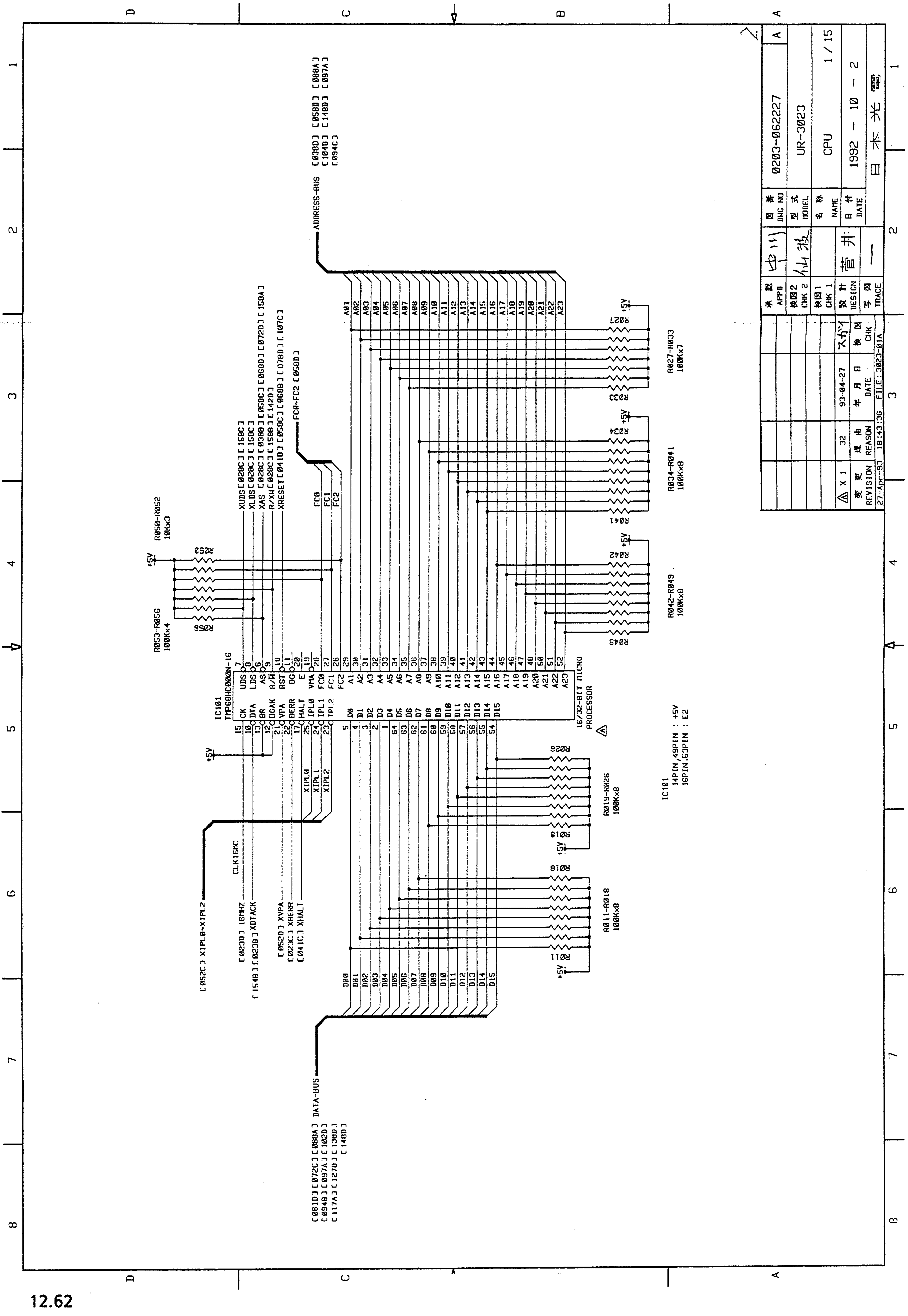

REVISIONS
EFF
AUTHORITY
ZONE
LTR
DESCRIPTION
DATE
APPROVED
ECC1AD
ECC2AD
[10D] [10D]
[10C] [10C]
IC904,906 7PIN : -8V 16PIN : +8V 6,8PIN : E1
IC906,907 8 PIN : NC
IC904C 4053
IC905C 4053
R923 825
R924 3.01k
R934 825
R933 3.01k
XHUM
IC908 A uPC812
IC909 A uPC812C
C910
C917
R921 60.1k
R931 60.1k
R919 562k
R932 562k
0.047u x3 C909
0.047u x3 C916
VR108 20k HUM 1
VR109 20k HUM 2
C908
C915
R920 4.75k
R930 4.75k
R910 1M
R949 1M
VR106 10k OFFSET1
VR107 10k OFFSET2
IC906 uPC811C
IC907 uPC811C
C907 1000p
C914 1000p
R911 1M
R917 1M
IC902 B uPC812C
IC903 B uPC812C
C906 0.47u
C926 0.47u
R909 1M
R948 1M
R913 15k
R914 562k
R915 562k
R918 15.0k
R905 30.1k
R906 10k
R907 10k
R908 30.1k
R944 30.1k
R945 10k
R946 10k
R947 30.1k
D903 1SS184
D904 1SS184
D907 1SS184
D908 1SS184
IC904B 4053
IC906B 4053
R912 100k
R916 100k
IC904A 4053
IC906A 4053
R904 1k
R943 1k
C905 10u
C904 10u
C923 10u
C922 10u
D902 1SS106
D901 1SS106
D906 1SS106
D905 1SS106
C903 10u
C902 10u
C925 10u
C924 10u
R903 34.0k
R942 34.0k
C901 2200p
R902 100k
C921 2200p
R941 100k
IC902 A uPC812C
IC903 A uPC812C
XIC3.2
XINST
[10C]
R901 100k
R940 100k
HAECC1
HAECC2
CN103
15mV/1mV
IC901A 4053
+10VREF
R951 200k
R950 150
XTEST
[10C]
0V
+8V
-8V
3
1074179 A
0203-042338
図番 DWG NO
機種 MODEL
UP - 0670
名称 NAME
BSM DPU
ECC/RESP
17 / 19
日付 DATE
1991 - 3 - 29
日本光電
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
製図 TRACE
木下
REVISION
REASON
DATE
CHK
91.3.29
29-Mar-91 14:42:07
FILE: 0670-17
A
B
C
D
1
2
3
4
5
6
7
8

12. CIRCUIT DIAGRAM

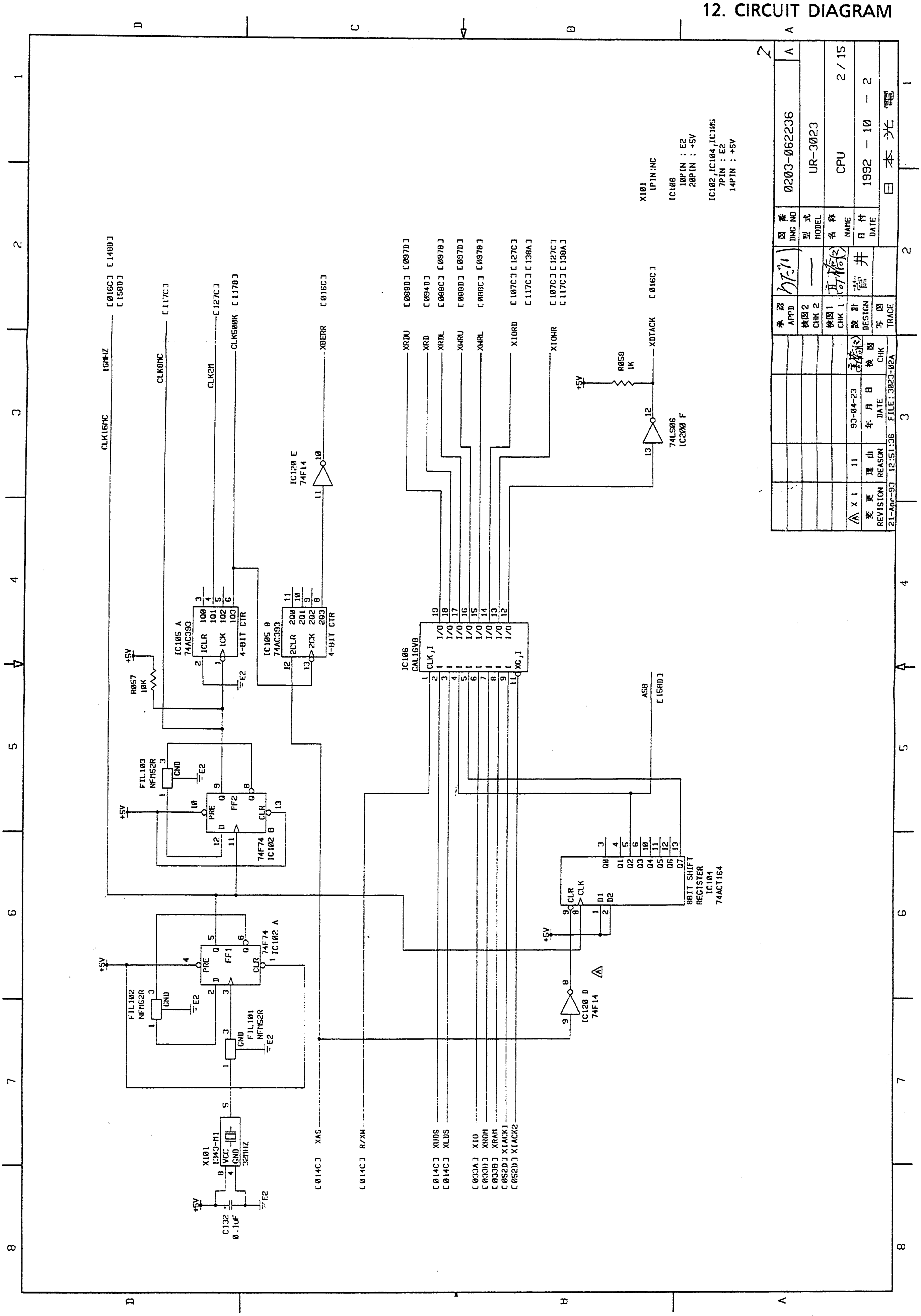

REVISIONS
EFF
AUTHORITY
ZONE
LTR
DESCRIPTION
DATE
APPROVED
NOTE INITIAL
JIS1
IEC1
COM1
JIS2
IEC2
COM2
IC901,904,906,910
7PIN : -8V
8PIN : E1
16PIN : +8V
6PIN : E1
IC912
2004
8 PIN : E1
9 PIN : NC
SET
RESPAD
XTEST
XINST
XTC3.2
XRUM
XHICUT
XRTC10
XRINST
100k × 7
R961
R962
R963
R964
R966
R965
R967
IC910C
4053
IC911 B
uPC812C
IC911 A
uPC812C
IC901C
4053
IC901B
4053
IC910A
4053
IC910B
4053
IC913 B
uPC812C
IC913 A
uPC812C
IC908 B
uPC812C
IC909 B
uPC812C
WECG1W
WECG2W
XHICUT
XRINST
ECG1W
ECG2W
IEC1
IEC2
TP
J1 *1
J2 *2
R927 49.9
R937 49.9
R926 475k
R925 475k
R936 475k
R935 475k
R928 40.2k
R939 40.2k
R952 100k
R953 100k
R954 1k
R955 2.21M
R956 301k
R957 15k
R969 301k
C911 0.015u
C912 5600p
C913 0.1u
C918 0.015u
C919 5600p
C920 0.1u
C927 0.1u
C928 10u
C929 10u
C930 0.1u
ECG1AD
ECG2AD
HARESP
CN103
50mV/1
0203-042347
UP - 0670
BSM DPU
10 / 19
107420 A
D
C
B
A
1
2
3
4
5
6
7
8

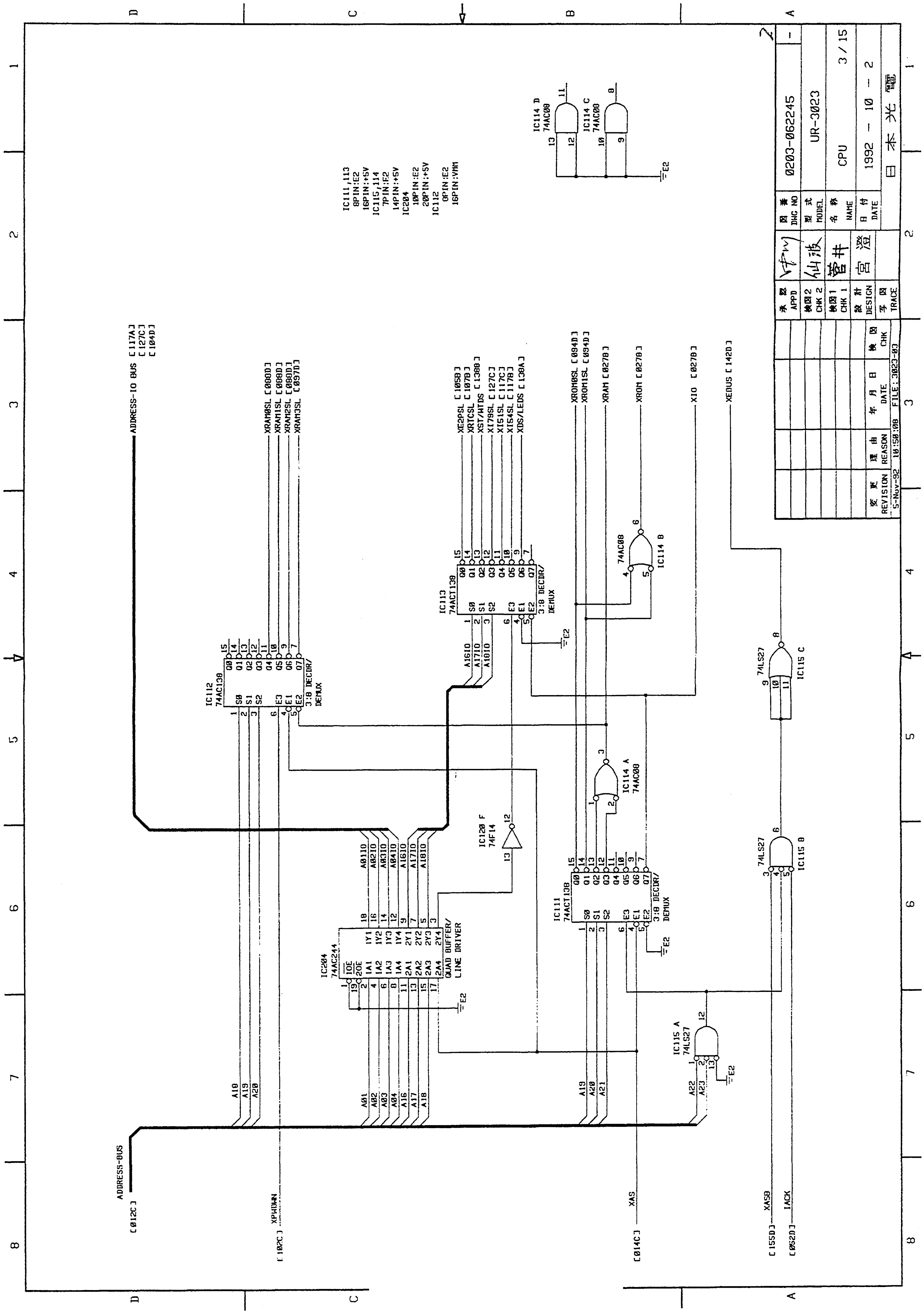

REVISIONS
EFF
AUTHORITY
ZONE
LTR
DESCRIPTION
DATE
APPROVED
CN101
CN102
CN103
CN104
NOTE
CONNECTOR
CN101 (S CONNECTOR) PCN10EA-90P-2.54DS(05)
CN102 (L CONNECTOR) PCN10EA-32P-2.54DS(05)
CN103 (IO CONNECTOR) RDCD-37SE-LNA
CN104 DF11-16DP-2DS
GND
DGND
AGND
CNIL
SYNC
FCLK
RCLK
(16mS)
(120KHz)
(160KHz)
STS
+8V
E1
-8V
E3
+21V
EH
EHC
ER
FCLK TP
SYNC TP
DA921 DAN401
DA922 DAP401
5V
R002 100k
R001 10k
C022 0.01u
C021 0.01u
49.9 × 4
R971
R972
R973
R974
IC921 74HC367
IC921 16 PIN : +5V 8 PIN : E2
[C092D] JACNIL
[C071C] JASYNC
[C071D] JAFCLK
[C071C] JARCLK
[C090A] JASTS
C036 0.1u
C040 0.1u
C034 0.1u
C039 0.1u
C033 0.1u
C038 0.1u
C032 0.1u
C037 0.1u
C031 0.1u
C036 0.1u
C001 6.8u/35V
C002 6.8u/35V
8V
-8V
TP AGND
D001 1S2076
D002 1S2076
15V
-15V
C005 6.8u/35V
C006 6.8u/35V
C041 0.1u
C042 0.1u
IC922 78L15
IC923 79L15
IN
OUT
GND
C003 6.8u/35V
C004 6.8u/35V
+21V
-21V
E4
C043-C050,C052-C075 0.1u × 42
C007 6.8uF/35V
DGND
+5V
E2
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
トレース TRACE
荒沢
木下
金子
浅川
秋山
図番 DWG NO 0203-042356 -
機種 MODEL UP-0670
名称 NAME BSM DPU POWER 19/19
日付 DATE 1991 - 1 - 23
日本光電
1991年7月16日(コード化)用
旧図番 1074271
3
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
23-Jan-91 19:41:17
FILE: 0670-19
A
B
C
D
1
2
3
4
5
6
7
8

12. CIRCUIT DIAGRAM

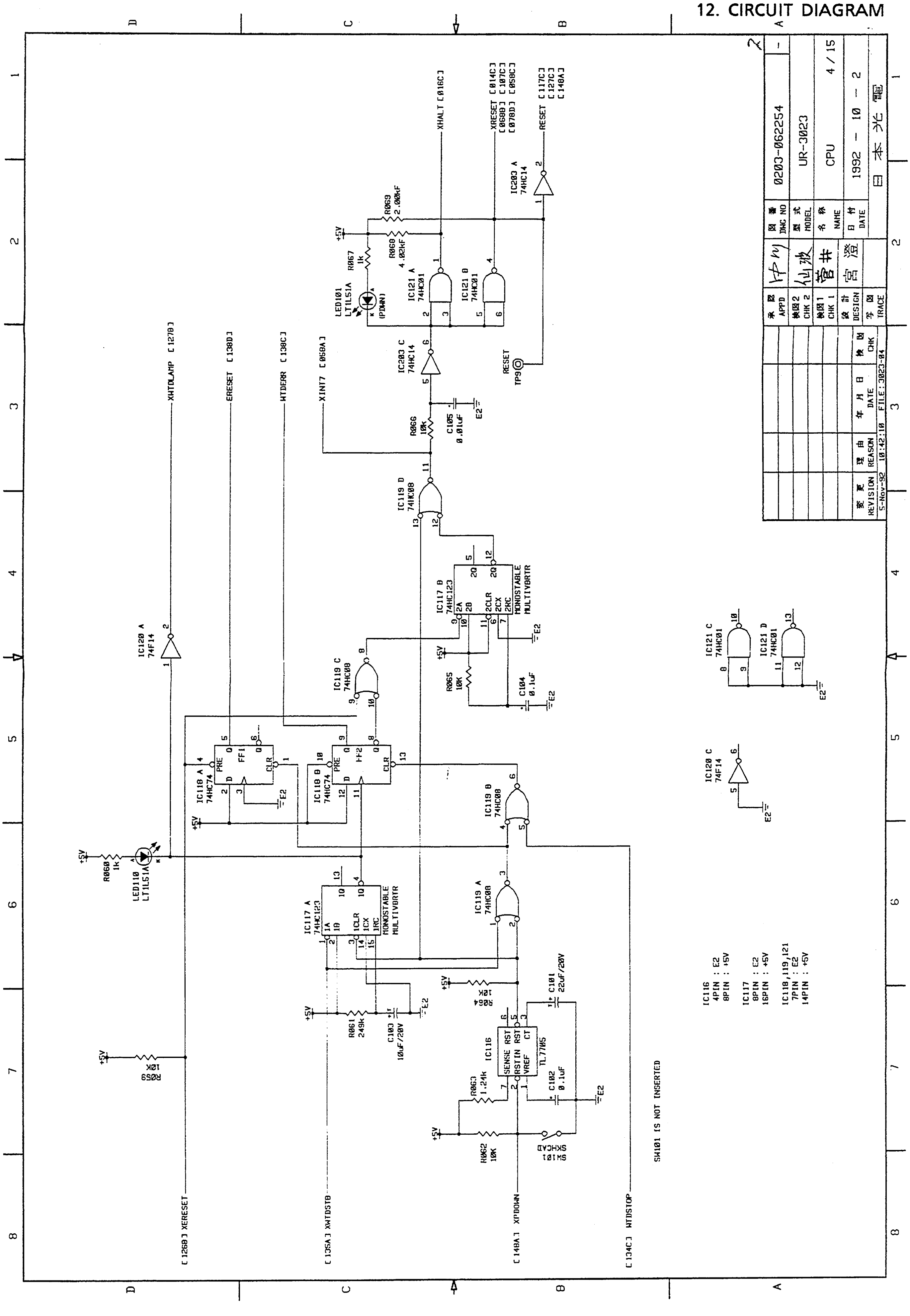

IC101
TMP68HC000N-16
16/32-BIT MICRO PROCESSOR
IC101
14PIN,49PIN : +5V
16PIN,53PIN : E2
ADDRESS-BUS
DATA-BUS
FC0~FC2
XIPL0~XIPL2
CLK16MC
16MHZ
XDTACK
XVPA
XBERR
XHALT
XUDS
XLDS
XAS
R/XW
XRESET
R050-R052 10Kx3
R053-R056 100Kx4
R027-R033 100Kx7
R034-R041 100Kx8
R042-R049 100Kx8
R019-R026 100Kx8
R011-R018 100Kx8
+5V
0203-062227
UR-3023
CPU
1/15
1992 - 10 - 2
日本光電
図番 DWG NO
型式 MODEL
名称 NAME
日付 DATE
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
93-04-27
FILE:3023-01A
27-Apr-93 18:43:36

12. CIRCUIT DIAGRAM

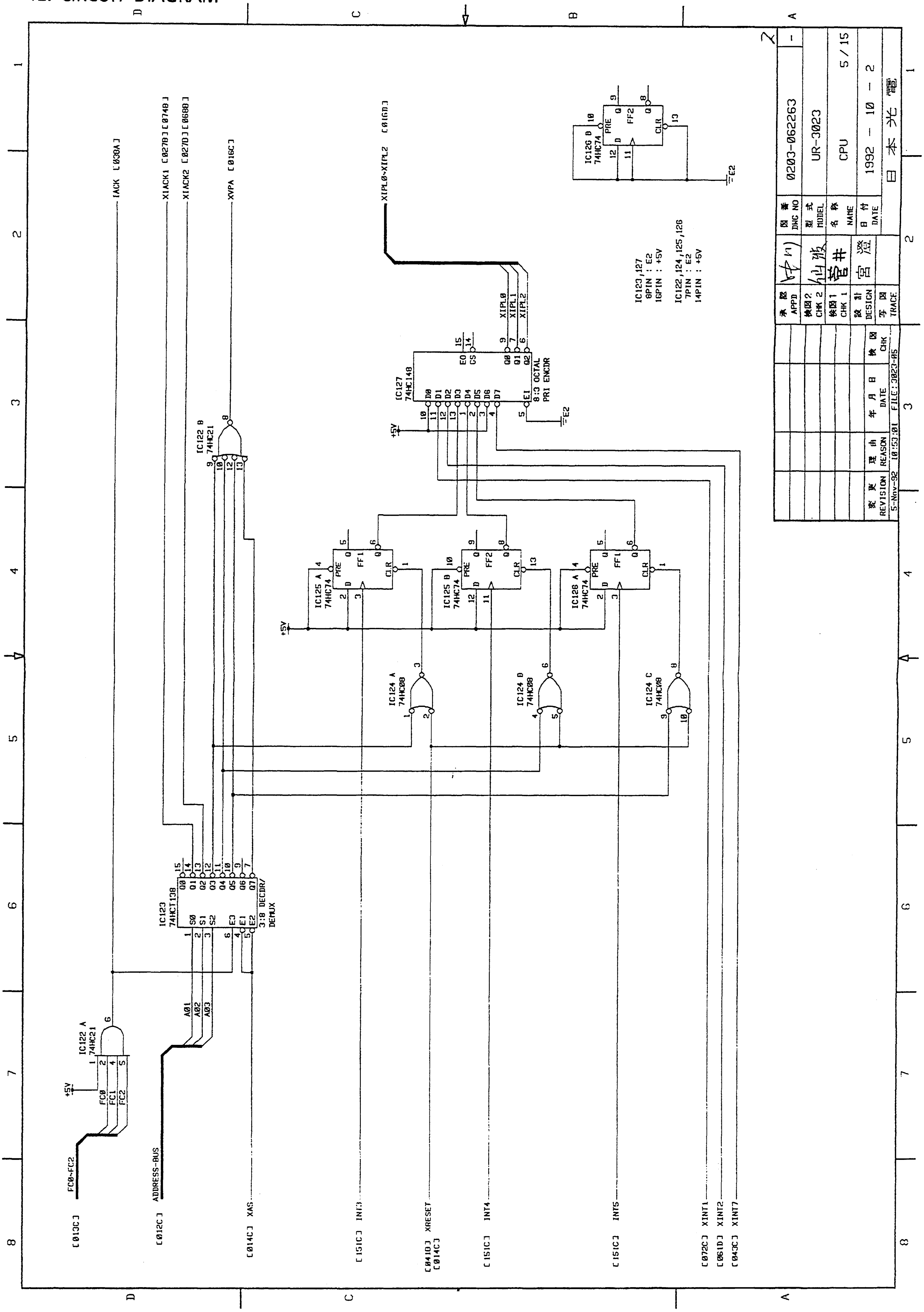

0203-062236
UR-3023
CPU
2 / 15
1992 - 10 - 2
日本光電
図番 DWG NO
型式 MODEL
名称 NAME
日付 DATE
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
X 1
11
93-04-23
21-Apr-93 12:51:36
FILE:3023-02A
X101 1PIN:NC
IC106 10PIN : E2 20PIN : +5V
IC102,IC104,IC105 7PIN : E2 14PIN : +5V
CLK16MC
16MHZ
[016C] [140B]
[158D]
CLK8MC
[117C]
CLK2M
[127C]
CLK500K
[117B]
XBERR
[016C]
IC120 E 74F14
XRDU [080D] [097D]
XRD [094D]
XRDL [088C] [097B]
XWRU [080D] [097D]
XWRL [088C] [097B]
XIORD [107C] [127C] [117C] [138A]
XIOWR [107C] [127C] [117C] [138A]
XDTACK [016C]
R058 1K
+5V
74LS06 IC200 F
IC105 A 74AC393 4-BIT CTR
1CLR 1CK 1Q0 1Q1 1Q2 1Q3
IC105 B 74AC393 4-BIT CTR
2CLR 2CK 2Q0 2Q1 2Q2 2Q3
R057 10K
E2
IC106 GAL16V8
CLK,I I I/O XG,I
AS0 [158D]
FIL103 NFM52R
GND
PRE Q FF2 Q CLR D
74F74 IC102 B
8BIT SHIFT REGISTER IC104 74ACT164
CLR CLK D1 D2 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
FF1
74F74 IC102 A
FIL102 NFM52R
FIL101 NFM52R
IC120 D 74F14
X101 1343-M1 VCC GND 32MHZ
C132 0.1uF
[014C] XAS
[014C] R/XW
[014C] XUDS
[014C] XLDS
[003A] XIO
[003B] XROM
[003B] XRAM
[052D] XIACK1
[052D] XIACK2
A B C D
1 2 3 4 5 6 7 8

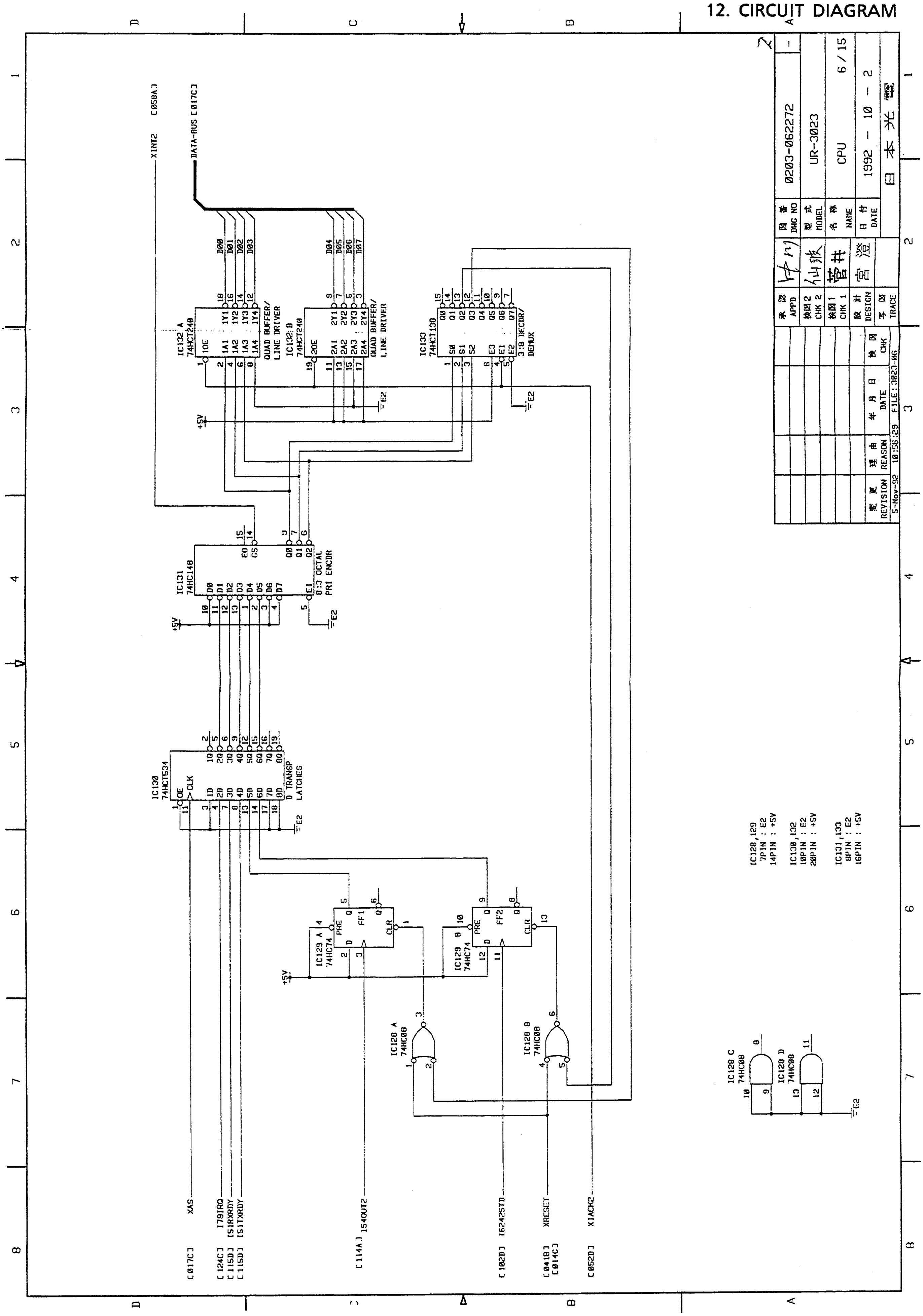


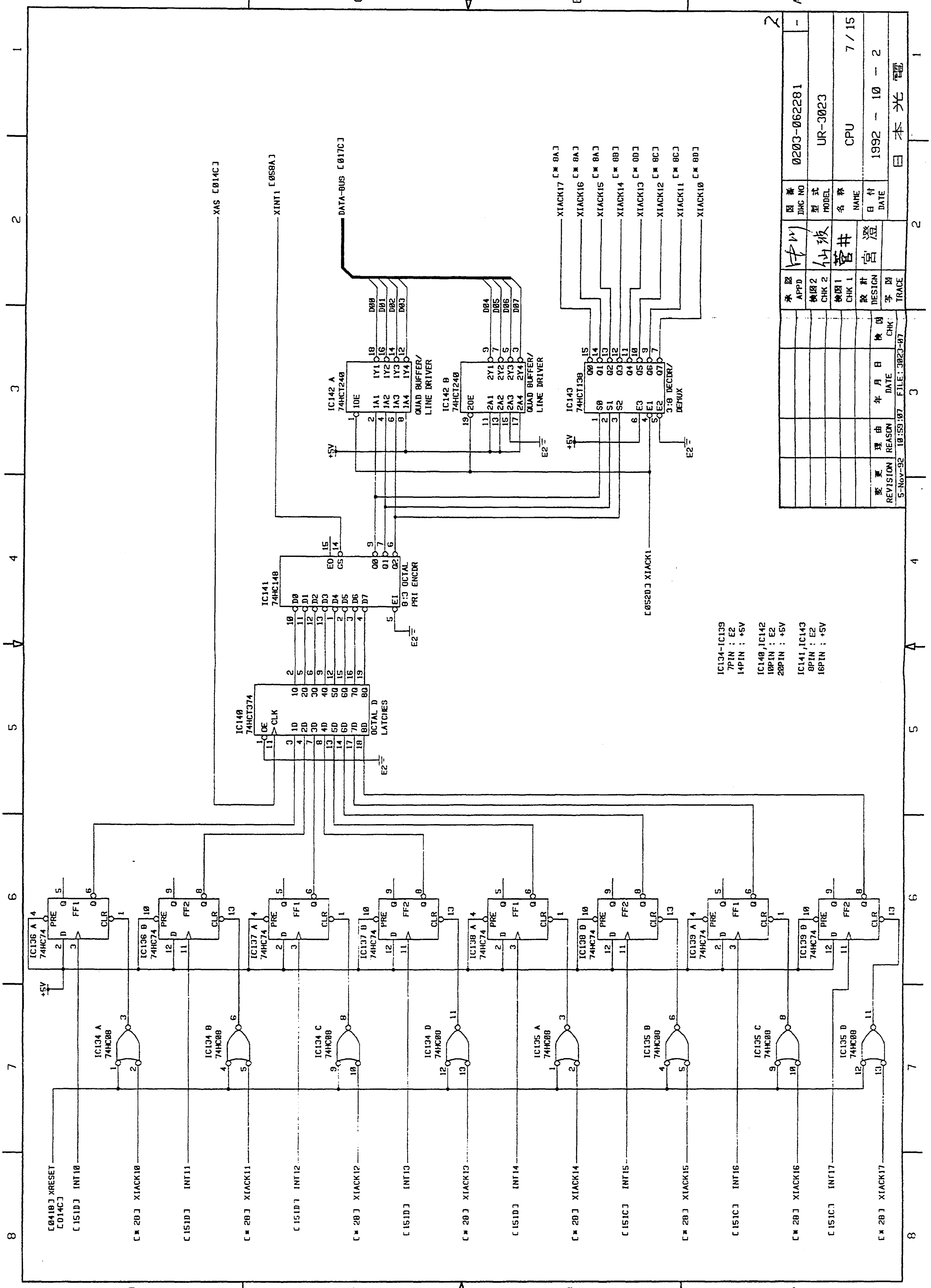
IC114 D
74AC00
IC114 C
74AC00
IC111,113
8PIN:E2
16PIN:+5V
IC115,114
7PIN:E2
14PIN:+5V
IC204
10PIN:E2
20PIN:+5V
IC112
8PIN:E2
16PIN:VHH
ADDRESS-IO BUS [117A] [127C] [104D]
XRAM0SL [080D]
XRAM1SL [080D]
XRAM2SL [080D]
XRAM3SL [097D]
XE2PSL [105B]
XRTCSL [107B]
XST/HTDS [130B]
XI79SL [127C]
XI51SL [117C]
XI54SL [117B]
XDS/LEDS [130A]
XROM0SL [094D]
XROM1SL [094D]
XRAM [027B]
XROM [027B]
XIO [027B]
XEBUS [142D]
IC112
74AC138
3:8 DECDR/
DEMUX
IC113
74ACT138
3:8 DECDR/
DEMUX
74AC08
IC114 B
74LS27
IC115 C
IC114 A
74AC08
IC120 F
74F14
74LS27
IC115 B
IC111
74ACT138
3:8 DECDR/
DEMUX
IC204
74AC244
QUAD BUFFER/
LINE DRIVER
IC115 A
74LS27
A0110
A0210
A0310
A0410
A1610
A1710
A1810
A16
A17
A18
A18
A19
A20
A01
A02
A03
A04
A19
A20
A21
A22
A23
ADDRESS-BUS
[012C]
XPWDWN
[102C]
XAS
[014C]
XAS0
[155D]
IACK
[052D]
E2
0203-062245
UR-3023
CPU
3 / 15
1992 - 10 - 2
日 本 光 電
図 番 DWG NO
型 式 MODEL
名 称 NAME
日 付 DATE
承 認 APPD
検図2 CHK 2
検図1 CHK 1
設 計 DESIGN
写 図 TRACE
変 更 REVISION
理 由 REASON
年 月 日 DATE
検 図 CHK
5-Nov-92 10:50:08 FILE:3023-03

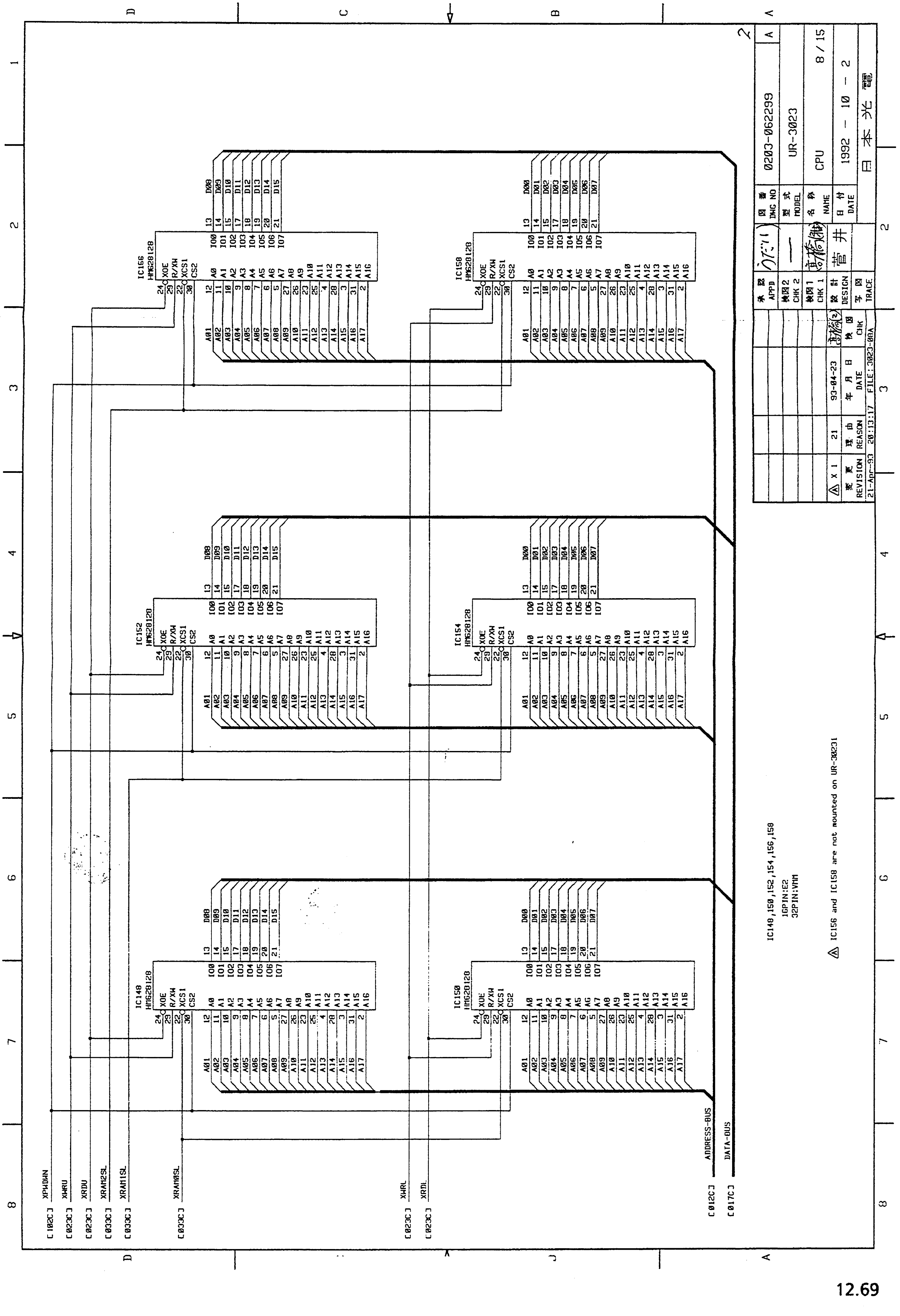

0203-062254
UR-3023
CPU
4 / 15
1992 - 10 - 2
日本光電
FILE:3023-04
5-Nov-92 10:42:10
XHALT [016C]
XRESET [014C] [060D] [070D] [107C] [058C]
RESET [117C] [127C] [140A]
XHTDLAMP [127D]
ERESET [138D]
HTDERR [138C]
XINT7 [058A]
IC203 A 74HC14
IC203 C 74HC14
IC121 A 74HC01
IC121 B 74HC01
IC121 C 74HC01
IC121 D 74HC01
IC119 A 74HC08
IC119 B 74HC08
IC119 C 74HC08
IC119 D 74HC08
IC117 A 74HC123 MONOSTABLE MULTIVBRTR
IC117 B 74HC123 MONOSTABLE MULTIVBRTR
IC118 A 74HC74
IC118 B 74HC74
IC120 A 74F14
IC120 C 74F14
IC116 TL7705
SENSE RSTIN VREF RST RST CT
LED101 LT1L51A (PDWN)
LED110 LT1L51A
R060 4.02kF
R069 2.00kF
R067 1k
R066 10K
C105 0.01uF
R065 10K
C104 0.1uF
R068 1k
R059 10K
R061 249k
C103 10uF/20V
R064 10K
C101 22uF/20V
R063 1.24k
C102 0.1uF
R062 10K
SW101 SKHCAD
RESET TP9
[126D] XERESET
[135A] XHTDSTB
[140A] XPDOWN
[134C] HTDSTOP
SW101 IS NOT INSERTED
IC116 4PIN : E2 8PIN : +5V
IC117 8PIN : E2 16PIN : +5V
IC118,119,121 7PIN : E2 14PIN : +5V
+5V
E2

12. CIRCUIT DIAGRAM

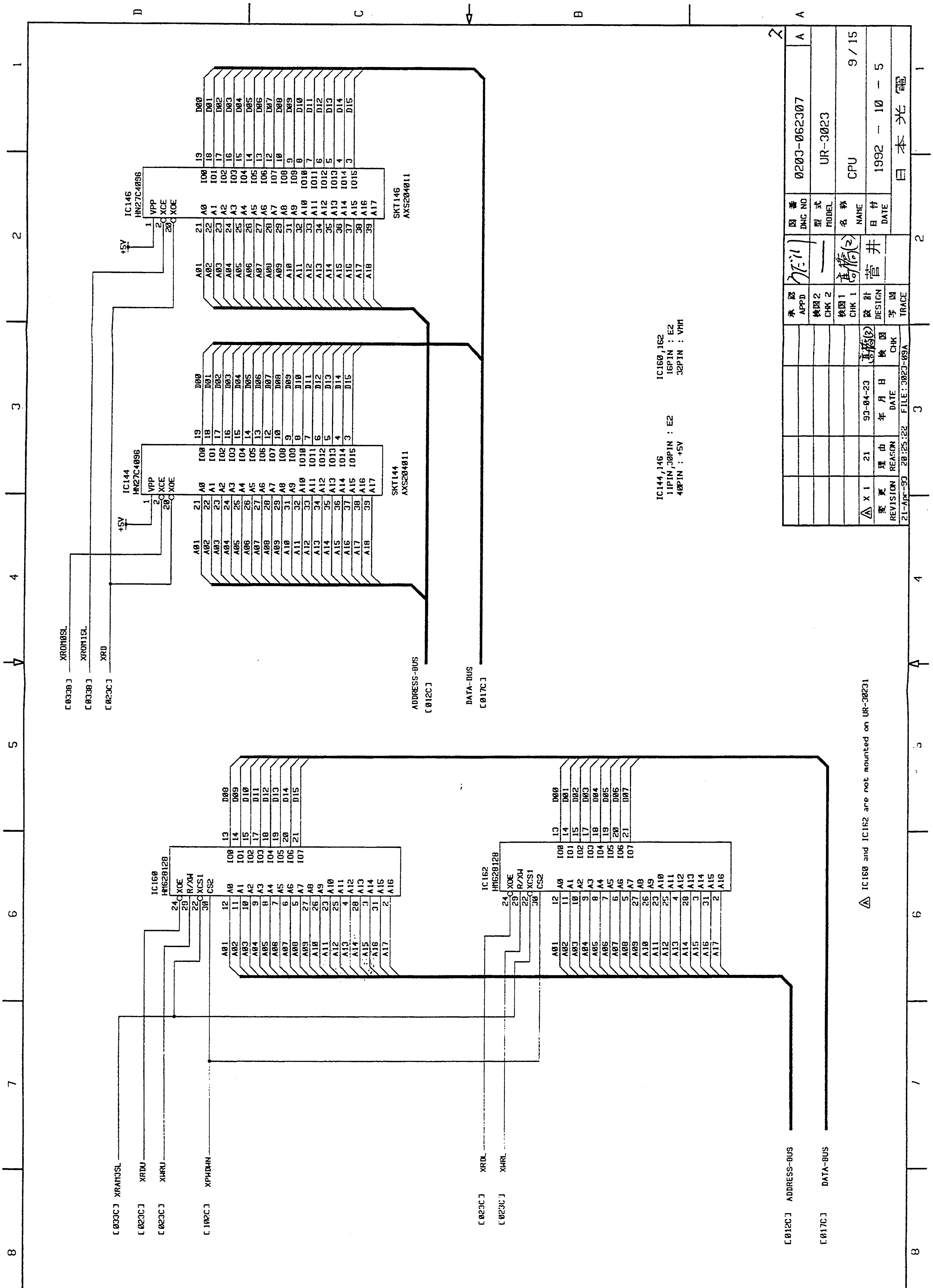

0203-062263
UR-3023
CPU
5 / 15
1992 - 10 - 2
日本光電
FILE:3023-05
5-Nov-92 10:53:01
IC127 74HC148 8:3 OCTAL PRI ENCDR
IC123 74HC138 3:8 DECDR/DEMUX
IC122 A 74HC21
IC122 B 74HC21
IC125 A 74HC74
IC125 B 74HC74
IC126 A 74HC74
IC126 B 74HC74
IC124 A 74HC08
IC124 B 74HC08
IC124 C 74HC08
IC123,127 8PIN : E2 16PIN : +5V
IC122,124,125,126 7PIN : E2 14PIN : +5V
XIPL0~XIPL2 [016D]
XIPL0
XIPL1
XIPL2
IACK [030A]
XIACK1 [027D][074D]
XIACK2 [027D][068D]
XVPA [016C]
FC0~FC2
FC0
FC1
FC2
ADDRESS-BUS
A01
A02
A03
[013C]
[012C]
[014C] XAS
[151C] INT3
[041D] [014C] XRESET
[151C] INT4
[151C] INT5
[072C] XINT1
[061D] XINT2
[043C] XINT7
+5V
E2


0203-062272
UR-3023
CPU 6 / 15
1992 - 10 - 2
日本光電
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
5-Nov-92 10:56:29 FILE:3023-06
XINT2 [050A]
DATA-BUS [017C]
D00
D01
D02
D03
D04
D05
D06
D07
IC132 A 74HCT240 QUAD BUFFER/ LINE DRIVER
IC132 B 74HCT240 QUAD BUFFER/ LINE DRIVER
IC133 74HCT138 3:8 DECDR/ DEMUX
IC131 74HC148 8:3 OCTAL PRI ENCDR
IC130 74HCT534 D TRANSP LATCHES
IC129 A 74HC74 FF1
IC129 B 74HC74 FF2
IC128 A 74HC08
IC128 B 74HC08
IC128 C 74HC08
IC128 D 74HC08
+5V
E2
XAS [017C]
I79IRQ [124C]
I51RXRDY [115D]
I51TXRDY [115D]
I54OUT2 [114A]
I6242STD [102D]
XRESET [041B] [014C]
XIACK2 [052D]
IC128,129 7PIN : E2 14PIN : +5V
IC130,132 10PIN : E2 20PIN : +5V
IC131,133 8PIN : E2 16PIN : +5V

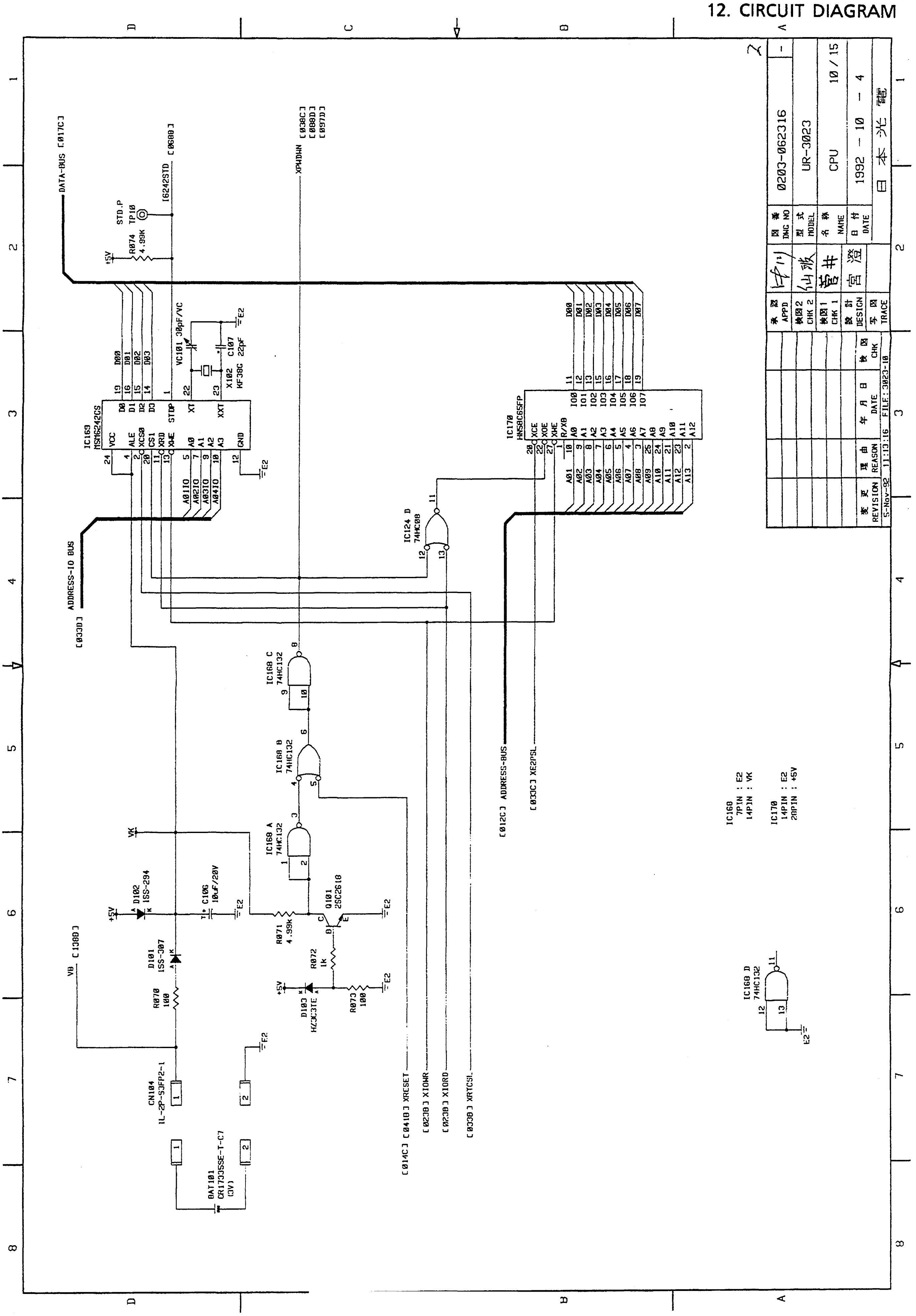

0203-062281
UR-3023
CPU
7 / 15
1992 - 10 - 2
日本光電
図番 DWG NO
型式 MODEL
名称 NAME
日付 DATE
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
5-Nov-92 10:59:07 FILE: 3023-07
XAS [014C]
XINT1 [058A]
DATA-BUS [017C]
XIACK17 [* 8A]
XIACK16 [* 8A]
XIACK15 [* 8A]
XIACK14 [* 8B]
XIACK13 [* 8B]
XIACK12 [* 8C]
XIACK11 [* 8C]
XIACK10 [* 8D]
IC142 A 74HCT240 QUAD BUFFER/ LINE DRIVER
IC142 B 74HCT240 QUAD BUFFER/ LINE DRIVER
IC143 74HCT138 3:8 DECDR/ DEMUX
IC141 74HC148 8:3 OCTAL PRI ENCDR
IC140 74HCT374 OCTAL D LATCHES
[052D] XIACK1
IC134-IC139 7PIN : E2 14PIN : +5V
IC140,IC142 10PIN : E2 20PIN : +5V
IC141,IC143 8PIN : E2 16PIN : +5V
IC136 A 74HC74 FF1
IC136 B 74HC74 FF2
IC137 A 74HC74 FF1
IC137 B 74HC74 FF2
IC138 A 74HC74 FF1
IC138 B 74HC74 FF2
IC139 A 74HC74 FF1
IC139 B 74HC74 FF2
IC134 A 74HC08
IC134 B 74HC08
IC134 C 74HC08
IC134 D 74HC08
IC135 A 74HC08
IC135 B 74HC08
IC135 C 74HC08
IC135 D 74HC08
+5V
E2
[041B] XRESET [014C]
[151D] INT10
[* 2B] XIACK10
[151D] INT11
[* 2B] XIACK11
[151D] INT12
[* 2B] XIACK12
[151D] INT13
[* 2B] XIACK13
[151D] INT14
[* 2B] XIACK14
[151C] INT15
[* 2B] XIACK15
[151C] INT16
[* 2B] XIACK16
[151C] INT17
[* 2B] XIACK17


IC156 HM628128
IC158 HM628128
IC152 HM628128
IC154 HM628128
IC140 HM628128
IC150 HM628128
XOE
R/XW
XCS1
CS2
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16
IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7
A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13 A14 A15 A16 A17
D00 D01 D02 D03 D04 D05 D06 D07
D08 D09 D10 D11 D12 D13 D14 D15
ADDRESS-BUS
DATA-BUS
[012C]
[017C]
[102C] XPWDWN
[023C] XWRU
[023C] XRDU
[033C] XRAM2SL
[033C] XRAM1SL
[033C] XRAM0SL
[023C] XWRL
[023C] XRDL
IC140,150,152,154,156,158
16PIN:E2
32PIN:VMM
IC156 and IC158 are not mounted on UR-3023I
図番 DWG NO 0203-062299
型式 MODEL UR-3023
名称 NAME CPU 8 / 15
日付 DATE 1992 - 10 - 2
日本光電
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN 菅井
写図 TRACE
変更 REVISION X 1
理由 REASON 21
年月日 DATE 93-04-23
検図 CHK
21-Apr-93 20:13:17 FILE:3023-08A
A B C D
1 2 3 4 5 6 7 8

12. CIRCUIT DIAGRAM

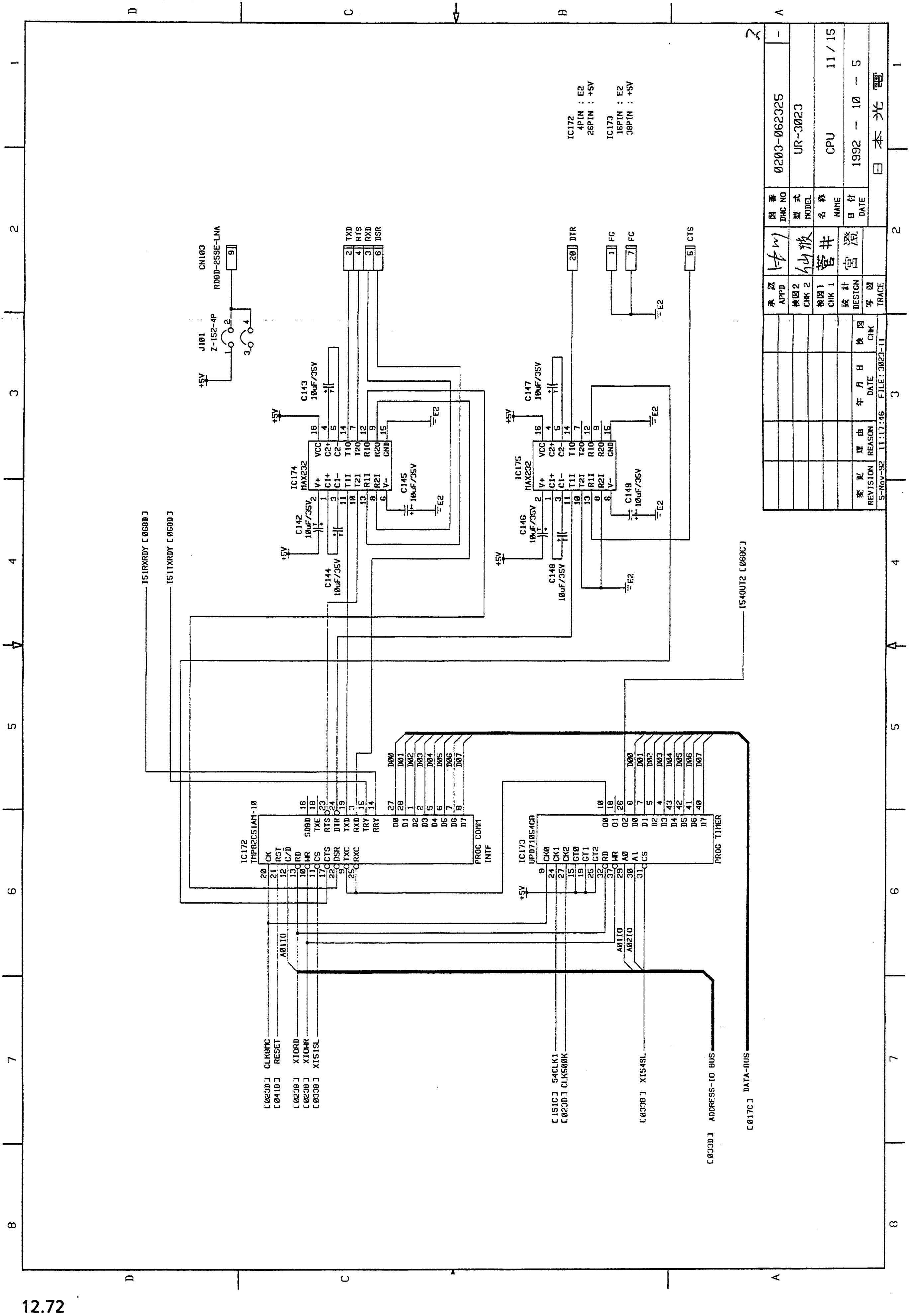

IC146
HN27C4096
SKT146
AXS204011
IC144
HN27C4096
SKT144
AXS204011
IC160
HM628128
IC162
HM628128
+5V
ADDRESS-BUS [012C]
DATA-BUS [017C]
[033B] XROM0SL
[033B] XROM1SL
[023C] XRD
[033C] XRAM3SL
[023C] XRDU
[023C] XWRU
[102C] XPHDWN
[023C] XRDL
[023C] XWRL
IC144,146 11PIN,30PIN : E2 40PIN : +5V
IC160,162 16PIN : E2 32PIN : VMM
IC160 and IC162 are not mounted on UR-3023I
0203-062307
UR-3023
CPU 9/15
1992 - 10 - 5
日本光電
21
93-04-23
FILE:3023-09A
21-Apr-93 20:25:22

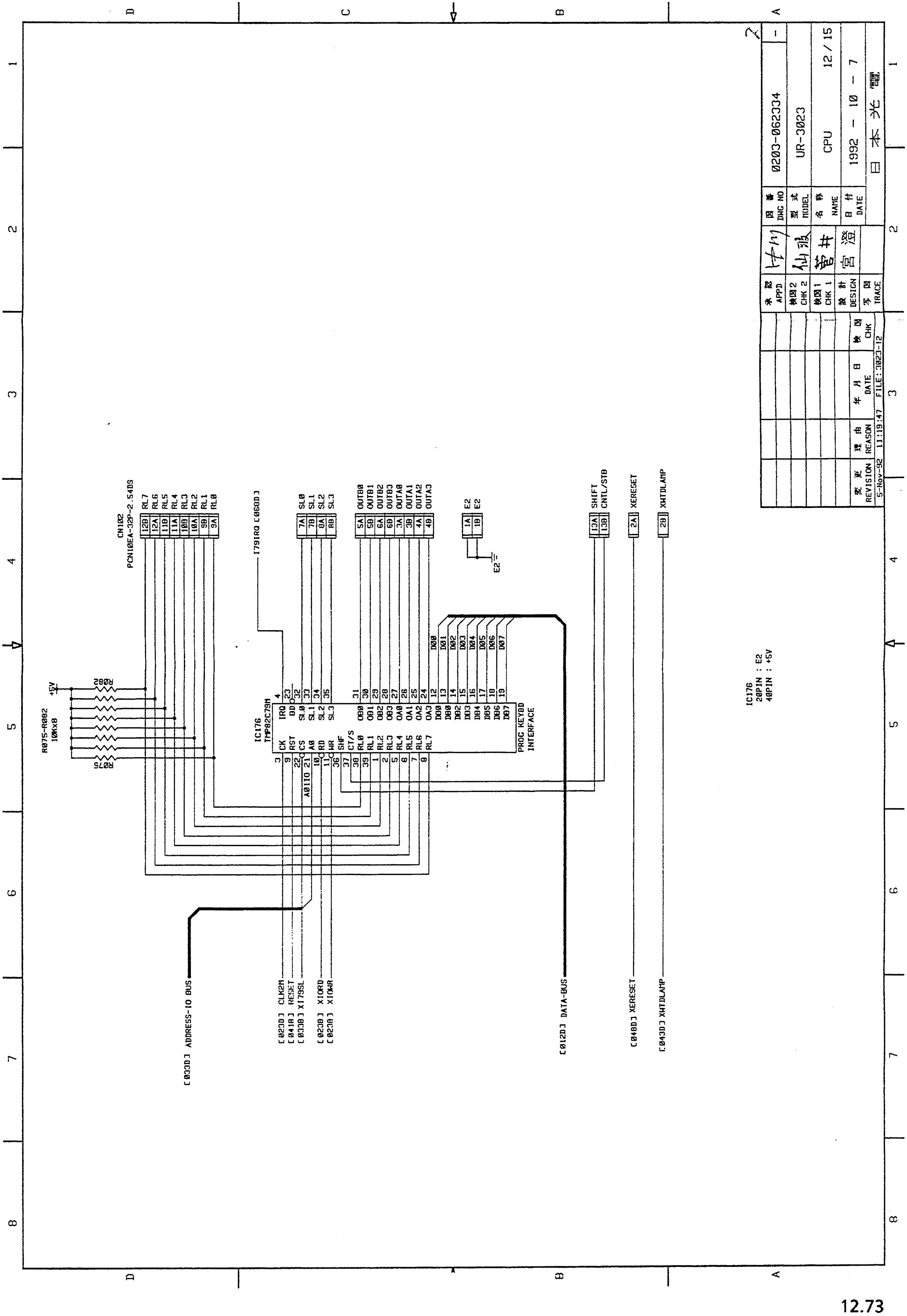
12. CIRCUIT DIAGRAM



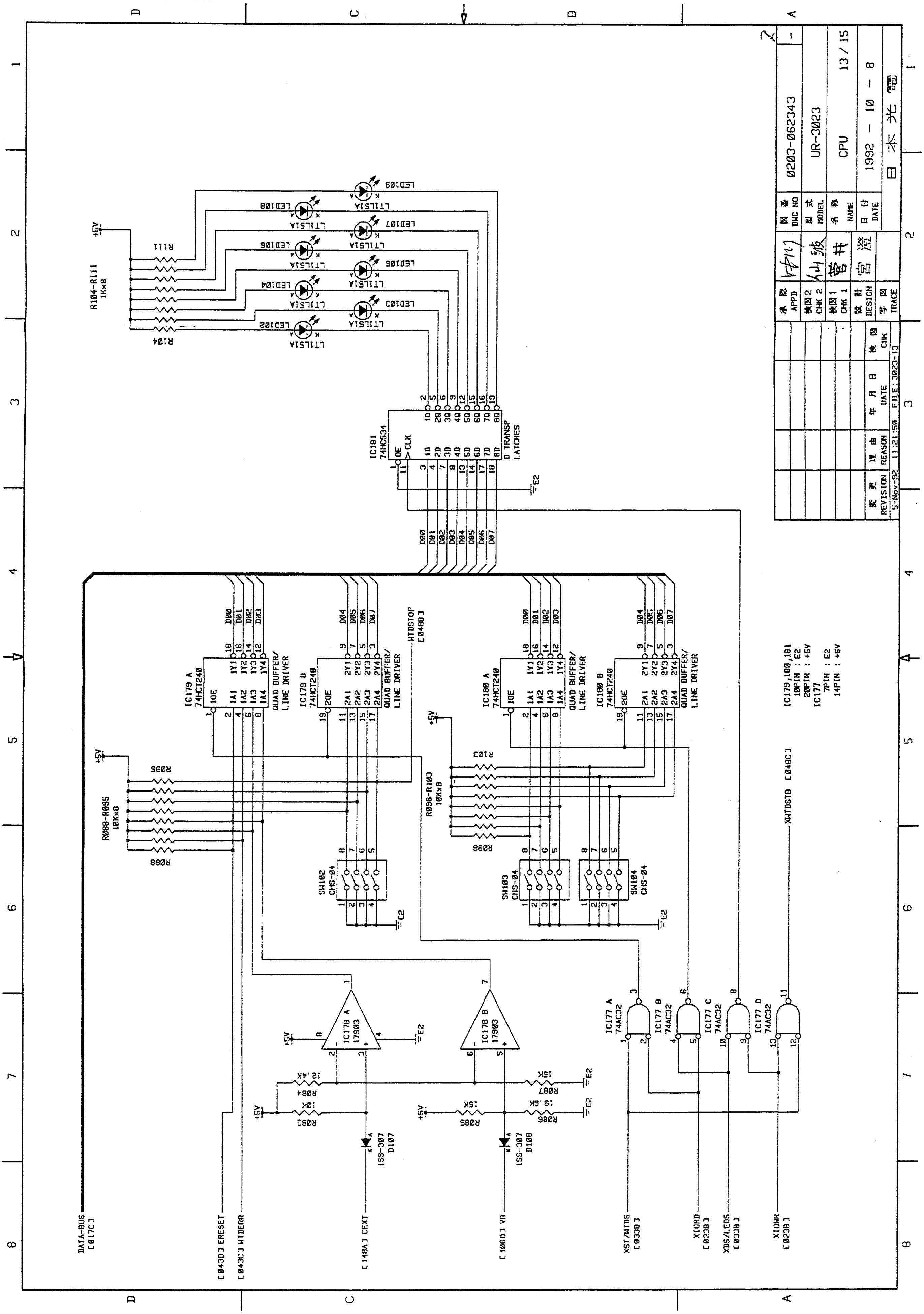
DATA-BUS [017C]
[6242STD [060B]
STD.P TP10
R074 4.99K
+5V
XPWDWN [038C] [080D] [097D]
IC169 MSM6242GS
VCC ALE XCS0 CS1 XRD XWE A0 A1 A2 A3 GND
D0 D1 D2 D3 STDP XT XXT
D00 D01 D02 D03
VC101 30pF/VC
C107 22pF
X102 KF38G
E2
A01IO A02IO A03IO A04IO
ADDRESS-IO BUS [033D]
IC170 HN58C65FP
XCE XOE XWE R/XB A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12
IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7
D00 D01 D02 D03 D04 D05 D06 D07
A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13
IC124 D 74HC08
IC168 C 74HC132
IC168 B 74HC132
IC168 A 74HC132
IC168 D 74HC132
[012C] ADDRESS-BUS
[033C] XE2PSL
IC168 7PIN : E2 14PIN : VK
IC170 14PIN : E2 28PIN : +5V
VK
D102 1SS-294
C106 10uF/20V
D101 1SS-307
R070 100
VB [130D]
R071 4.99K
Q101 2SC2618
R072 1K
D103 HZ3C3TE
R073 100
CN104 IL-2P-S3FP2-1
BAT101 CR1335SE-T-C7 (3V)
[014C] [041D] XRESET
[023B] XIOWR
[023B] XIORD
[003B] XRTCSL
D C B A
1 2 3 4 5 6 7 8
0203-062316
UR-3023
CPU 10 / 15
1992 - 10 - 4
日本光電
図番 DWG NO
型式 MODEL
名称 NAME
日付 DATE
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
5-Nov-92 11:13:16 FILE:3023-10

12. CIRCUIT DIAGRAM


IC172
4PIN : E2
26PIN : +5V
IC173
16PIN : E2
38PIN : +5V
0203-062325
UR-3023
CPU
11/15
1992 - 10 - 5
日本光電
図番 DWG NO
型式 MODEL
名称 NAME
日付 DATE
承認 APP'D
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
5-Nov-92
11:17:46
FILE:3023-11
CN103
RDDD-25SE-LNA
J101
Z-152-4P
+5V
TXD
RTS
RXD
DSR
DTR
FG
FG
CTS
E2
IC174
MAX232
IC175
MAX232
C142 10uF/35V
C143 10uF/35V
C144 10uF/35V
C145 10uF/35V
C146 10uF/35V
C147 10uF/35V
C148 10uF/35V
C149 10uF/35V
VCC C2+ C2- T1O T2O R1O R2O GND
V+ C1+ C1- T1I T2I R1I R2I V-
I51RXRDY [060D]
I51TXRDY [060D]
I54OUT2 [060C]
IC172
TMP82C51AM-10
CK RST C/D RD WR CS CTS DSR TXC RXC
SDBD TXE RTS DTR TXD RXD TRY RRY
D0 D1 D2 D3 D4 D5 D6 D7
PROG COMM INTF
IC173
UPD71054CB
CK0 CK1 CK2 GT0 GT1 GT2 RD WR A0 A1 CS
O0 O1 O2
D0 D1 D2 D3 D4 D5 D6 D7
PROG TIMER
D00 D01 D02 D03 D04 D05 D06 D07
A01IO
A02IO
[020D] CLK8MC
[041D] RESET
[023D] XIORD
[023D] XIOWR
[033D] XI51SL
[151C] 54CLK1
[020D] CLK500K
[033D] XI54SL
[033D] ADDRESS-IO BUS
[017C] DATA-BUS
1 2 3 4 5 6 7 8
A B C D

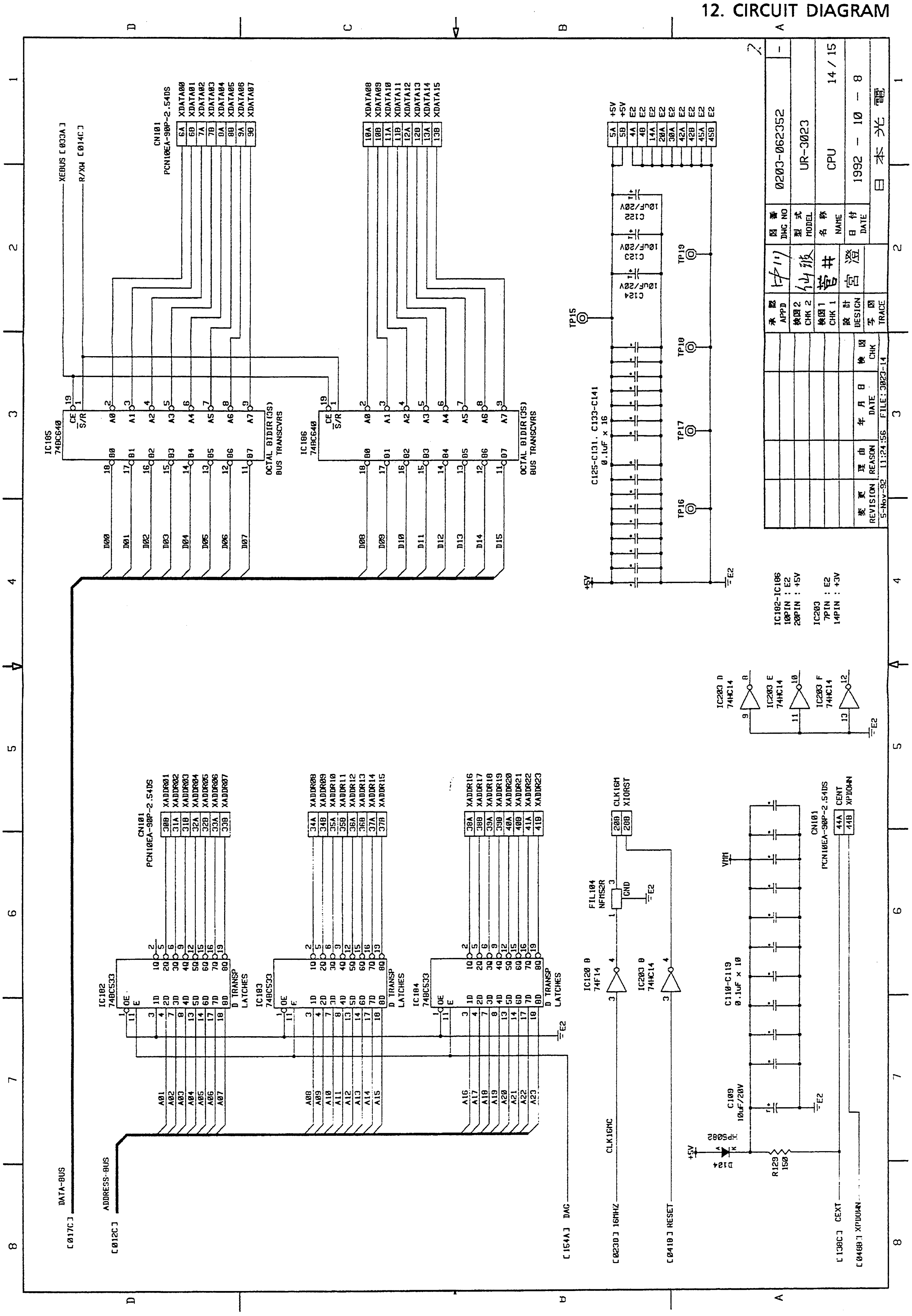

0203-062334
UR-3023
CPU
12 / 15
1992 - 10 - 7
日本光電
図番 DWG NO
型式 MODEL
名称 NAME
日付 DATE
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
菅井
宮澄
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
5-Nov-92 11:19:47 FILE:3023-12
CN102
PCN10EA-32P-2.54DS
RL7 RL6 RL5 RL4 RL3 RL2 RL1 RL0
12B 12A 11B 11A 10B 10A 9B 9A
I79IRQ [060D]
SL0 SL1 SL2 SL3
7A 7B 8A 8B
OUTB0 OUTB1 OUTB2 OUTB3 OUTA0 OUTA1 OUTA2 OUTA3
5A 5B 6A 6B 3A 3B 4A 4B
E2 E2
1A 1B
SHIFT
CNTL/STB
13A 13B
XERESET
2A
XHTDLAMP
2B
R075-R082
10Kx8
+5V
R082
R075
IC176
TMP82C79M
CK RST CS A0 RD WR SHF CT/S RL0 RL1 RL2 RL3 RL4 RL5 RL6 RL7
IRQ BD SL0 SL1 SL2 SL3 OB0 OB1 OB2 OB3 OA0 OA1 OA2 OA3 DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
PROG KEYBD
INTERFACE
A0110
D00 D01 D02 D03 D04 D05 D06 D07
IC176
20PIN : E2
40PIN : +5V
[030D] ADDRESS-IO BUS
[020D] CLK2M
[041B] RESET
[033B] XI79SL
[023D] XIORD
[023B] XIOWR
[012D] DATA-BUS
[040D] XERESET
[043D] XHTDLAMP

12. CIRCUIT DIAGRAM



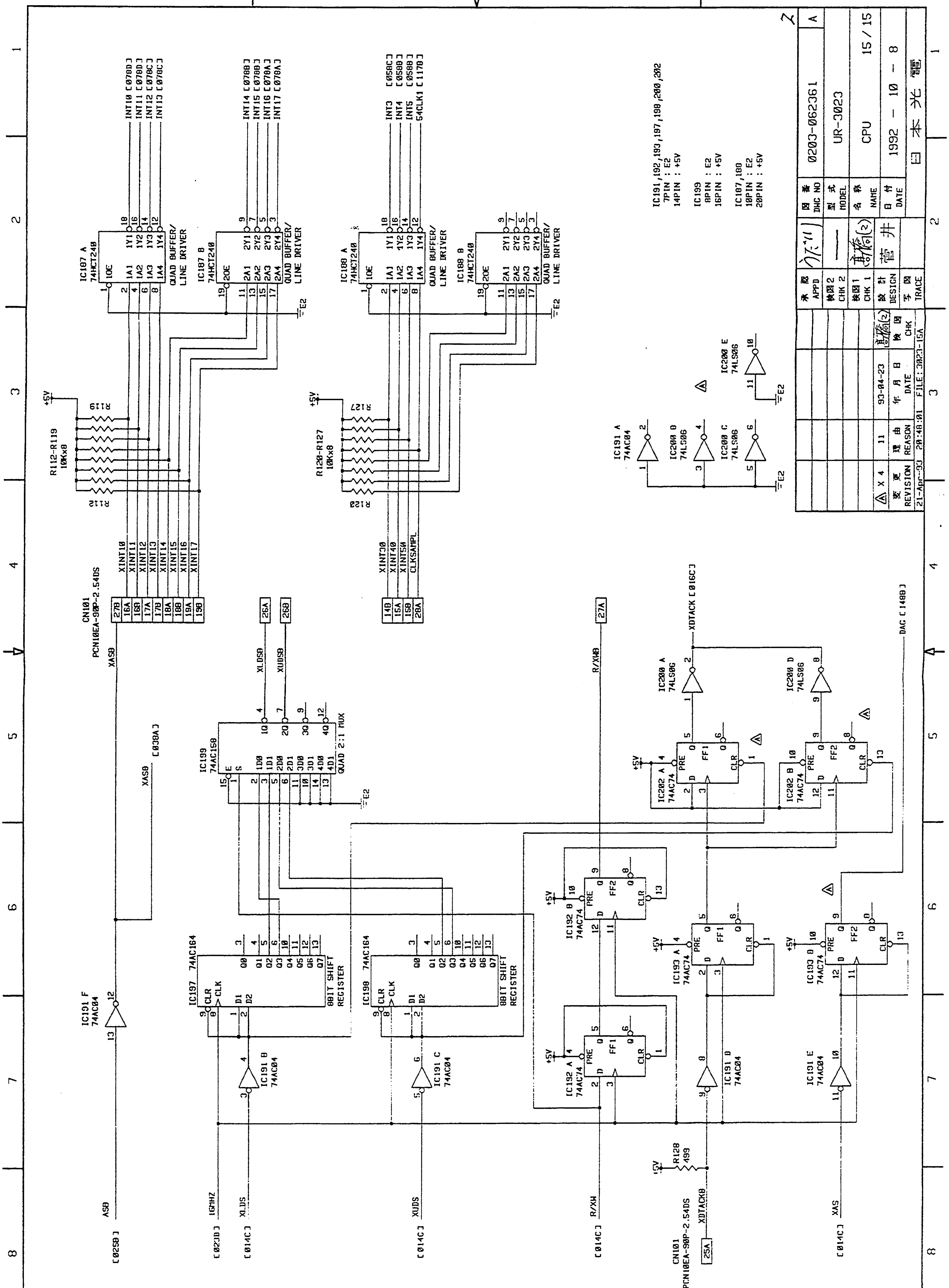
0203-062343
UR-3023
CPU
13 / 15
1992 - 10 - 8
日 本 光 電
図 番 DWG NO
型 式 MODEL
名 称 NAME
日 付 DATE
承 認 APPD
検図2 CHK 2
検図1 CHK 1
設 計 DESIGN
写 図 TRACE
変 更 REVISION
理 由 REASON
年 月 日 DATE
検 図 CHK
5-Nov-92 11:21:50 FILE:3023-13
IC181
74HC534
D TRANSP LATCHES
OE
CLK
1D 2D 3D 4D 5D 6D 7D 8D
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
LED102
LED103
LED104
LED105
LED106
LED107
LED108
LED109
LT1L51A
R104-R111
1K×8
R104
R111
+5V
E2
D00
D01
D02
D03
D04
D05
D06
D07
IC179 A
74HCT240
IC179 B
74HCT240
IC180 A
74HCT240
IC180 B
74HCT240
QUAD BUFFER/ LINE DRIVER
1OE
2OE
1A1 1A2 1A3 1A4
1Y1 1Y2 1Y3 1Y4
2A1 2A2 2A3 2A4
2Y1 2Y2 2Y3 2Y4
HTDSTOP [048D]
R088-R095
10K×8
R088
R095
R096-R103
10K×8
R096
R103
SW102
CHS-04
SW103
CHS-04
SW104
CHS-04
IC179,180,181
10PIN : E2
20PIN : +5V
IC177
7PIN : E2
14PIN : +5V
XHTDSTB [048C]
IC178 A
17903
IC178 B
17903
R084
12.4K
R083
12K
R087
15K
R085
15K
R086
19.6K
D107
1SS-307
D108
1SS-307
IC177 A
74AC32
IC177 B
74AC32
IC177 C
74AC32
IC177 D
74AC32
DATA-BUS [017C]
[043D] ERESET
[043C] HIDERR
[148A] CEXT
[106D] VD
XST/HTDS [033B]
XIORD [023B]
XDS/LEDS [033B]
XIOWR [023B]
A
B
C
D
1
2
3
4
5
6
7
8

12. CIRCUIT DIAGRAM

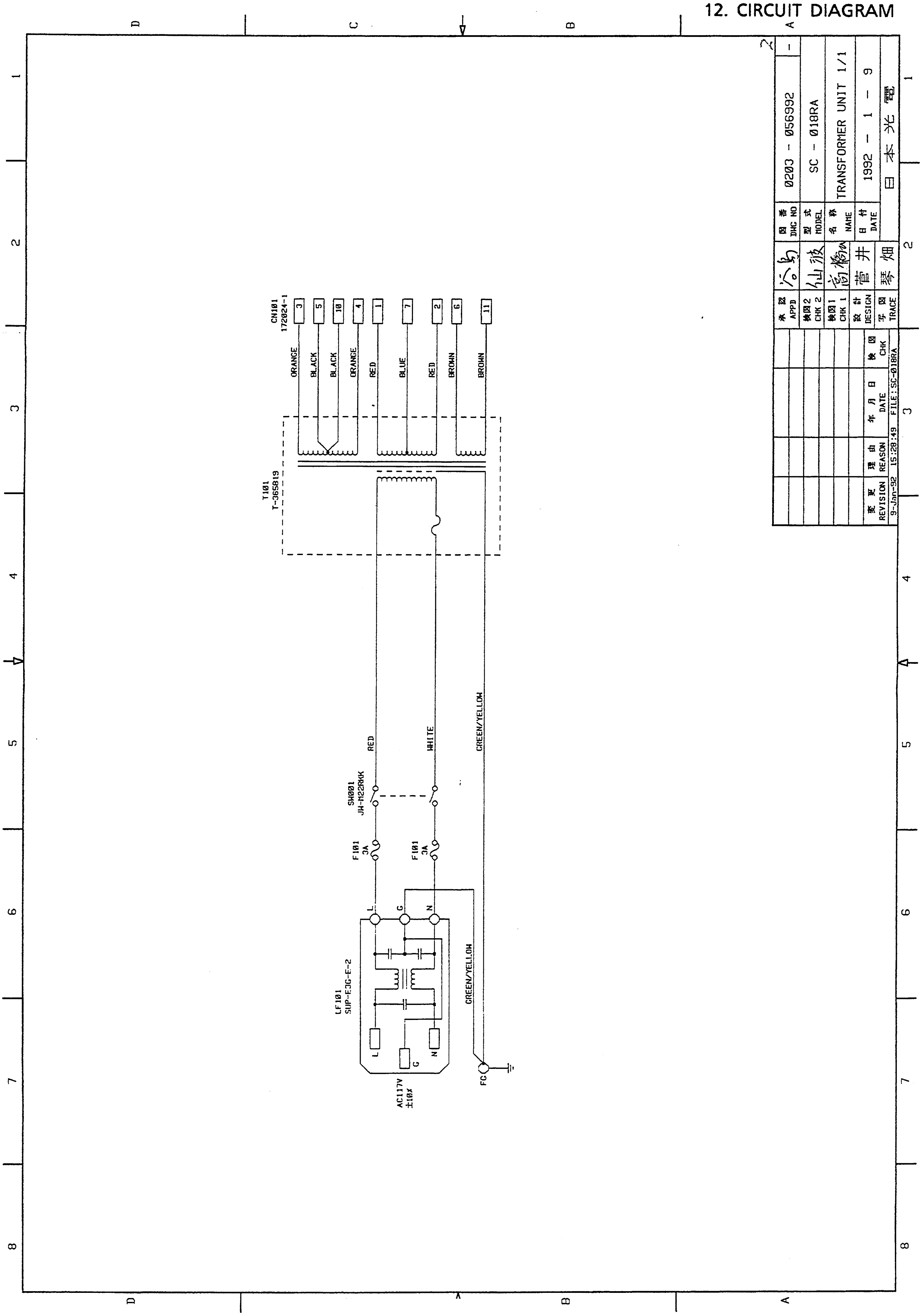


0203-062352
UR-3023
CPU
14 / 15
1992 - 10 - 8
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
5-Nov-92
11:24:56
FILE: 3023-14
CN101
PCN10EA-90P-2.54DS
XDATA00
XDATA01
XDATA02
XDATA03
XDATA04
XDATA05
XDATA06
XDATA07
XDATA08
XDATA09
XDATA10
XDATA11
XDATA12
XDATA13
XDATA14
XDATA15
XEBUS [033A]
R/XW [014C]
IC105
74BC640
IC106
74BC640
OCTAL BIDIR(3S)
BUS TRANSCVRS
D00
D01
D02
D03
D04
D05
D06
D07
D08
D09
D10
D11
D12
D13
D14
D15
C122
C123
C124
10uF/20V
C125-C131, C133-C141
0.1uF x 16
TP15
TP16
TP17
TP18
TP19
+5V
E2
IC102-IC106
10PIN : E2
20PIN : +5V
IC203
7PIN : E2
14PIN : +3V
IC203 D
IC203 E
IC203 F
74HC14
IC102
74BC533
IC103
74BC533
IC104
74BC533
D TRANSP
LATCHES
XADDR01
XADDR02
XADDR03
XADDR04
XADDR05
XADDR06
XADDR07
XADDR08
XADDR09
XADDR10
XADDR11
XADDR12
XADDR13
XADDR14
XADDR15
XADDR16
XADDR17
XADDR18
XADDR19
XADDR20
XADDR21
XADDR22
XADDR23
A01
A02
A03
A04
A05
A06
A07
A08
A09
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
CLK16M
XIORST
FIL104
NFM52R
GND
IC120 B
74F14
IC203 B
74HC14
CLK16MC
C110-C119
0.1uF x 10
C109
10uF/20V
VMM
D104
1PS082
R129
150
CENT
XPDOWN
DATA-BUS
ADDRESS-BUS
[017C]
[012C]
[154A] DAC
[023D] 16MHZ
[041B] RESET
[138C] CEXT
[046B] XPDOWN

12. CIRCUIT DIAGRAM

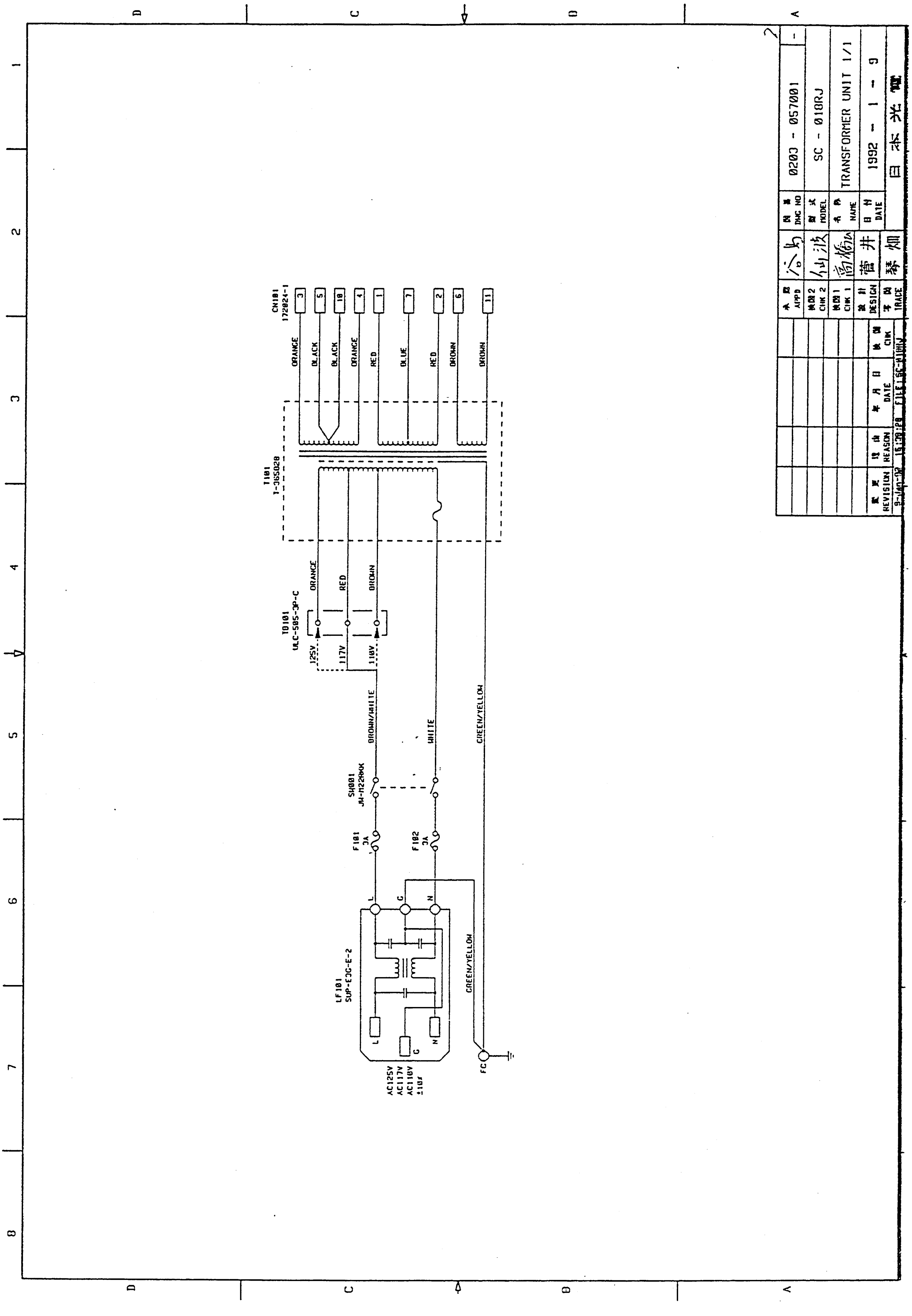

0203-062361
UR-3023
CPU
15 / 15
1992 - 10 - 8
日本光電
図番 DWG NO
型式 MODEL
名称 NAME
日付 DATE
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
検図 CHK
変更 REVISION
理由 REASON
年月日 DATE
X 4
11
93-04-23
21-Apr-93 20:48:01 FILE:3023-15A
IC191,192,193,197,198,200,202 7PIN : E2 14PIN : +5V
IC199 8PIN : E2 16PIN : +5V
IC187,188 10PIN : E2 20PIN : +5V
IC187 A 74HCT240 QUAD BUFFER/ LINE DRIVER
IC187 B 74HCT240 QUAD BUFFER/ LINE DRIVER
IC188 A 74HCT240 QUAD BUFFER/ LINE DRIVER
IC188 B 74HCT240 QUAD BUFFER/ LINE DRIVER
INT10 [070D]
INT11 [070D]
INT12 [070C]
INT13 [070C]
INT14 [070B]
INT15 [070B]
INT16 [070A]
INT17 [070A]
INT3 [058C]
INT4 [058B]
INT5 [058B]
54CLK1 [117B]
R112-R119 10Kx8
R120-R127 10Kx8
CN101 PCN10EA-90P-2.54DS
XINT10
XINT11
XINT12
XINT13
XINT14
XINT15
XINT16
XINT17
XINT30
XINT40
XINT50
CLKSAMPL
IC199 74AC158 QUAD 2:1 MUX
XLDS0
XUDS0
R/XW0
XDTACK [016C]
DAC [148B]
IC200 A 74LS06
IC200 D 74LS06
IC202 A 74AC74
IC202 B 74AC74
IC192 A 74AC74
IC192 B 74AC74
IC193 A 74AC74
IC193 B 74AC74
IC197 74AC164 8BIT SHIFT REGISTER
IC198 74AC164 8BIT SHIFT REGISTER
IC191 A 74AC04
IC191 B 74AC04
IC191 C 74AC04
IC191 D 74AC04
IC191 E 74AC04
IC191 F 74AC04
IC200 B 74LS06
IC200 C 74LS06
IC200 E 74LS06
XAS0 [030A]
AS0 [025B]
16MHZ [023D]
XLDS [014C]
XUDS [014C]
R/XW [014C]
XAS [014C]
R128 499
XDTACK0
+5V
E2

12. CIRCUIT DIAGRAM

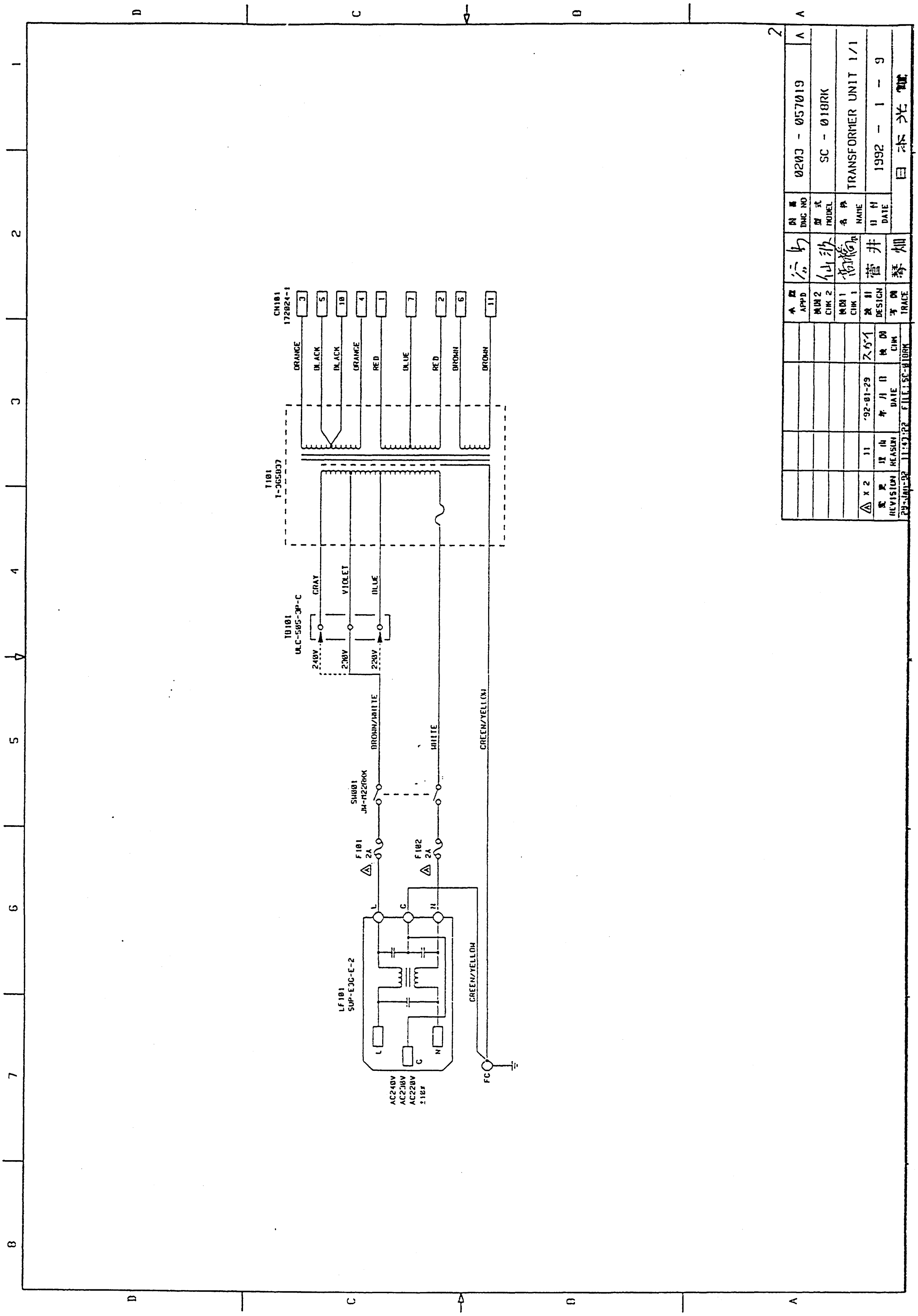

CN101
172024-1
3
5
10
4
1
7
2
6
11
ORANGE
BLACK
BLACK
ORANGE
RED
BLUE
RED
BROWN
BROWN
T101
T-365819
RED
WHITE
GREEN/YELLOW
SW001
JH-M22RKK
F101
3A
F101
3A
L
G
N
LF101
SUP-E3G-E-2
GREEN/YELLOW
FG
AC117V
±10%
0203 - 056992
SC - 018RA
TRANSFORMER UNIT 1/1
1992 - 1 - 9
日本光電
図番 DHC NO
型式 MODEL
名称 NAME
日付 DATE
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
仙波
高橋
菅井
琴畑
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
9-Jan-92 15:28:49 FILE:SC-018RA
A
B
C
D
1
2
3
4
5
6
7
8

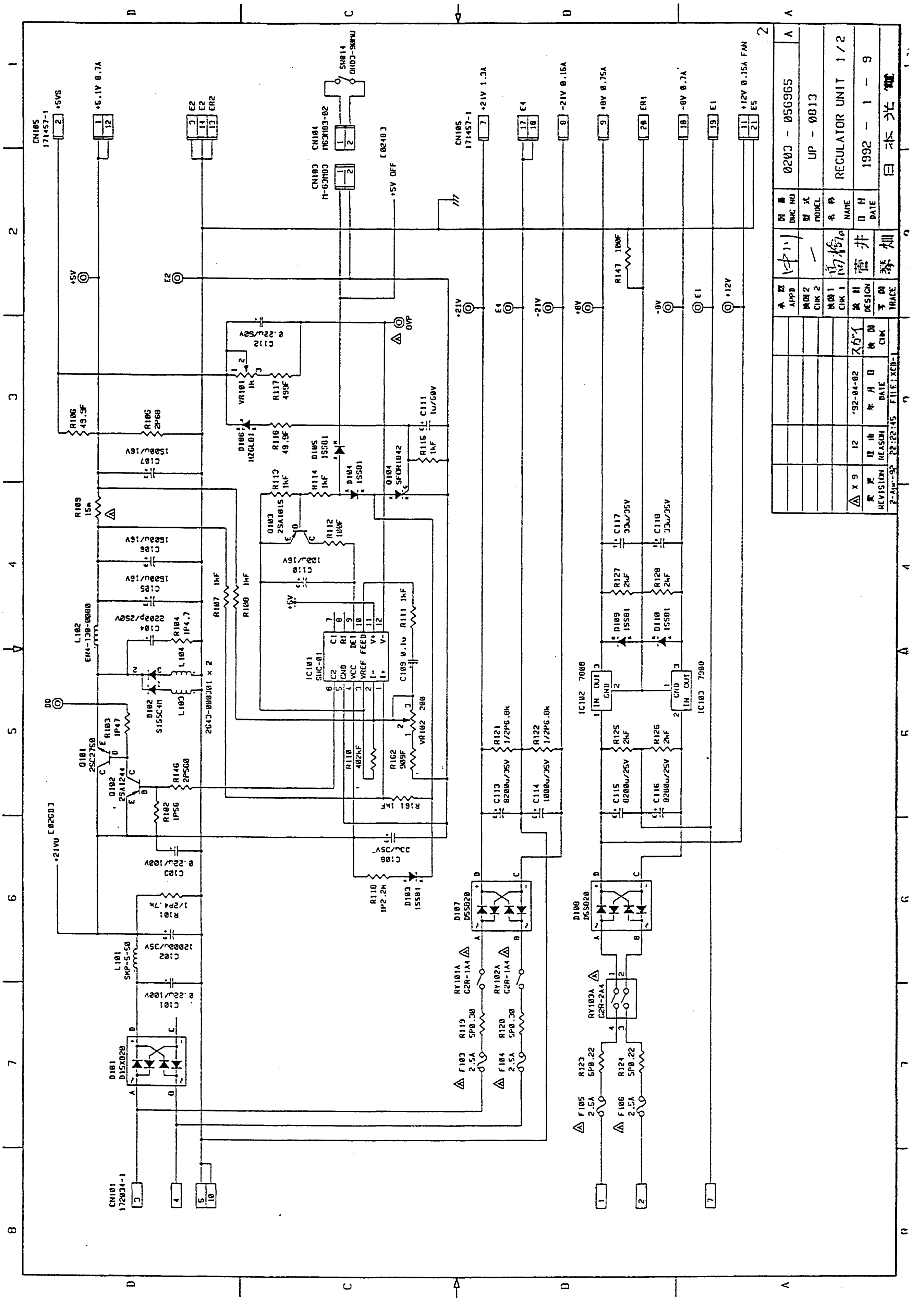
12. CIRCUIT DIAGRAM

NO CONTENTS

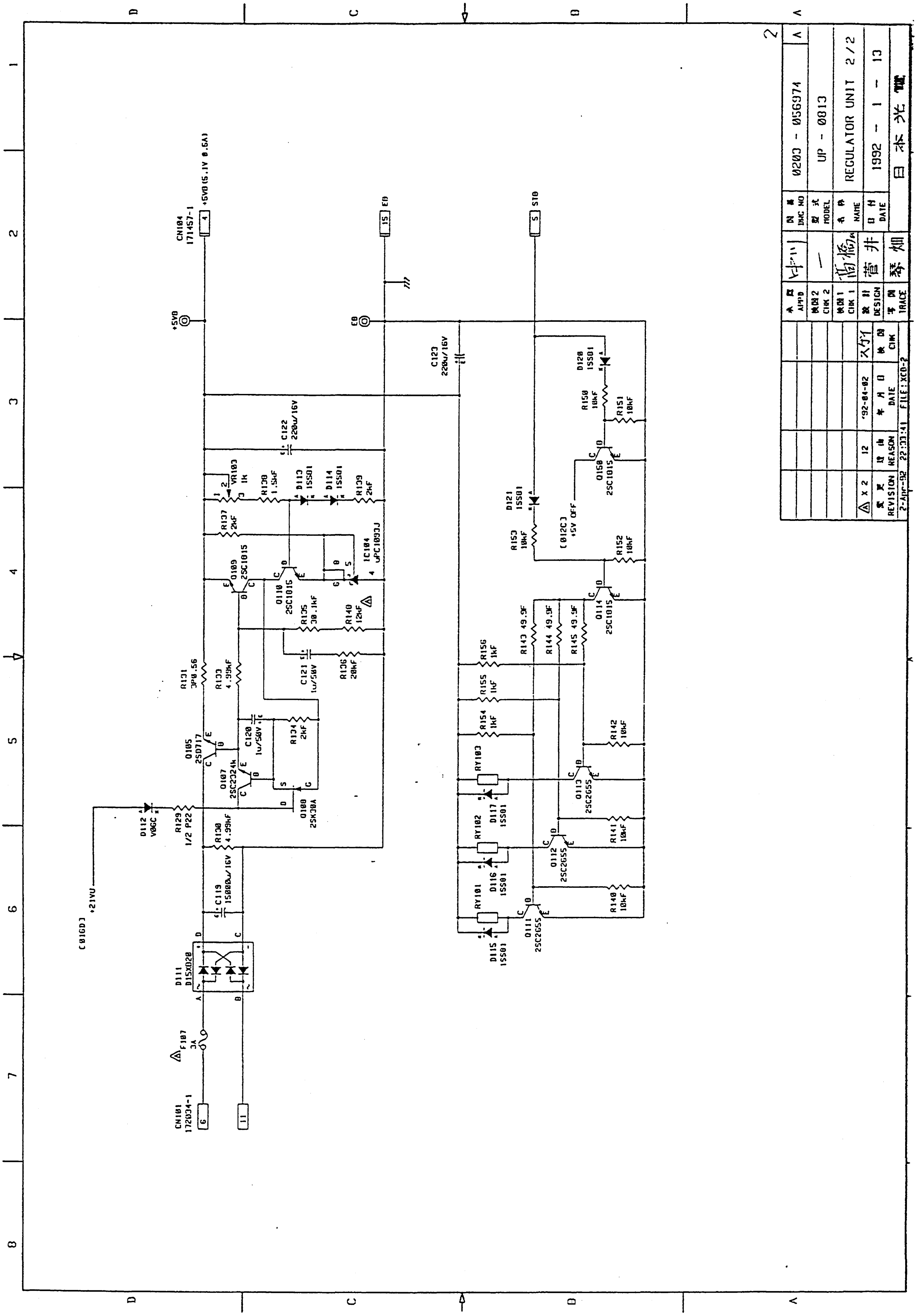

CN101
172024-1
3
5
10
4
1
7
2
6
11
ORANGE
BLACK
BLACK
ORANGE
RED
BLUE
RED
BROWN
BROWN
T101
T-365028
ORANGE
RED
BROWN
TB101
VLC-505-3P-C
125V
117V
110V
BROWN/WHITE
WHITE
GREEN/YELLOW
SW001
JW-M22RKK
F101
3A
F102
3A
L
G
N
LF101
SUP-E3G-E-2
GREEN/YELLOW
AC125V
AC117V
AC110V
±10%
FG
0203 - 057001
SC - 010RJ
TRANSFORMER UNIT 1/1
1992 - 1 - 9
日本光電
図番 DWG NO
型式 MODEL
名称 NAME
日付 DATE
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
手図 TRACE
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
9-Jan-92 15:39:28 FILE:SC-010RJ
A
B
C
D
1
2
3
4
5
6
7
8

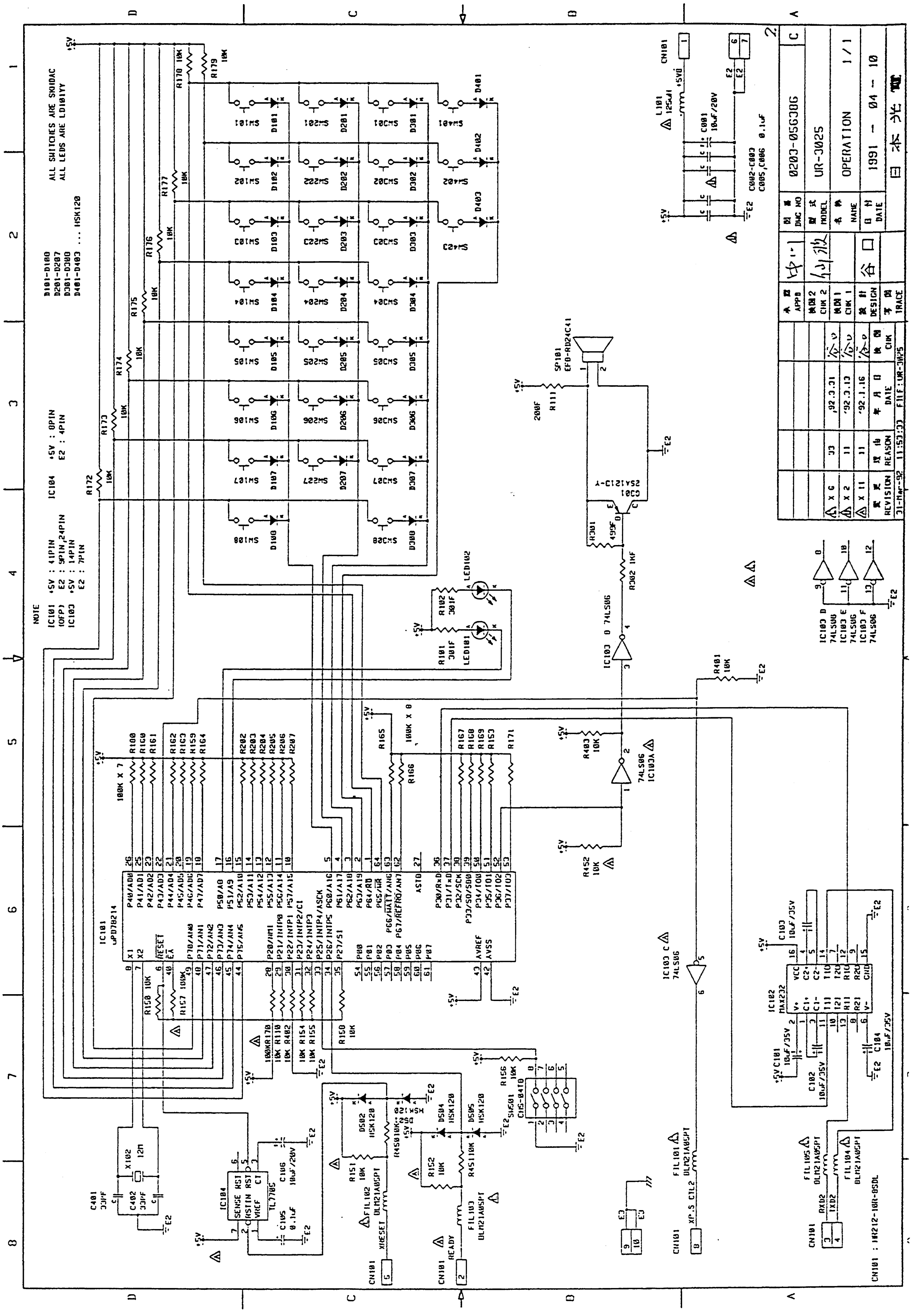
12. CIRCUIT DIAGRAM


CN101
172024-1
3
5
10
4
1
7
2
6
11
ORANGE
BLACK
BLACK
ORANGE
RED
BLUE
RED
BROWN
BROWN
T101
T-365037
TU101
ULC-505-3P-C
GRAY
VIOLET
BLUE
240V
230V
220V
BROWN/WHITE
WHITE
GREEN/YELLOW
SW801
JH-M22RKK
F101
2A
F102
2A
L
G
N
LF101
SUP-E3G-E-2
GREEN/YELLOW
FG
AC240V
AC230V
AC220V
±10%
0203 - 057019
SC - 018RK
TRANSFORMER UNIT 1/1
1992 - 1 - 9
DWG NO
MODEL
NAME
DATE
APP'D
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
'92-01-29
29-JAN-92 11:47:22 FILE:SC-018RK

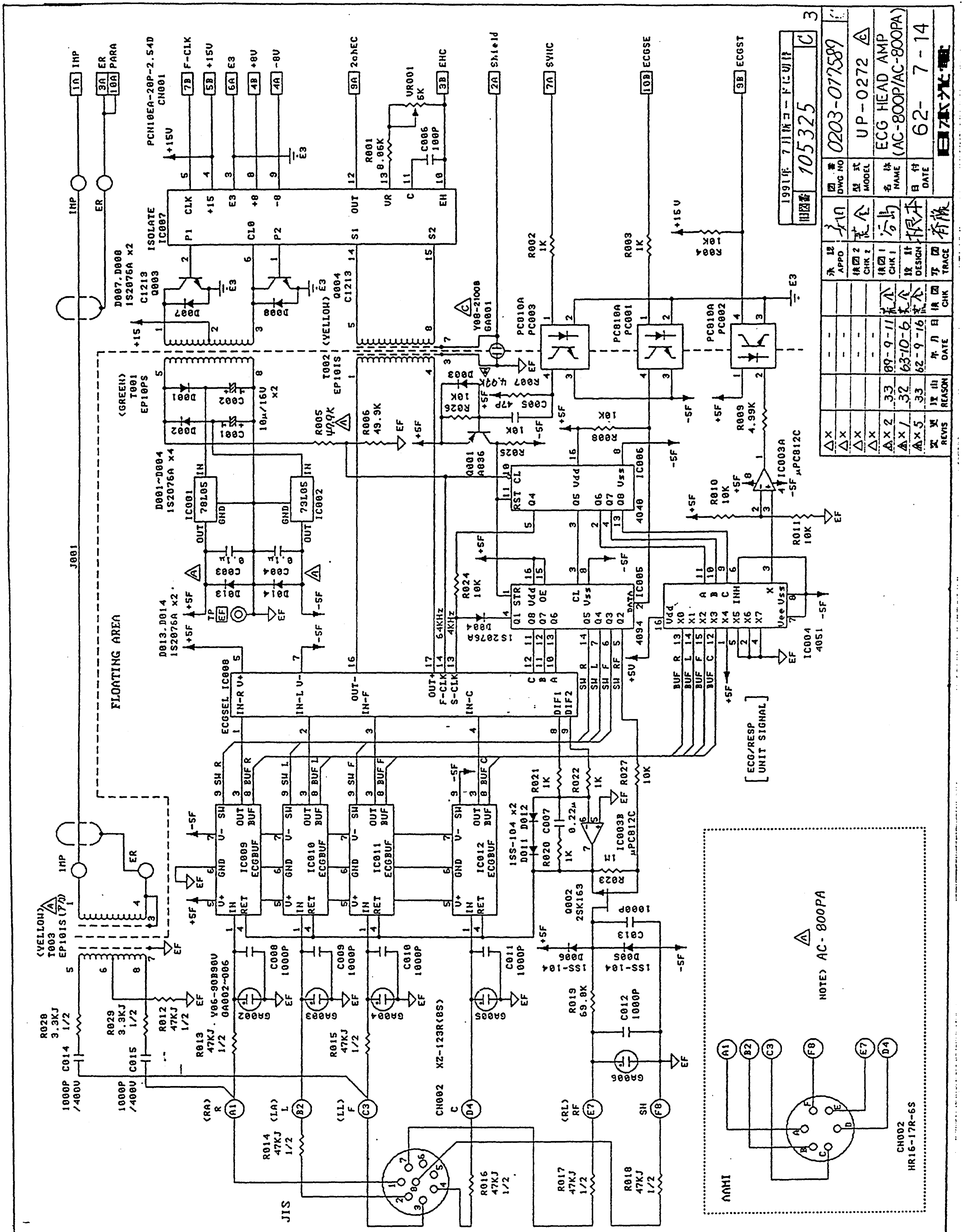

0203 - 056965
UP - 0813
REGULATOR UNIT 1/2
1992 - 1 - 9
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
'92-04-02
12
FILE:XCD-1
CN105 171457-1
CN101 172034-1
CN103 M-63M03
CN104 M63M03-02
SW014
+5V OFF
+5VS
+6.1V 0.7A
E2
ER2
+21V 1.3A
E4
-21V 0.16A
+8V 0.75A
ER1
-8V 0.7A
E1
+12V 0.15A FAN
ES
+21VU
IC101 SHC-01
IC102 7808
IC103 7908
D101 D15XB20
D107 D5SB20
D108 D5SB20
Q101 2SC2750
Q102 2SA1244
Q103 2SA1015
Q104 SFOR1042
D102 S15SC4M
D103 1SS81
D104 1SS81
D105 1SS81
D106 HZ6L01
D109 1SS81
D110 1SS81
L101 SKP-5-50
L102 EN4-130-0000
L103
L104
VR101 1K
VR102 200
RY101A C2R-1A4
RY102A C2R-1A4
RY103A C2R-2A4
F103 2.5A
F104 2.5A
F105 2.5A
F106 2.5A
R119 5P0.30
R120 5P0.30
R123 5P0.22
R124 5P0.22
R147 100F
C101 0.22u/100V
C102 12000u/35V
C103 0.22u/100V
C104 2200p/250V
C105 1500u/16V
C106 1500u/16V
C107 1500u/16V
C110 100u/16V
C111 1u/50V
C112 0.22u/50V
C113 8200u/35V
C114 1000u/35V
C115 8200u/25V
C116 8200u/25V
C117 33u/35V
C118 33u/35V
OVP
DD
+5V
+21V
-21V
+8V
-8V
+12V

12. CIRCUIT DIAGRAM

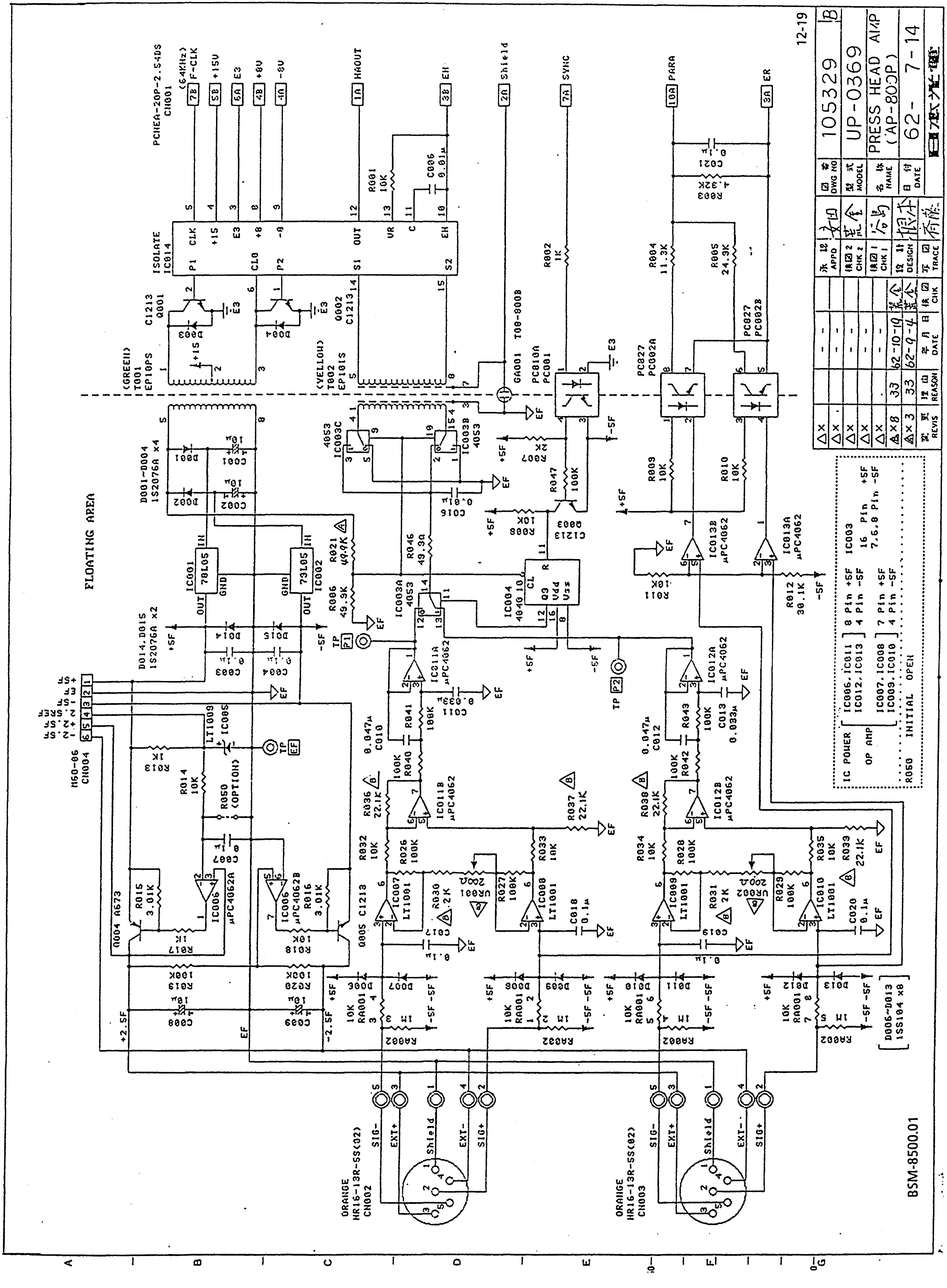

0203 - 056974
UP - 0813
REGULATOR UNIT 2/2
1992 - 1 - 13
DWG NO
MODEL
NAME
DATE
APP'D
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
'92-04-02
FILE:XC0-2
CN104
171457-1
+5V0(5.1V 0.6A)
+5V0
CN101
172034-1
F107
3A
D111
D15XB20
C119
15000u/16V
R130
4.99kF
R129
1/2 P22
D112
V06C
+21VU
Q105
2SD717
Q107
2SC2324K
Q108
2SK30A
C120
1u/50V
R134
2kF
R131
RPG.56
R133
4.99kF
Q109
2SC1015
Q110
2SC1015
R135
30.1kF
C121
1u/50V
R136
20kF
R140
12kF
IC104
uPC1093J
R137
2kF
VR103
1K
R138
1.5kF
D113
1SS01
D114
1SS01
R139
2kF
C122
220u/16V
E0
C123
220u/16V
ST0
D120
1SS01
R150
10kF
R151
10kF
Q150
2SC1015
D121
1SS01
(012C)
+5V OFF
R153
10kF
R152
10kF
Q114
2SC1015
R143 49.9F
R144 49.9F
R145 49.9F
R156
1kF
R155
1kF
R154
1kF
RY103
RY102
RY101
D117
1SS01
D116
1SS01
D115
1SS01
Q113
2SC2655
Q112
2SC2655
Q111
2SC2655
R142
10kF
R141
10kF
R140
10kF


ALL SWITCHES ARE SKHDAC
ALL LEDS ARE LD101YY
D101-D108
D201-D207
D301-D308
D401-D403 ... 1SK120
IC104 +5V : 8PIN
E2 : 4PIN
NOTE
IC101 (QFP) +5V : 41PIN
E2 : 9PIN,24PIN
IC103 +5V : 14PIN
E2 : 7PIN
IC101 uPD78214
IC102 MAX232
IC103 74LS06
IC104 TL7705
SP101 EFO-RD24C41
Q301 2SA1213-Y
X102 12M
CN101
0203-05G30G
UR-3025
OPERATION 1/1
1991 - 04 - 10
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
'92.3.31
'92.3.13
'92.1.16
CN101 : IMR212-10R-0SDL

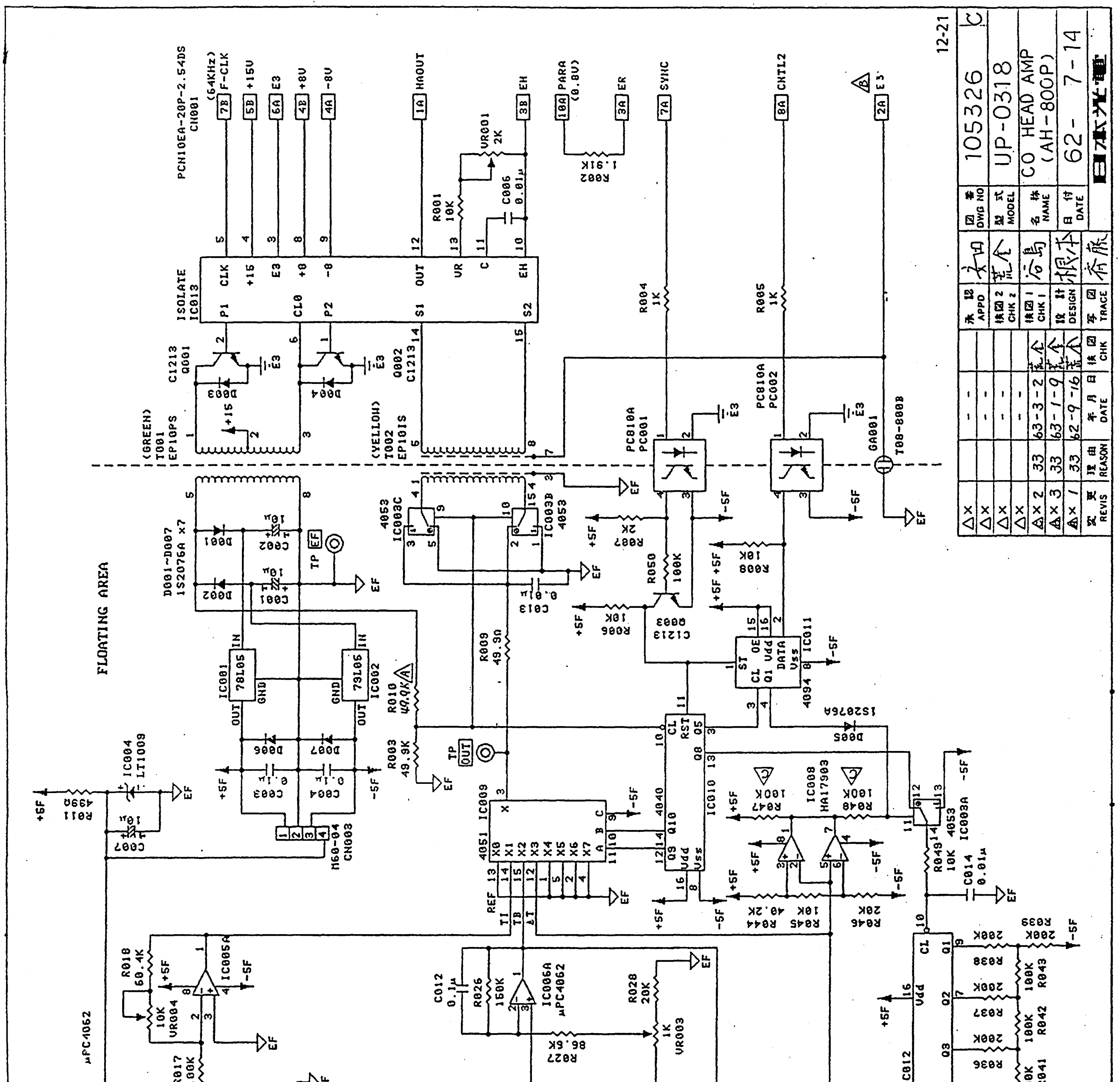
12. CIRCUIT DIAGRAM

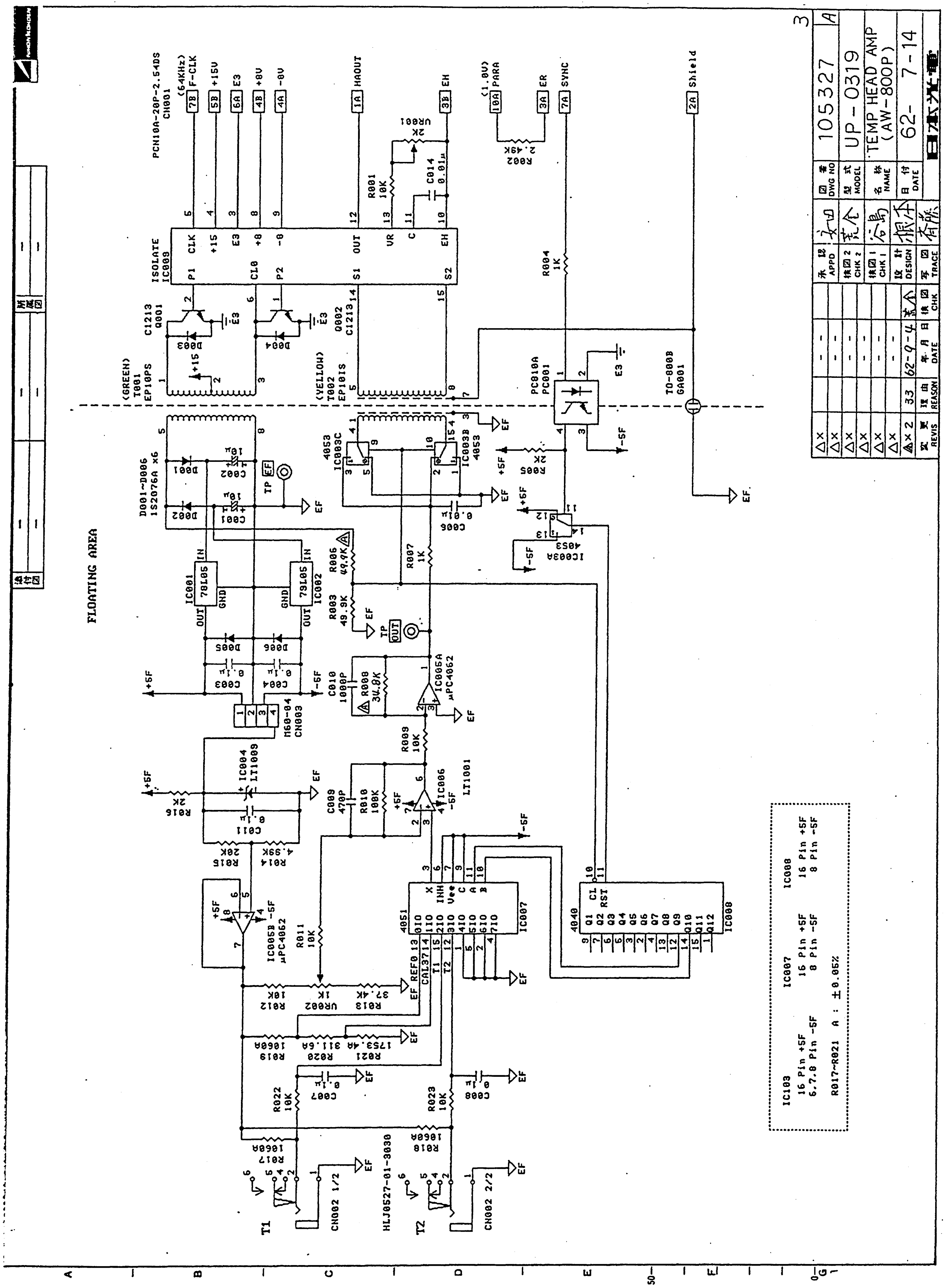


0203-077589
UP-0272
ECG HEAD AMP
(AC-800P/AC-800PA)
62- 7-14
105325
FLOATING AREA
ISOLATE IC007
ECGSEL IC008
IC009 ECGBUF
IC010 ECGBUF
IC011 ECGBUF
IC012 ECGBUF
IC001 78L05
IC002 73L05
IC004 4051
IC005 4094
IC006 4040
IC003A μPC812C
IC003B μPC812C
PC001 PC810A
PC002 PC810A
PC003 PC810A
T001 EP10PS
T002 EP101S
T003 EP101S
CN001 PCN10EA-20P-2.54D
CN002 HR16-17R-6S
IMP
ER
J001
JIS
AAMI
ECG/RESP UNIT SIGNAL
NOTE) AC-800PA
1A IMP
3A ER
10A PARA
7B F-CLK
5B +15V
6A E3
4B +8V
4A -8V
9A 2chEC
3B EHC
2A Shield
7A SYNC
10B ECGSE
9B ECGST

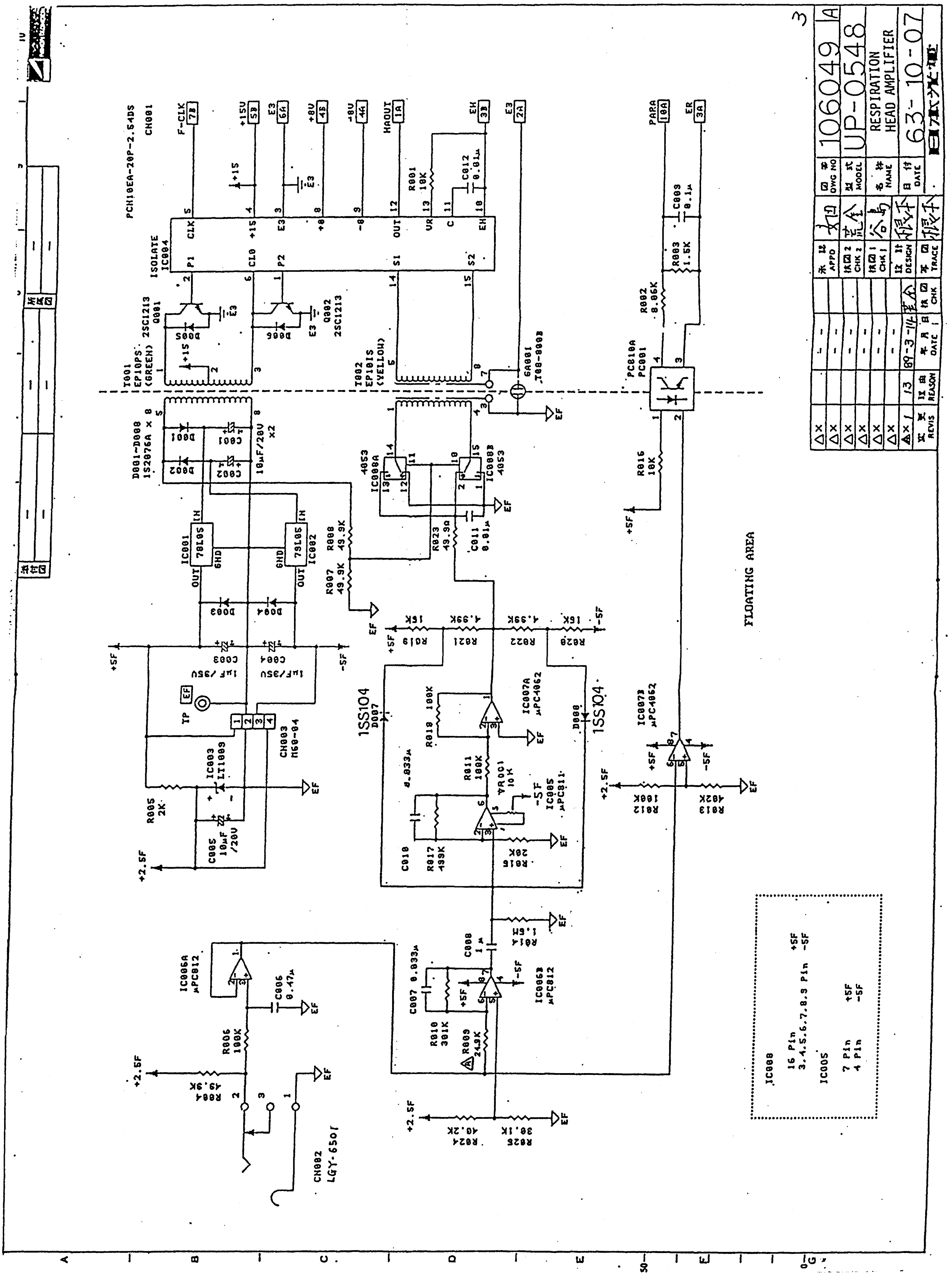

12-19
105329 B
UP-0369
PRESS HEAD AMP
(AP-800P)
62- 7-14
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVIS
REASON
DATE
CHK
62-10-19
62-9-4
FLOATING AREA
PCHEA-20P-2.54DS
CN001
(64KHz) 7B F-CLK
5B +15V
6A E3
4B +8V
4A -8V
1A HAOUT
3B EH
2A Shield
7A SYNC
10A PARA
3A ER
ISOLATE IC014
IC001 78L05
IC002 79L05
IC003A 4053
IC003B 4053
IC003C 4053
IC004 4040
IC006 μPC4062A
IC006 μPC4062B
IC007 LT1001
IC008 LT1001
IC009 LT1001
IC010 LT1001
IC011A μPC4062
IC011B μPC4062
IC012A μPC4062
IC012B μPC4062
IC013A μPC4062
IC013B μPC4062
PC810A PC001
PC827 PC002A
PC827 PC002B
T001 EP10PS (GREEN)
T002 EP101S (YELLOW)
GA001 T00-800B
D001~D004 1S2076A x4
D014,D015 1S2076A x2
D006~D013 1SS104 x8
M60-06 CN004
ORANGE HR16-13R-5S(02) CN002
ORANGE HR16-13R-5S(02) CN003
SIG-
EXT+
Shield
EXT-
SIG+
TP P1
TP P2
TP EF
R050 (OPTION)
IC POWER
IC006.IC011 IC012.IC013 8 Pin +5F 4 Pin -5F
IC007.IC008 IC009.IC010 7 Pin +5F 4 Pin -5F
IC003 16 Pin +5F 7.6.8 Pin -5F
OP AMP
R050 INITIAL OPEN
A
B
C
D
E
F
G

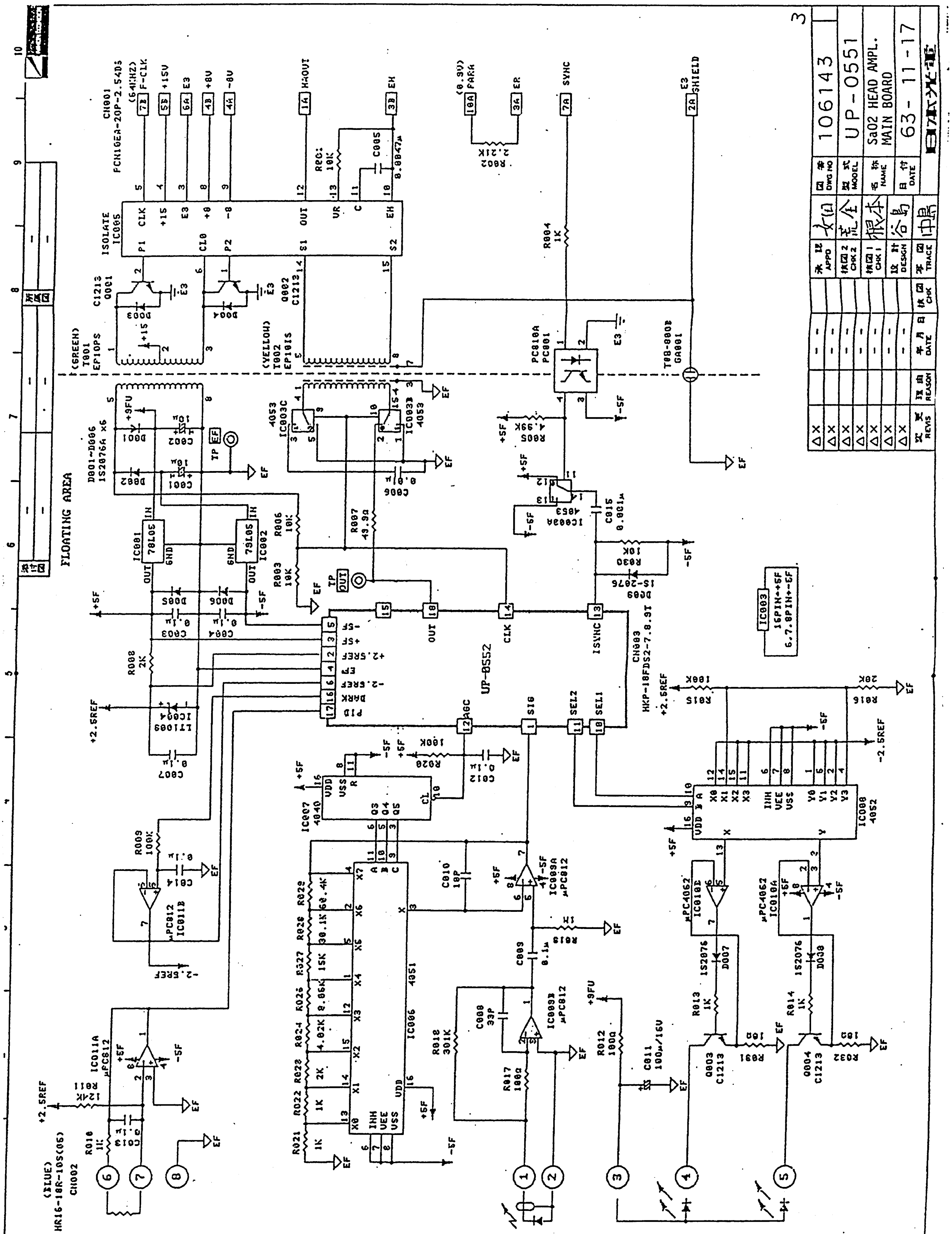
12. CIRCUIT DIAGRAM


12-21
105326 C
DWG NO
UP-0318
MODEL
CO HEAD AMP
(AH-800P)
NAME
62- 7-14
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVIS
REASON
DATE
CHK
63-3-2
63-1-9
62-9-16
BSM-8500.02
FLOATING AREA
PCH10EA-20P-2.54DS
CN001
(64KHz) F-CLK
+15V
E3
+8V
-8V
HAOUT
EH
PARA (0.8V)
ER
SVHC
CNTL2
E3
ISOLATE
IC013
CLK
OUT
VR
R001 10K
VR001 2K
C006 0.01μ
R002 1.91K
R004 1K
R005 1K
PC810A PC001
PC810A PC002
GA001
T08-080B
(GREEN) T001 EP10PS
(YELLOW) T002 EP101S
C1213 Q001
C1213 Q002
D003
D004
D001-D007 1S2076A x7
D001
D002
C001 10μ
C002 10μ
TP EF
IC001 78L05
IC002 79L05
D006
D007
C003 0.1
C004 0.1
CN003 H60-04
IC004 LT1009
R011 499Ω
C007 10μ
4053 IC003C
IC003B 4053
C013 0.01
R007 2K
R050 100K
R006 10K
R008 10K
C1213 Q003
IC011 4094
1S2076A
D005
R009 49.9Ω
R010 49.9K
R003 49.9K
TP OUT
4051 IC009
IC010 4040
IC008 HA17903
R047 100K
R048 100K
R044 40.2K
R045 10K
R046 20K
IC003A 4053
R049 10K
C014 0.01μ
R039 200K
IC005 μPC4062
R018 60.4K
VR004 10K
IC005A
IC005B
R017 100K
C008 0.01μ
R014 249K
R016 100K
R013 20K
VR002 1K
R015 100K
C009 0.1μ
R012 113K
C012 0.1μ
R026 150K
IC006A μPC4062
R028 20K
VR003 1K
R027 86.6K
C010 0.1μ
R024 39.2K
IC007 LT1001
R025 1K
C011 0.47μ
R023 100K
R021 2K
R022 100Ω
IC012 4040
R038 R037 R036 R035 R034 200K
R043 R042 R041 R040 100K
IC006B μPC4062
R031 200K
VR005 1K
R032 19.6K
R033 60.4K
(-2~+2V)
IC003, IC009 16 Pin +5F 6,8,7 Pin -5F
CN002 HR16-10R-10S(01) RED
TI (INJECTION PROBE)
TB (CATHETER)
EF
+5F
-5F
A B C D E F G

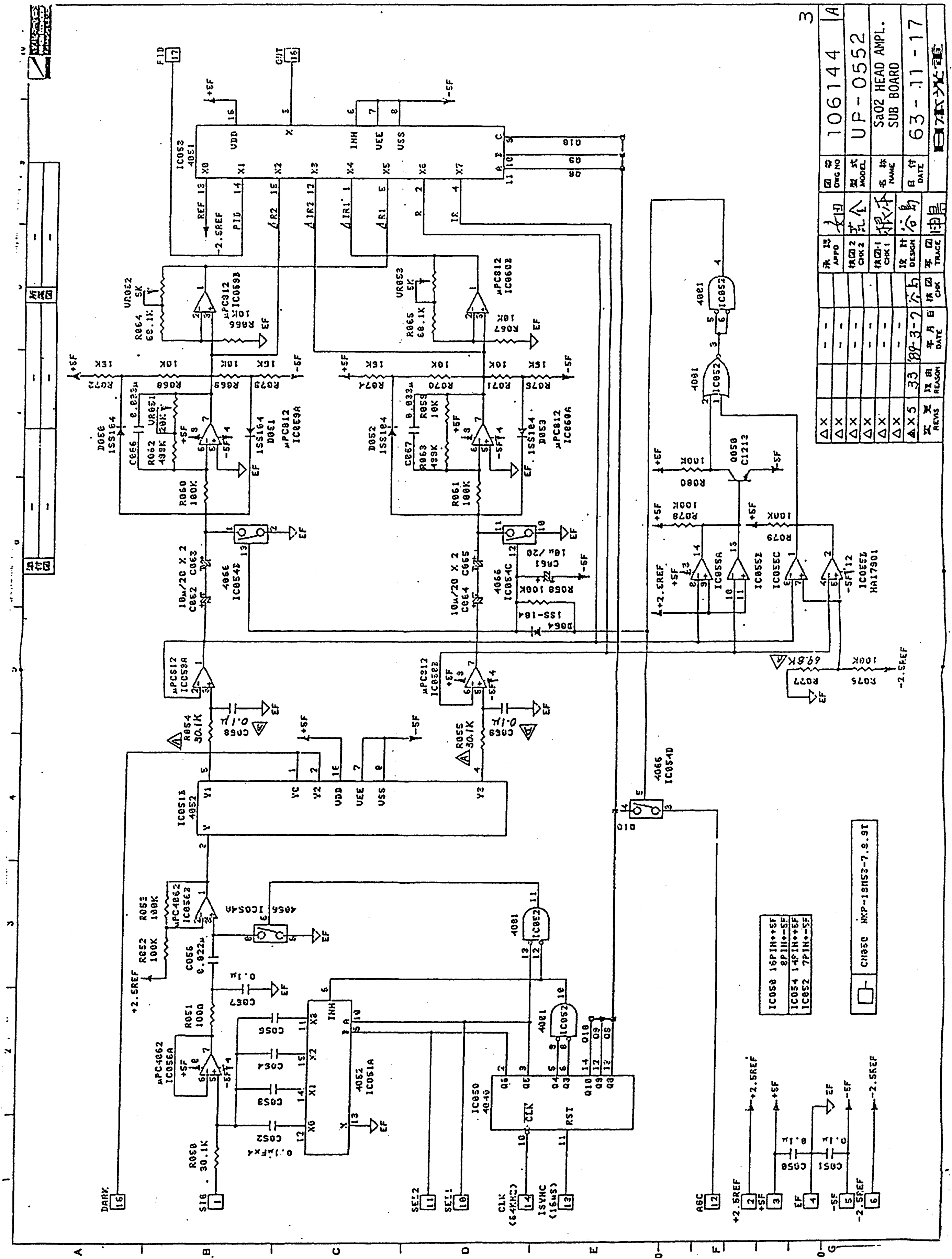

105327
UP-0319
TEMP HEAD AMP
(AW-800P)
62- 7-14
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVIS
DATE
REASON
62-9-4
33
FLOATING AREA
PCN10A-20P-2.54DS
CN001
(64KHz)
F-CLK
+15V
E3
+8V
-8V
HAOUT
EH
(1.8V)
PARA
ER
SYNC
Shield
ISOLATE
IC009
UR001 2K
R001 10K
C014 0.01μ
R002 2.49K
R004 1K
Q001 C1213
Q002 C1213
D003
D004
(GREEN) T001 EP10PS
(YELLOW) T002 EP101S
PC810A PC001
TO-800B GA001
D001~D006 1S2076A x6
TP EF
TP OUT
IC001 78L05
IC002 79L05
4053 IC003C
IC003B 4053
IC003A 4053
R005 2K
R006 49.9K
R007 1K
R003 49.9K
C006 0.01μ
C001 10μ
C002 10μ
C003 0.1μ
C004 0.1μ
M60-04 CN003
C010 1000P
R008 34.8K
IC005A μPC4062
R009 10K
IC004 LT1009
R016 2K
C011 0.1μ
R015 20K
R014 4.99K
IC005B μPC4062
C009 470P
R010 100K
IC006 LT1001
4051 IC007
4040 IC008
R011 10K
R012 10K
UR002 1K
R013 37.4K
R019 1060Ω
R020 311.6Ω
R021 1753.4Ω
R022 10K
C007 0.1μ
R023 10K
C008 0.1μ
R017 1060Ω
R018 1060Ω
T1
T2
CN002 1/2
CN002 2/2
HLJ0527-01-3030
IC103 16 Pin +5F 6,7,8 Pin -5F
IC007 16 Pin +5F 8 Pin -5F
IC008 16 Pin +5F 8 Pin -5F
R017~R021 Δ : ±0.05%
+5F
-5F
EF

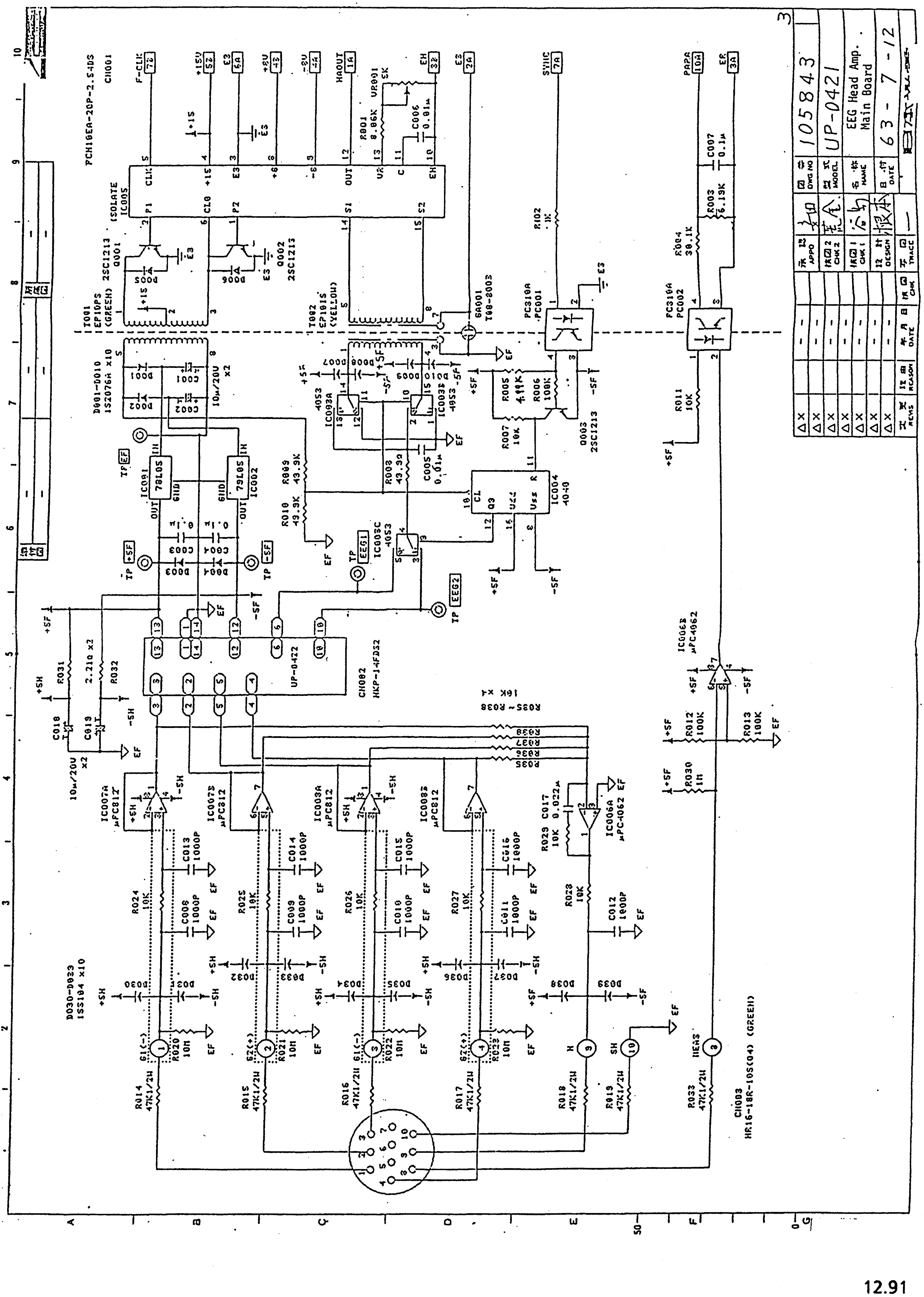
12. CIRCUIT DIAGRAM


106049 A
UP-0548
RESPIRATION HEAD AMPLIFIER
63-10-07
FLOATING AREA
ISOLATE IC004
PCN10EA-20P-2.54DS CN001
CN002 LGY-6501
CN003 N60-04
IC006A µPC812
IC006B µPC812
IC007A µPC4062
IC007B µPC4062
IC005 µPC811
IC008A 4053
IC008B 4053
IC001 78L05
IC002 79L05
IC003 LT1009
PC810A PC001
T001 EP10PS (GREEN)
T002 EP10IS (YELLOW)
Q001 2SC1213
Q002 2SC1213
1SS104
IC008 16 Pin +5F 3,4,5,6,7,8,9 Pin -5F
IC005 7 Pin +5F 4 Pin -5F

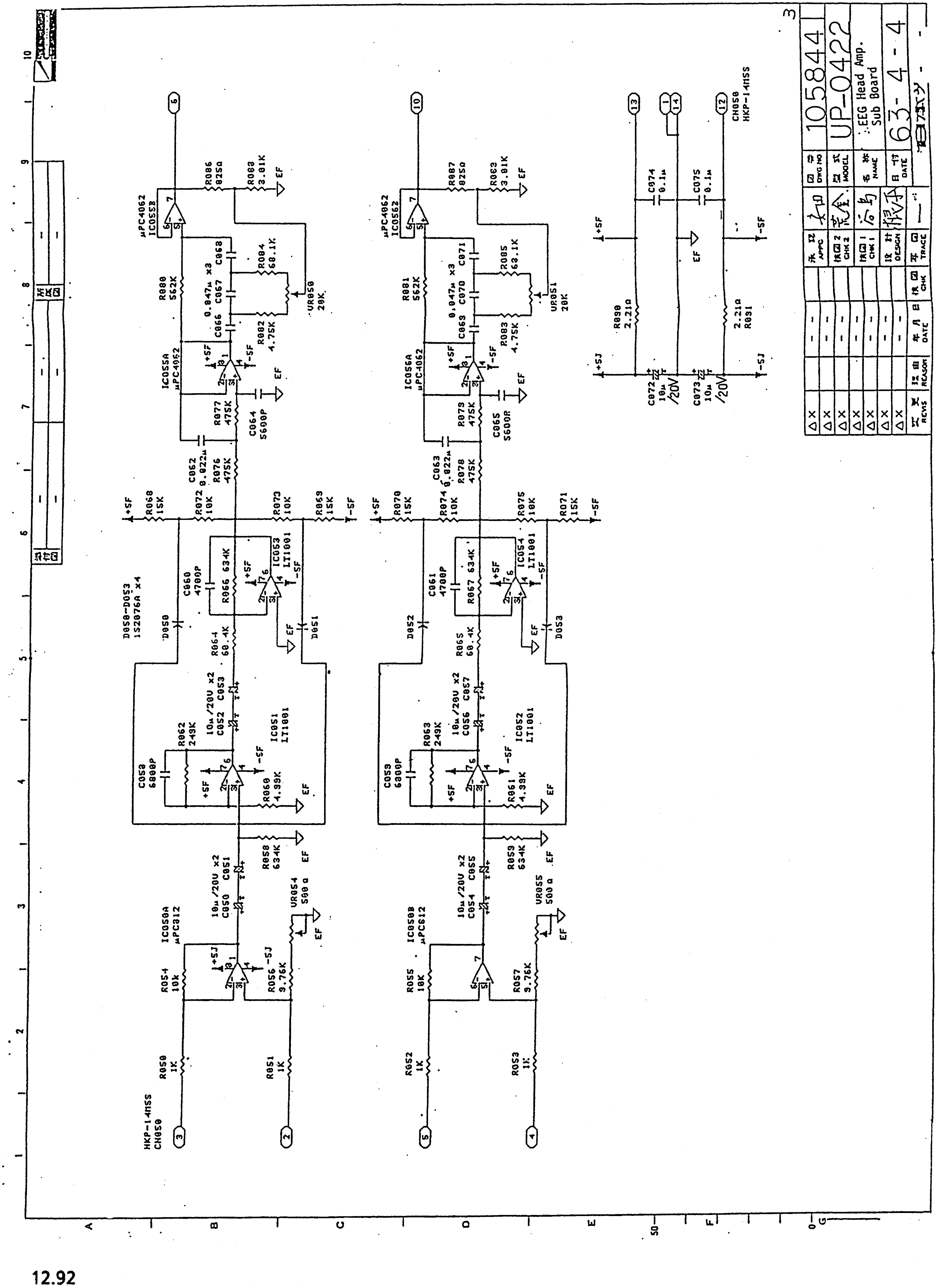

106143
UP-0551
SaO2 HEAD AMPL.
MAIN BOARD
63-11-17
FLOATING AREA
UP-0552
CN001 FCN10EA-20P-2.54DS
ISOLATE IC005
IC001 78L05
IC002 79L05
IC004 LT1009
IC006 4051
IC007 4040
IC008 4052
IC003A 4053
IC003B 4053
IC003C 4053
IC009A μPC812
IC009B μPC812
IC010A μPC4062
IC010B μPC4062
IC011A μPC812
IC011B μPC812
PC810A PC001
CN003 HKP-10FDS2-7.8.9T
CN002 HR16-10R-10S(06)
T001 EP10PS
T002 EP10IS
TBB-0003 GA001
D001~D006 1S2076A x6
Q001 C1213
Q002 C1213
Q003 C1213
Q004 C1213
F-CLK
+15V
E3
+8V
-8V
HAOUT
EH
PARK
ER
SYNC
SHIELD
OUT
CLK
ISYNC
SEL1
SEL2
SIG
AGC
PID
DARK
-2.5REF
+2.5REF
+5F
-5F
+9FU
EF
TP EF
TP OUT
IC003 16PIN→+5F 6.7.8PIN→-5F

12. CIRCUIT DIAGRAM

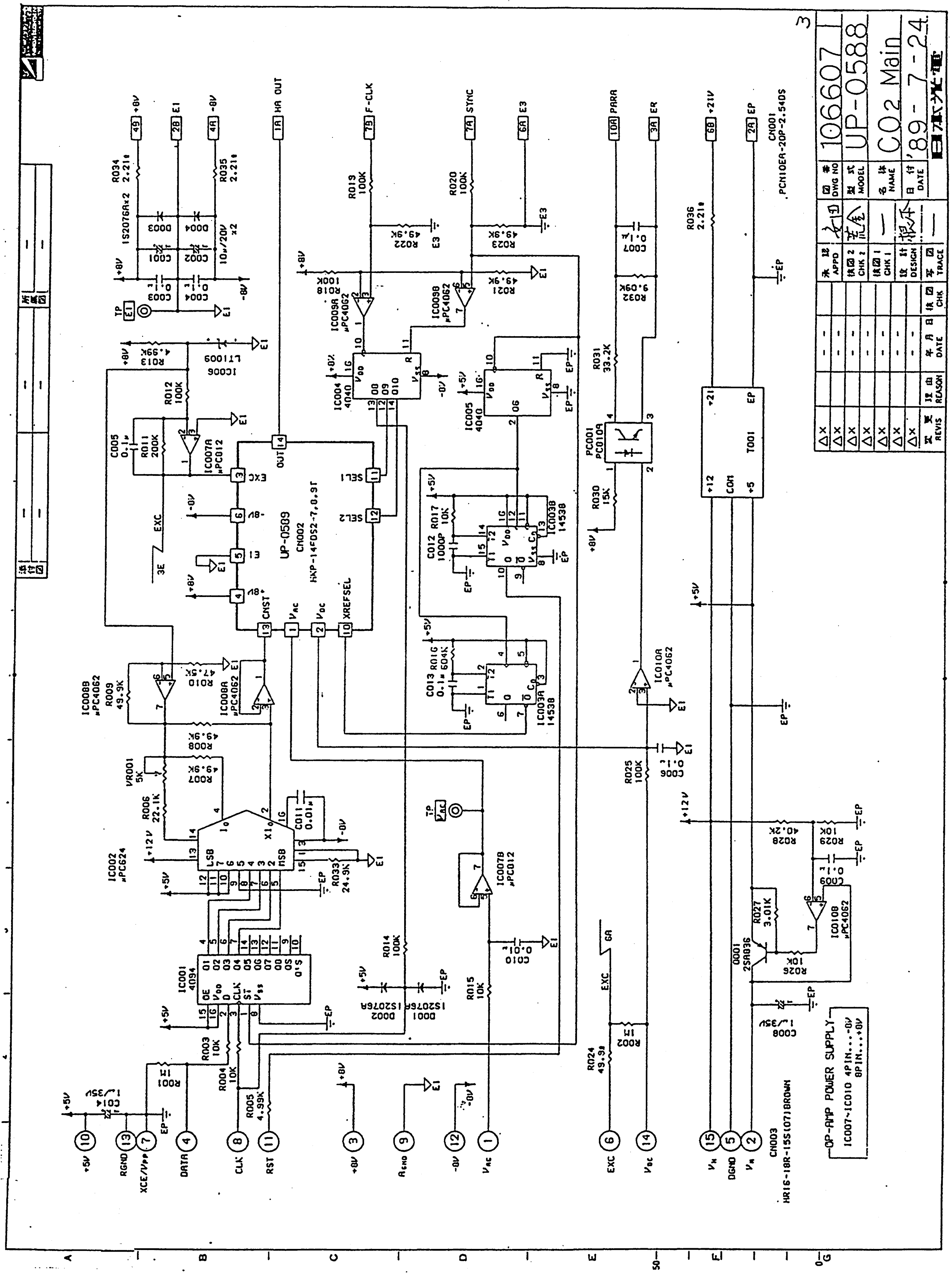

106144
UP-0552
Sa02 HEAD AMPL.
SUB BOARD
63-11-17
IC053 4051
IC051B 4052
IC051A 4052
IC050 4040
IC055A
IC055B
IC055C
IC055D
HA17901
4066 IC054A
4066 IC054B
4066 IC054C
4066 IC054D
SIG
DARK
SEL2
SEL1
CLK (64KHz)
1SYNC (16mS)
AGC
+2.5REF
+5F
EF
-5F
-2.5REF
FID
OUT
CN050 HKP-18MS3-7.8.9T


105843
UP-0421
EEG Head Amp. Main Board
63-7-12
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REASON
REVS
PCH10EA-20P-2.54DS CH001
F-CLK
+15V
E3
+8V
-8V
HAOUT
EH
E3
SYNC
PAPA
ER
ISOLATE IC005
2SC1213 Q001
2SC1213 Q002
T001 EP10PS (GREEN)
T002 EP1015 (YELLOW)
D001-D010 1S2076A x10
10μ/20V x2
IC001 78L05
IC002 79L05
TP EF
TP +5F
TP -5F
TP EEG1
TP EEG2
IC003A 4053
IC003B 4053
IC003C 4053
IC004 4040
R001 8.06K
VR001 5K
C006 0.01μ
C005 0.01μ
R008 43.9Ω
R009 43.9K
R010 43.9K
R005 4.11K
R006 100K
R007 10K
Q003 2SC1213
PC310A PC001
PC310A PC002
GA001 TGB-8003
R102 1K
R003 6.19K
R004 30.1K
C007 0.1μ
R011 10K
CH002 HKP-14FDS2
UP-0422
R031 2.21Ω x2 R032
C018 C019 10μ/20V x2
R035~R038 16K x4
IC006B μPC4062
IC006A μPC4062
R012 100K
R013 100K
R030 1M
R029 10K
C017 0.022μ
IC007A μPC812
IC007B μPC812
IC008A μPC812
IC008B μPC812
C013 1000P
C014 1000P
C015 1000P
C016 1000P
C008 1000P
C009 1000P
C010 1000P
C011 1000P
C012 1000P
R024 10K
R025 10K
R026 10K
R027 10K
R028 10K
D030-D039 1SS184 x10
G1(-)
G2(+)
G1(-)
G2(+)
N
SH
NEMS
R014 47K1/2W
R015 47K1/2W
R016 47K1/2W
R017 47K1/2W
R018 47K1/2W
R019 47K1/2W
R033 47K1/2W
R020 10M
R021 10M
R022 10M
R023 10M
CH003 HR16-10R-10S(04) (GREEN)
+5H
-5H
+5F
-5F
EF
A
B
C
D
E
F
G

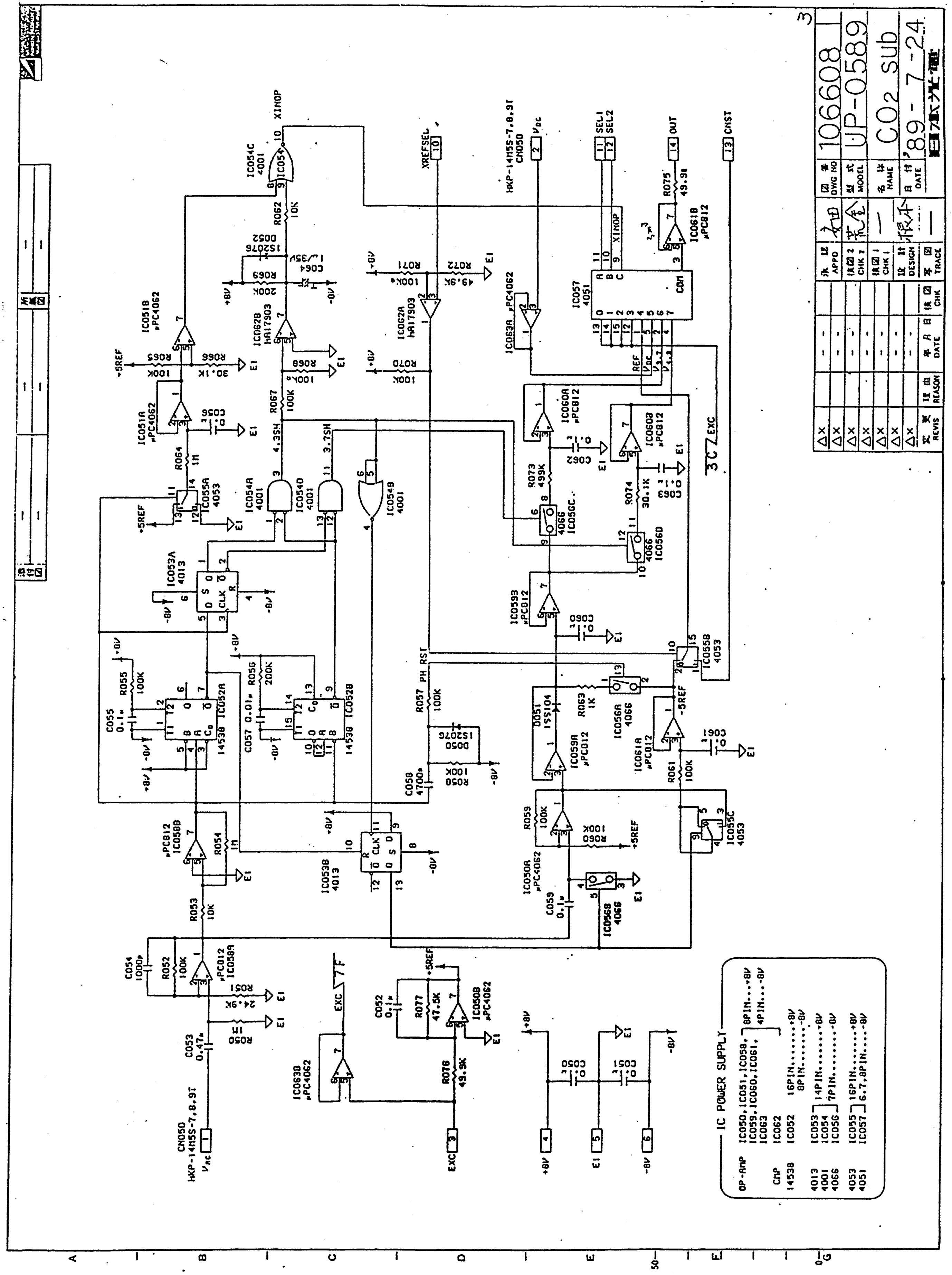
12. CIRCUIT DIAGRAM

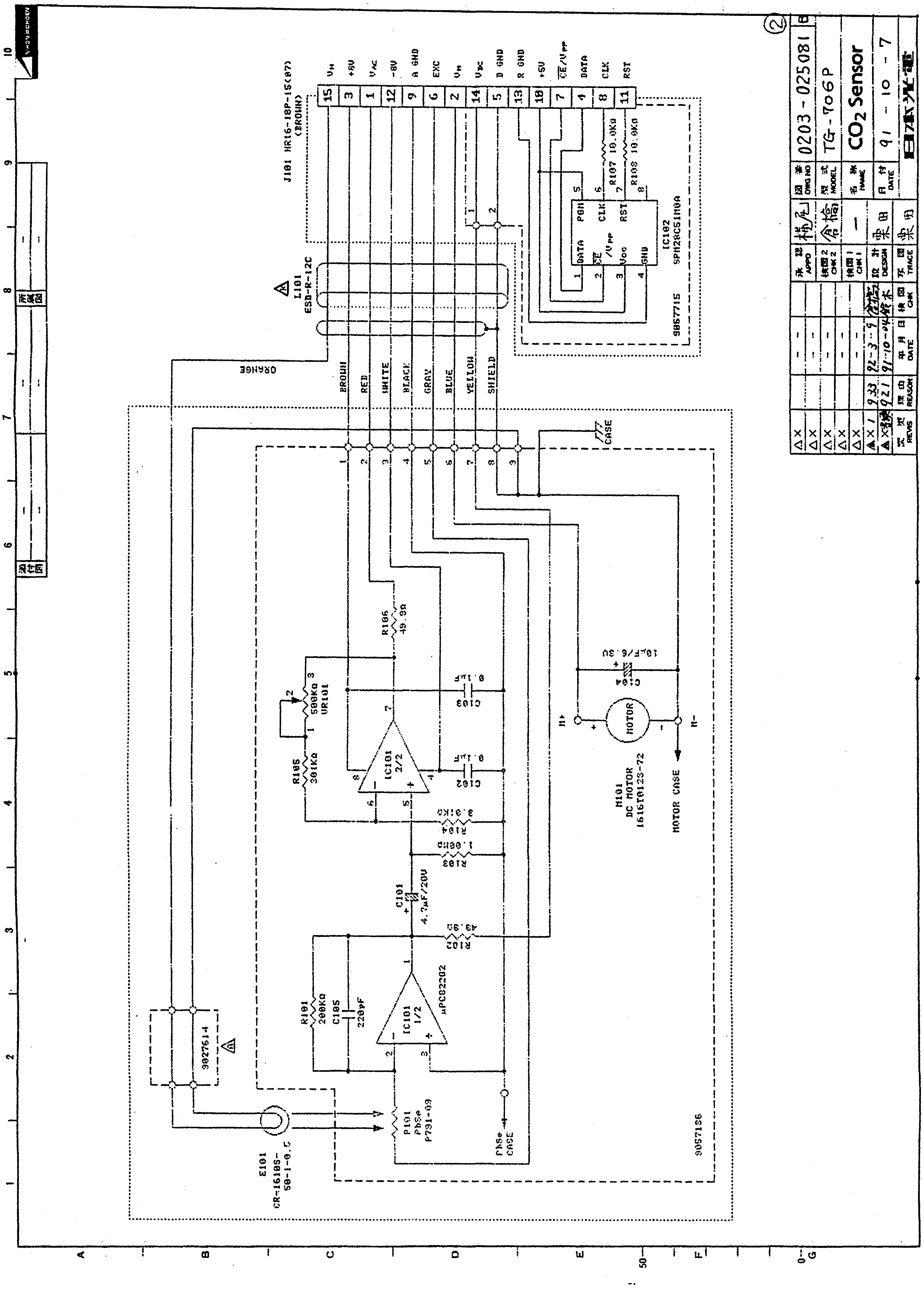

105844
UP-0422
EEG Head Amp. Sub Board
63-4-4
HKP-14MSS CN050
R050 1K
R051 1K
R052 1K
R053 1K
R054 10K
R055 10K
R056 9.76K
R057 9.76K
IC050A μPC812
IC050B μPC812
VR054 500Ω
VR055 500Ω
10μ/20V x2 C050 C051
10μ/20V x2 C054 C055
R058 634K
R059 634K
C058 6800P
C059 6800P
R062 249K
R063 249K
R060 4.99K
R061 4.99K
IC051 LT1001
IC052 LT1001
10μ/20V x2 C052 C053
10μ/20V x2 C056 C057
R064 60.4K
R065 60.4K
D050-D053 1S2076A x4
C060 4700P
C061 4700P
R066 634K
R067 634K
IC053 LT1001
IC054 LT1001
R068 15K
R069 15K
R070 15K
R071 15K
R072 10K
R073 10K
R074 10K
R075 10K
R076 475K
R077 475K
R078 475K
R079 475K
C062 0.022μ
C063 0.022μ
C064 5600P
C065 5600P
IC055A μPC4062
IC055B μPC4062
IC056A μPC4062
IC056B μPC4062
C066 C067 C068 0.047μ x3
C069 C070 C071 0.047μ x3
R080 562K
R081 562K
R082 4.75K
R083 4.75K
R084 60.1K
R085 60.1K
VR050 20K
VR051 20K
R086 825Ω
R087 825Ω
R088 3.01K
R089 3.01K
R090 2.21Ω
R091 2.21Ω
C072 10μ /20V
C073 10μ /20V
C074 0.1μ
C075 0.1μ
CN050 HKP-14MSS
+SF
-SF
+SJ
-SJ
EF

12. CIRCUIT DIAGRAM

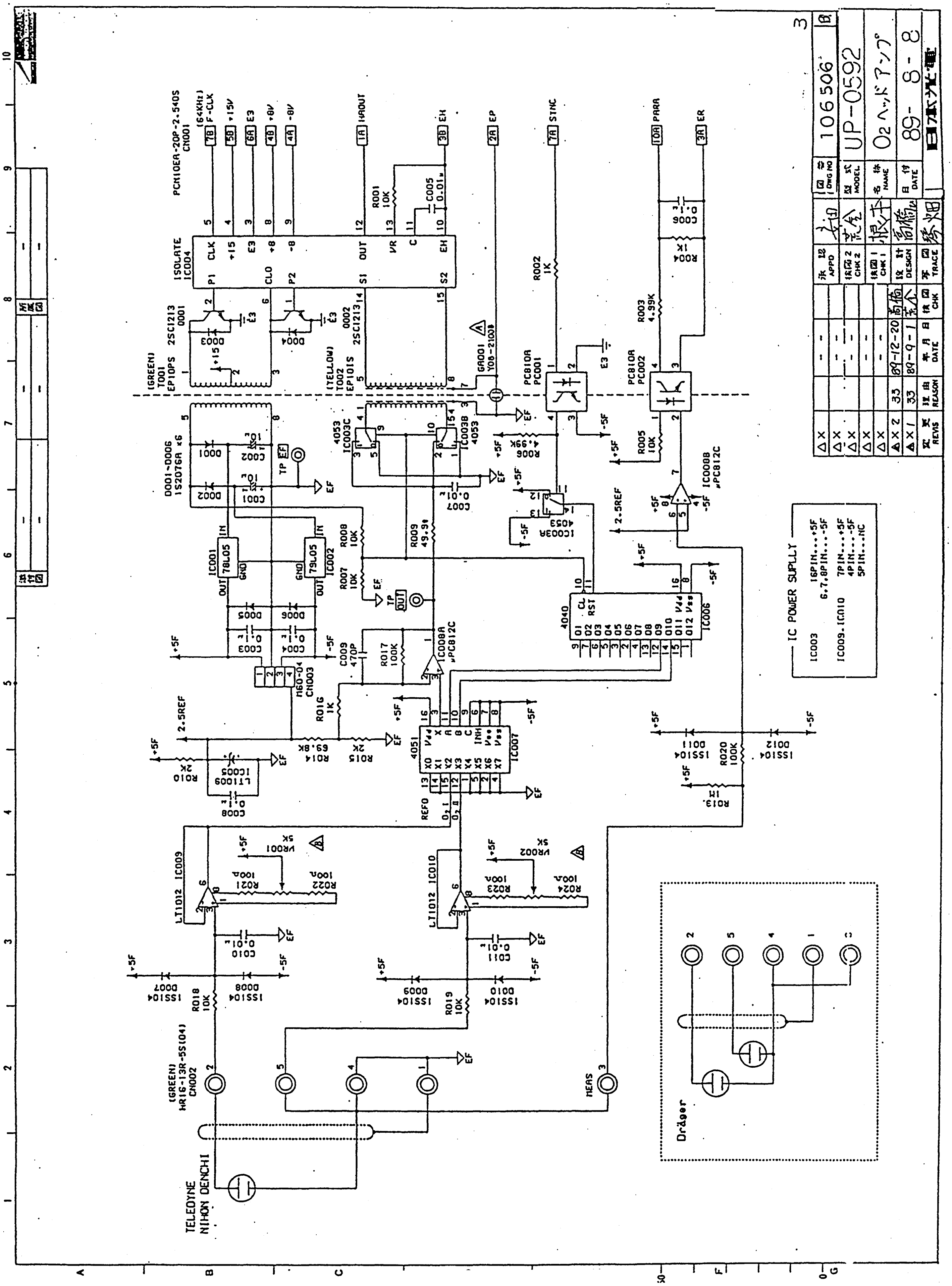

106607
UP-0588
CO2 Main
'89-7-24
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVIS
REASON
CHK
UP-0589
CN002
HKP-14FDS2-7.0.9T
CN001
PCN10ER-20P-2.54DS
CN003
HR16-18R-15S107)BROWN
IC001 4094
IC002 μPC624
IC003A 14538
IC003B 14538
IC004 4040
IC005 4040
IC006 LT1009
IC007A μPC012
IC007B μPC012
IC008A μPC4062
IC008B μPC4062
IC009A μPC4062
IC009B μPC4062
IC010A μPC4062
IC010B μPC4062
PC001 PC0104
Q001 2SA836
T001
VR001 5K
+5V
RGND
XCE/Vpp
DATA
CLK
RST
+8V
A_ENO
-8V
V_AC
EXC
V_DC
V_H
DGND
V_N
HR OUT
F-CLK
SYNC
PARA
ER
EP
E1
E3
OP-AMP POWER SUPPLY
IC007~IC010 4PIN...-8V
8PIN...+8V
A
B
C
D
E
F
G

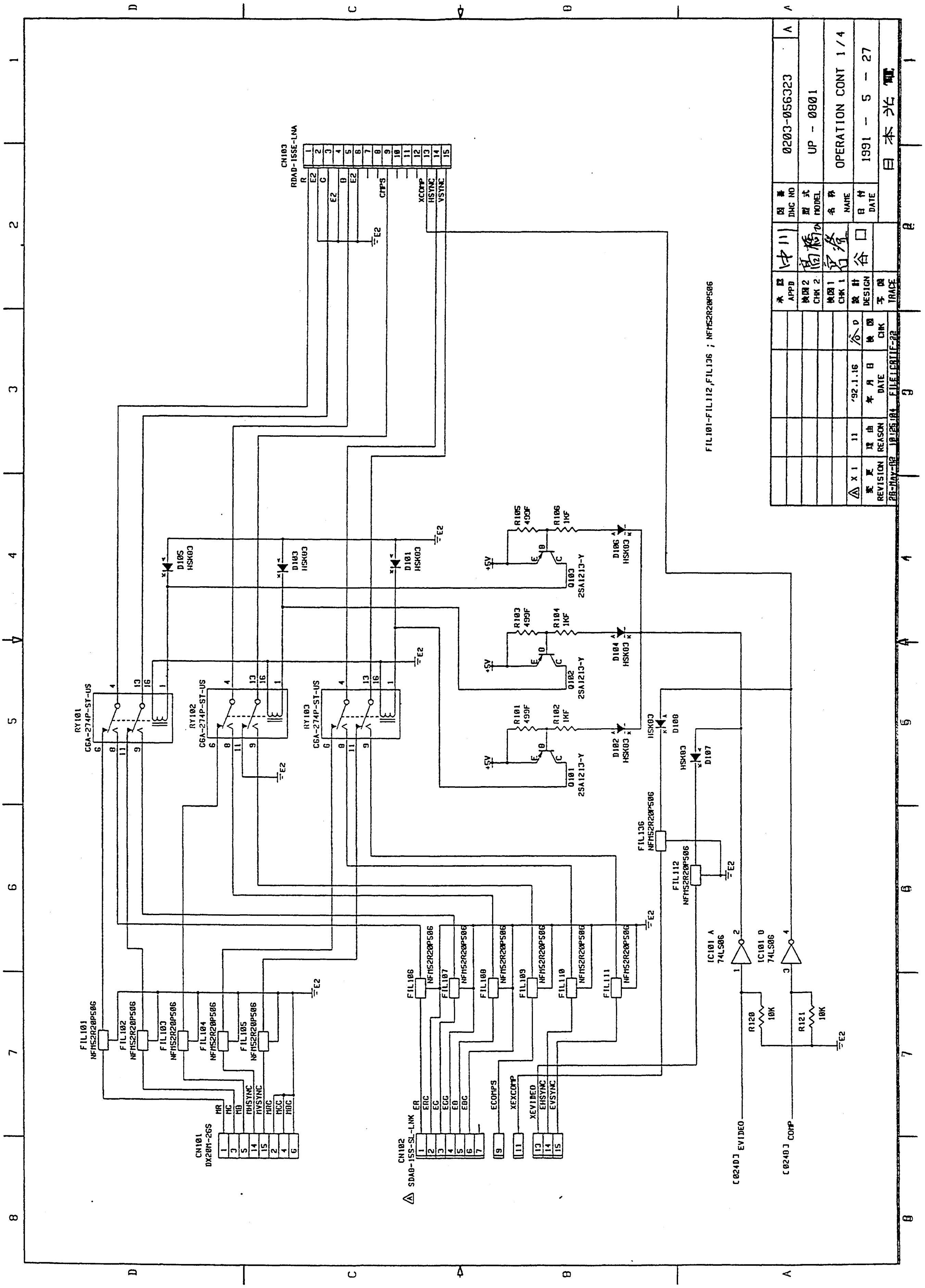
12. CIRCUIT DIAGRAM


106608
UP-0589
CO2 sub
'89-7-24
DWG NO
MODEL
NAME
DATE
APPO
CHK 2
CHK 1
DESIGN
TRACE
REVIS
REASON
CHK
3
IC POWER SUPPLY
OP-AMP IC050, IC051, IC058, IC059, IC060, IC061, IC063 8PIN...+8V 4PIN...-8V
CMP IC062
14538 IC052 16PIN.......+8V 8PIN.......-0V
4013 IC053
4001 IC054 14PIN.......+8V
4066 IC056 7PIN........-0V
4053 IC055 16PIN.......+8V
4051 IC057 6,7,8PIN....-8V
CN050 HKP-14H5S-7,8,9T
VAC
EXC
+8V
E1
-8V
XINOP
XREFSEL
VDC
SEL1
SEL2
OUT
CHST
IC054C 4001
IC051B μPC4062
IC051A μPC4062
IC062B HA17903
IC062A HA17903
IC063A μPC4062
IC057 4051
IC061B μPC812
IC060A μPC812
IC060B μPC812
IC055A 4053
IC054A 4001
IC054D 4001
IC054B 4001
IC056C 4066
IC056D 4066
IC053A 4013
IC052A 14538
IC052B 14538
IC059B μPC012
IC055B 4053
IC056A 4066
IC059A μPC012
IC061A μPC012
IC050A μPC4062
IC055C 4053
IC058B μPC812
IC053B 4013
IC056B 4066
IC058A μPC012
IC050B μPC4062
IC063B μPC4062
D050 1S2076
D051 1SS104
D052 1S2076
4.3SH
3.7SH
PH RST
+5REF
-5REF
EXC 7F
3C EXC
A
B
C
D
E
F
G

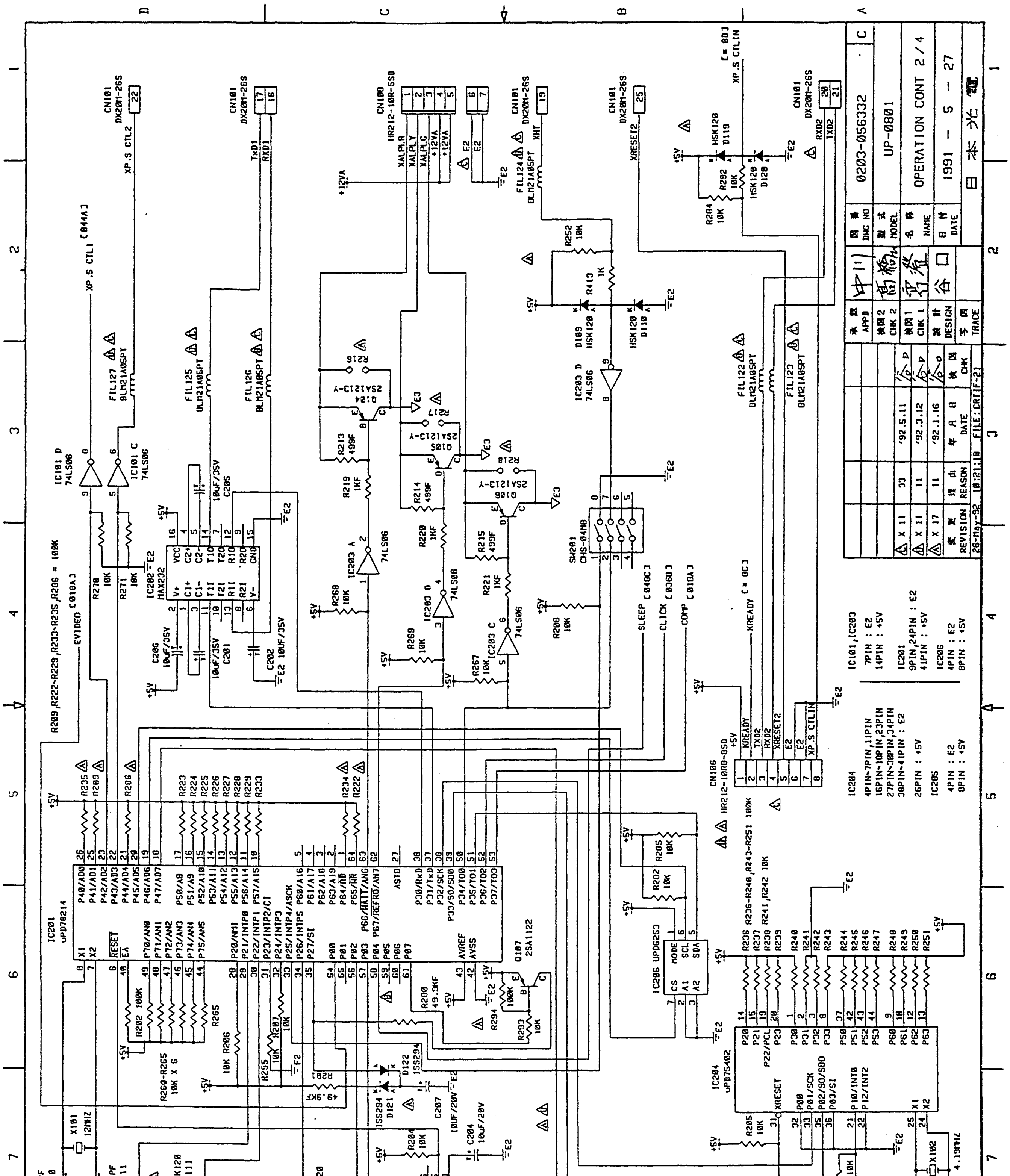

J101 HR16-18P-15(87) (BROWN)
15 V_H
3 +8V
1 V_AC
12 -8V
9 A GND
6 EXC
2 V_H
14 V_DC
5 D GND
13 R GND
10 +5V
7 CE/V_PP
4 DATA
8 CLK
11 RST
R107 10.0kΩ
R108 10.0kΩ
IC102 SPM28C51M0A
DATA
CE/V_PP
V_DD
GND
PGM
CLK
RST
9067715
L101 ESD-R-12C
ORANGE
BROWN
RED
WHITE
BLACK
GRAY
BLUE
YELLOW
SHIELD
CASE
R106 49.9Ω
UR101 500kΩ
R105 301kΩ
IC101 2/2
C103 0.1µF
C102 0.1µF
R104 3.01kΩ
R103 1.00kΩ
C101 4.7µF/20V
R102 49.9Ω
R101 200kΩ
C105 220pF
IC101 1/2 µPC8220Z
9027614
P101 PbSe P791-69
PbSe CASE
E101 CR-1610S-50-1-0.5
9057136
C104 10µF/6.3V
MOTOR
M+
M-
M101 DC MOTOR 1616T0123-72
MOTOR CASE
②
0203-025081
TG-906P
CO2 Sensor
91-10-7
A B C D E F G
1 2 3 4 5 6 7 8 9 10

12. CIRCUIT DIAGRAM

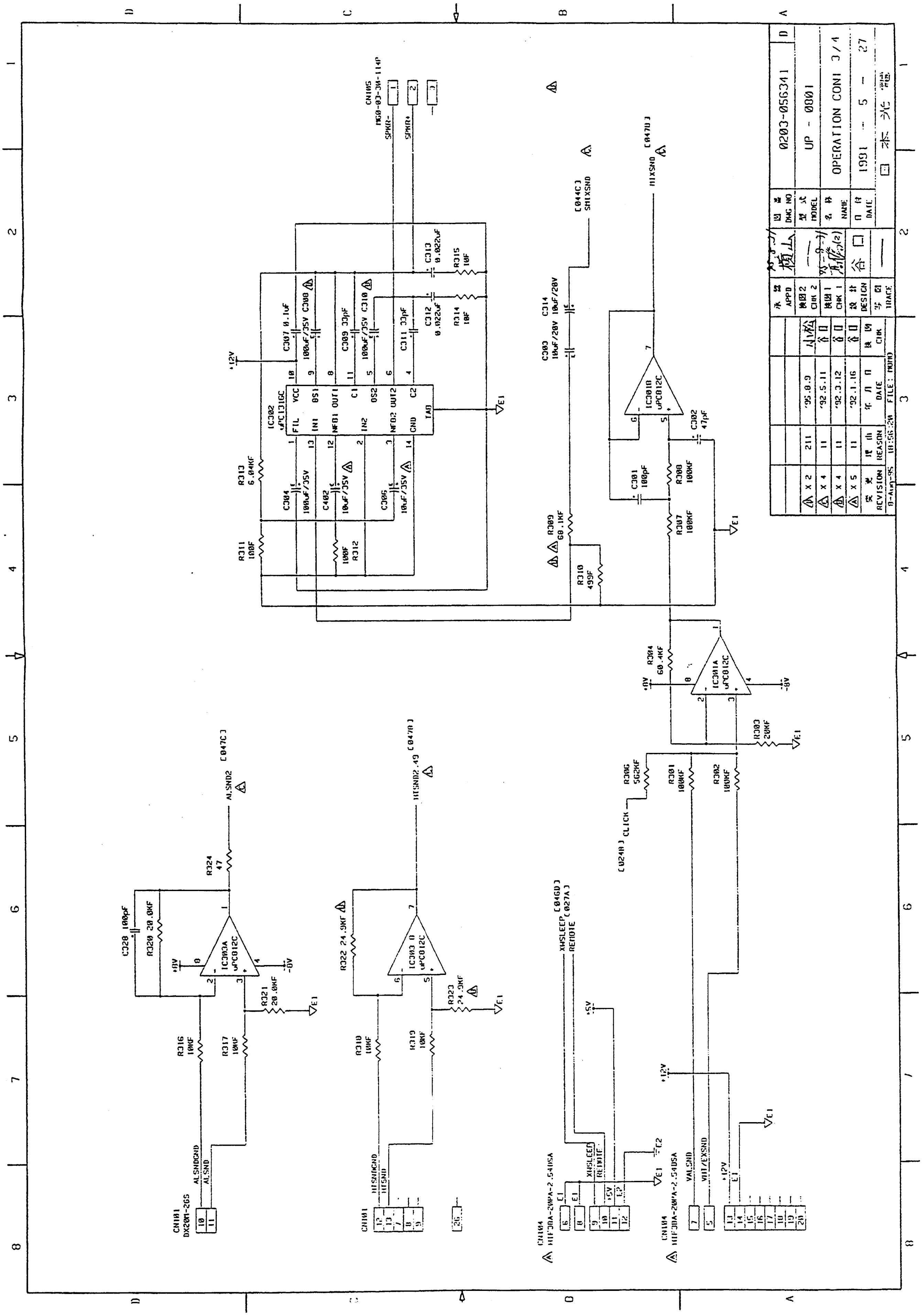

106506
UP-0592
O2ヘッドアンプ
89-8-8
日本光電
33 89-12-20
33 89-9-1
PCN10EA-20P-2.54DS CN001
F-CLK
+15V
E3
+8V
-8V
HAOUT
EH
EP
SYNC
PARA
ER
ISOLATE IC004
2SC1213 Q001
2SC1213 Q002
T001 EP10PS
T002 EP101S
PC810A PC001
PC810A PC002
4053 IC003A
4053 IC003B
4053 IC003C
78L05 IC001
79L05 IC002
4040 IC006
4051 IC007
µPC812C IC008A
µPC812C IC008B
LT1012 IC009
LT1012 IC010
LT1009 IC005
D001-D006 1S2076A x6
IC POWER SUPPLY
IC003 16PIN...+5F 6,7,8PIN...-5F
IC009, IC010 7PIN...+5F 4PIN...-5F 5PIN...NC
HR16-13R-5S(04) CN002
TELEDYNE
NIHON DENCHI
Dräger
MEAS
2.5REF
+5F
-5F
EF
VR001 5K
VR002 5K


0203-056323
UP - 0801
OPERATION CONT 1/4
1991 - 5 - 27
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
'92.1.16
FIL101-FIL112,FIL136 ; NFM52R20P506
CN103
RDAD-15SE-LNA
CN101
DX20M-26S
CN102
SDA0-15S-SL-LNK
RY101
G6A-274P-ST-US
RY102
G6A-274P-ST-US
RY103
G6A-274P-ST-US
D101
D103
D105
HSK03
Q101
Q102
Q103
2SA1213-Y
R101
R103
R105
499F
R102
R104
R106
1KF
D102
D104
D106
D107
D108
HSK03
FIL101
FIL102
FIL103
FIL104
FIL105
FIL106
FIL107
FIL108
FIL109
FIL110
FIL111
FIL112
FIL136
NFM52R20P506
IC101 A
IC101 D
74LS06
R120
R121
10K
+5V
E2
MR
MG
MHSYNC
MVSYNC
MRC
MGC
MBC
ER
ERC
EG
EGC
EB
EBC
ECOMPS
XEXCOMP
XEVIDEO
EHSYNC
EVSYNC
CMPS
XCOMP
HSYNC
VSYNC
[0240] EVIDEO
[0240] COMP

12. CIRCUIT DIAGRAM

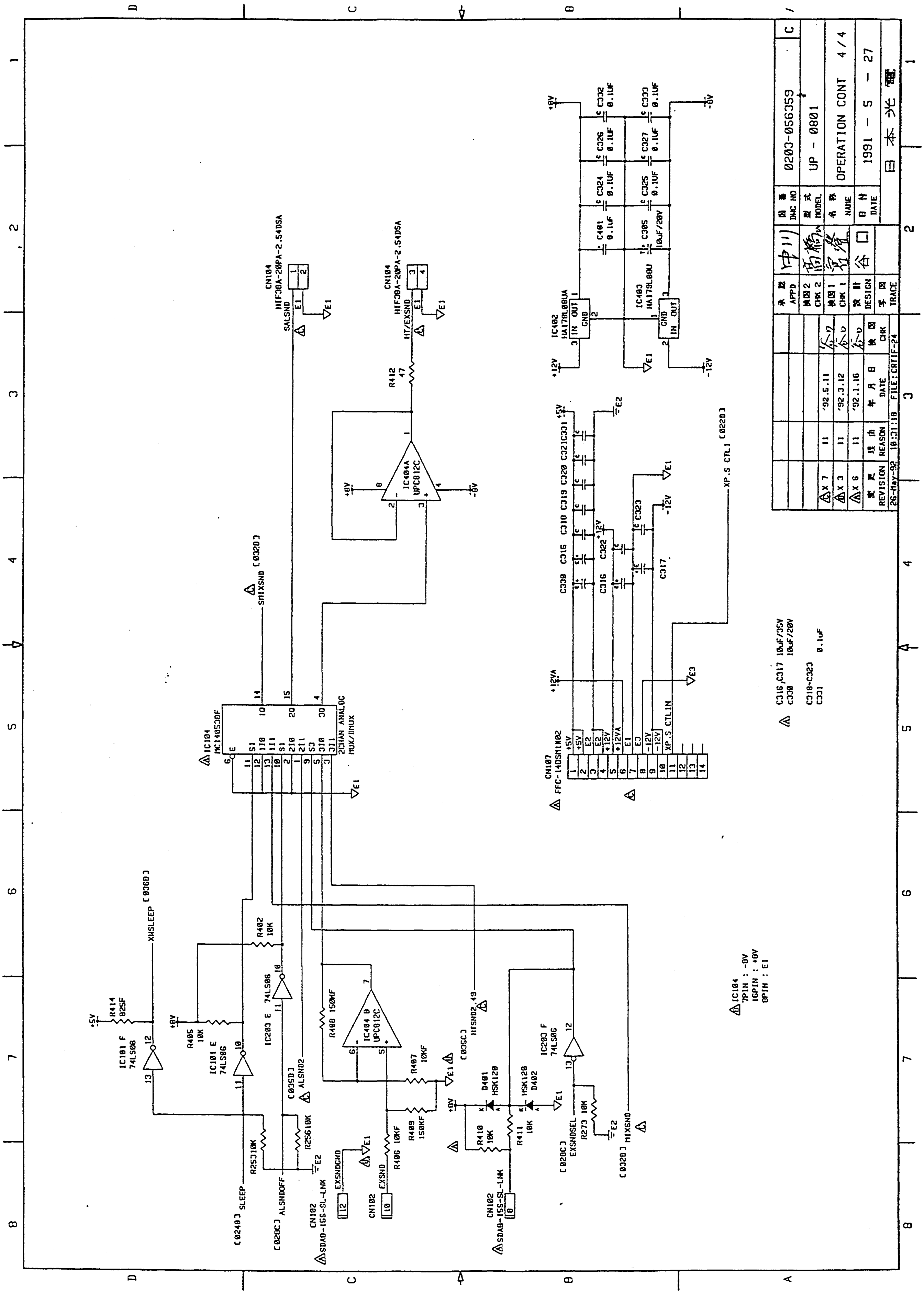

0203-056332
UP-0801
OPERATION CONT 2/4
1991 - 5 - 27
IC201 uPD78214
IC202 MAX232
IC203 74LS06
IC204 uPD75402
IC205 TL7705
IC206 UPD6253
IC101 74LS06
CN100 HR212-10R-5SD
CN101 DX20M-26S
CN106 HR212-10R0-8SD
SW201 CHS-04MB
X101 12MHZ
X102 4.19MHZ
Q104 2SA1213-Y
Q105 2SA1213-Y
Q106 2SA1213-Y
Q107 2SA1122
R209,R222-R229,R233-R235,R206 = 100K
R236-R240,R243-R251 100K
R241,R242 10K
R260-R265 10K X 6
XP.S CTL1
XP.S CTL2
XP.S CTLIN
EVIDEO
SLEEP
CLICK
COMP
KREADY
XRESET2
XRESET1
REMOTE
READY
ALSNDOFF
EXSNDSEL
M/S SEL
TXD1
RXD1
TXD2
RXD2
XALPLR
XALPLY
XALPLC
+12VA
XHT
IC101,IC203 7PIN : E2 14PIN : +5V
IC201 9PIN,24PIN : E2 41PIN : +5V
IC206 4PIN : E2 8PIN : +5V
IC204 4PIN~7PIN,11PIN 16PIN~19PIN,23PIN 27PIN~30PIN,34PIN 38PIN~41PIN : E2
26PIN : +5V
IC205 4PIN : E2 8PIN : +5V
26-May-92 10:21:10 FILE:CRTIF-21

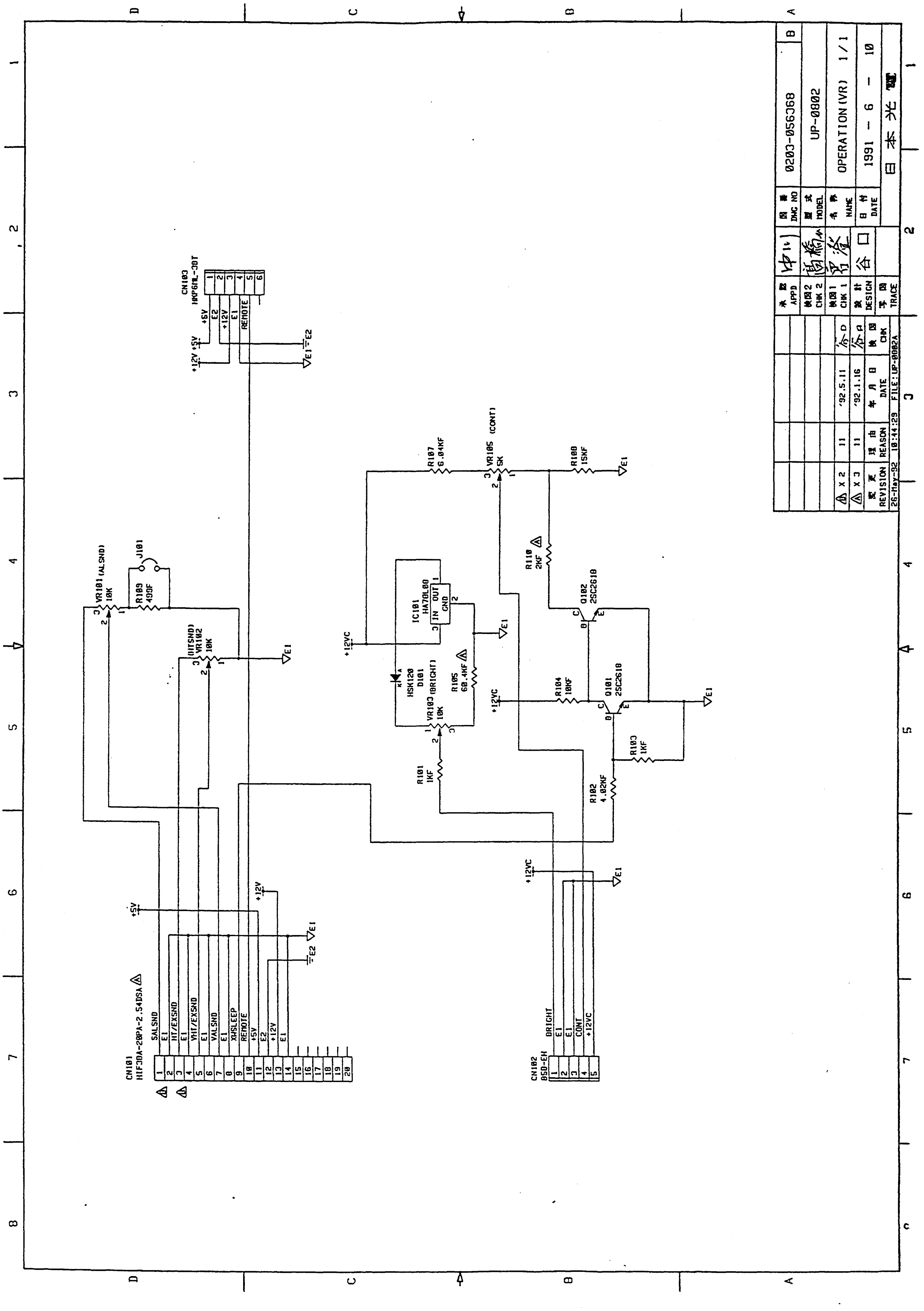
12. CIRCUIT DIAGRAM



0203-056341
D
UP - 0001
OPERATION CONT 3/4
1991 - 5 - 27
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
'95.8.9
'92.5.11
'92.3.12
'92.1.16
FILE: MONO
IC302 uPC1316C
IC301A uPC012C
IC301B uPC012C
IC303A uPC012C
IC303B uPC012C
CN105 MG0-03-3A-114P
SPKR-
SPKR+
MIXSND
SMIXSND
ALSND2
HTSND2
CLICK
XHSLEEP
REMOTE
VALSND
VHT/EXSND
ALSNDGND
ALSND
HTSNDGND
HTSND
CN101 DX20M-26S
CN104 HIF3DA-20PA-2.54DSA
+12V
+5V
+8V
-8V
E1
E2

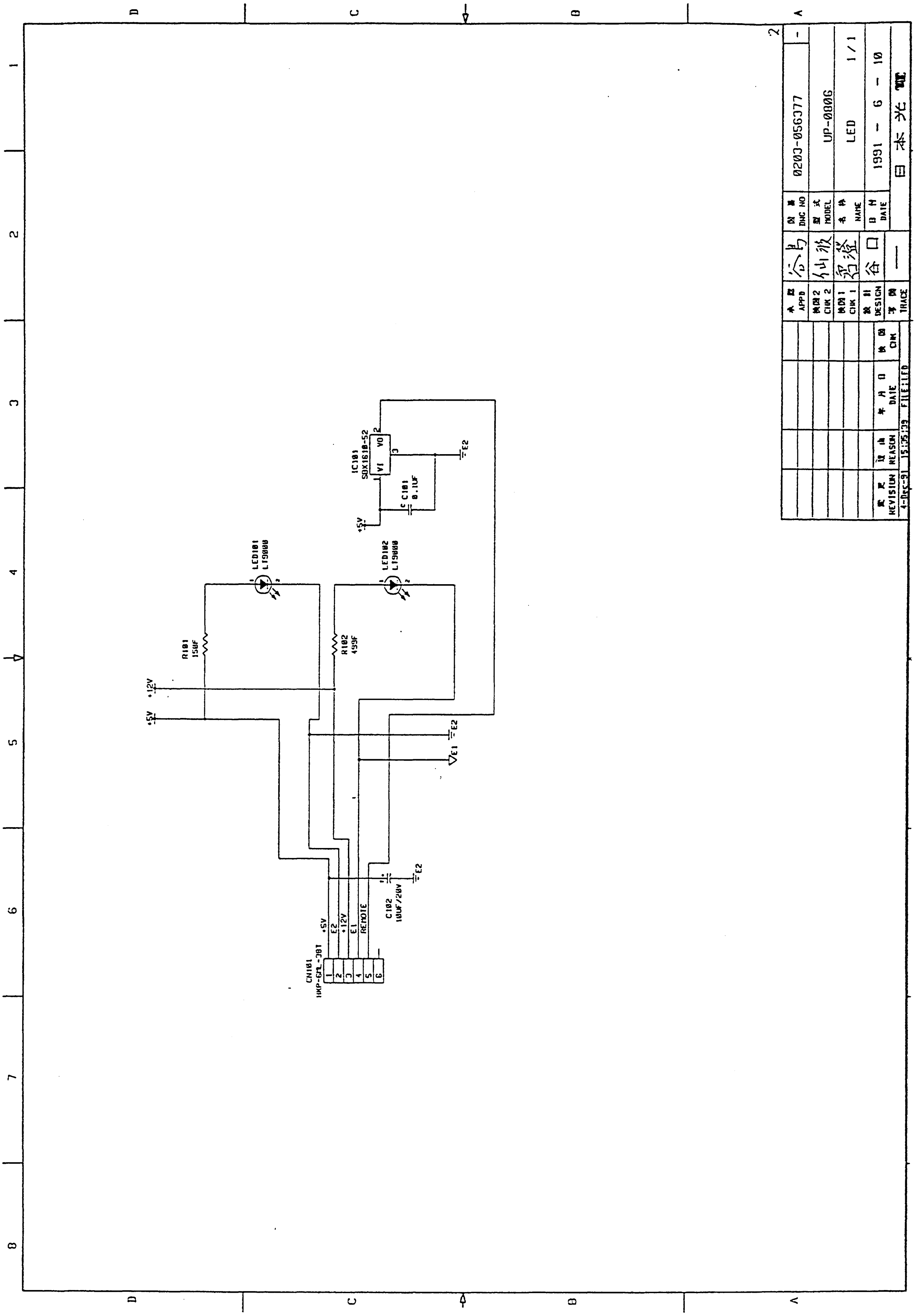
12. CIRCUIT DIAGRAM


0203-056359
UP - 0801
OPERATION CONT 4/4
1991 - 5 - 27
日本光電
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
△X 7 11 '92.6.11
△X 3 11 '92.3.12
△X 6 11 '92.1.16
26-May-92 10:31:10 FILE:CRTIF-24
IC104 MC14053DF
2CHAN ANALOG MUX/DMUX
IC404A UPC012C
IC404 B UPC012C
IC101 F 74LS06
IC101 E 74LS06
IC203 E 74LS06
IC203 F 74LS06
IC402 HA178L08UA
IC403 HA179L08U
CN104 HIF3BA-20PA-2.54DSA
CN107 FFC-14BSM1N02
CN102 SDAB-15S-SL-LNK
SALSND
HT/EXSND
SMIXSND [0320]
XHSLEEP [0360]
SLEEP [0240]
ALSNDOFF [020C]
ALSND2 [035D]
EXSNDGND
EXSND
EXSNDSEL [020C]
MIXSND [0320]
HTSND2,49 [035C]
XP.S CTL [0220]
R412 47
R414 825F
R405 10K
R402 10K
R408 150KF
R407 10KF
R409 150KF
R406 10KF
R410 10K
R411 10K
R273 10K
R253 10K
R256 10K
D401 HSK120
D402 HSK120
C332 0.1UF
C333 0.1UF
C326 0.1UF
C327 0.1UF
C324 0.1UF
C325 0.1UF
C401 0.1uF
C305 10uF/20V
C330 C315 C310 C319 C320 C321 C331
C316 C322 C323 C317
C316,C317 10uF/35V
C330 10uF/20V
C318-C323 C331 0.1uF
IC104 7PIN : -8V 16PIN : +8V 8PIN : E1
+5V
+8V
-8V
+12V
-12V
+12VA
E1
E2
E3



0203-056368
B
UP-0802
OPERATION (VR) 1/1
1991 - 6 - 10
日本光電
図番 DWG NO
型式 MODEL
名称 NAME
日付 DATE
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
11 '92.5.11
11 '92.1.16
変更 REVISION
理由 REASON
年月日 DATE
検図 CHK
26-May-92 10:44:29 FILE:UP-0802A
CN103 HKP6ML-30T
+5V
E2
+12V
E1
REMOTE
E1
E2
VR101 (ALSND) 10K
R109 499F
J101
VR102 (HITSND) 10K
IC101 HA70L08
IN OUT GND
D101 HSK120
VR103 (BRIGHT) 10K
R105 60.4KF
R101 1KF
R107 6.04KF
VR105 (CONT) 5K
R108 15KF
R110 2KF
Q102 2SC2618
Q101 2SC2618
R104 10KF
R103 1KF
R102 4.02KF
+12VC
CN101 HIF3DA-20PA-2.54DSA
SALSND
E1
HT/EXSND
E1
VHT/EXSND
E1
VALSND
E1
XWSLEEP
REMOTE
+5V
E2
+12V
E1
CN102 B5D-EH
BRIGHT
E1
E1
CONT
+12VC

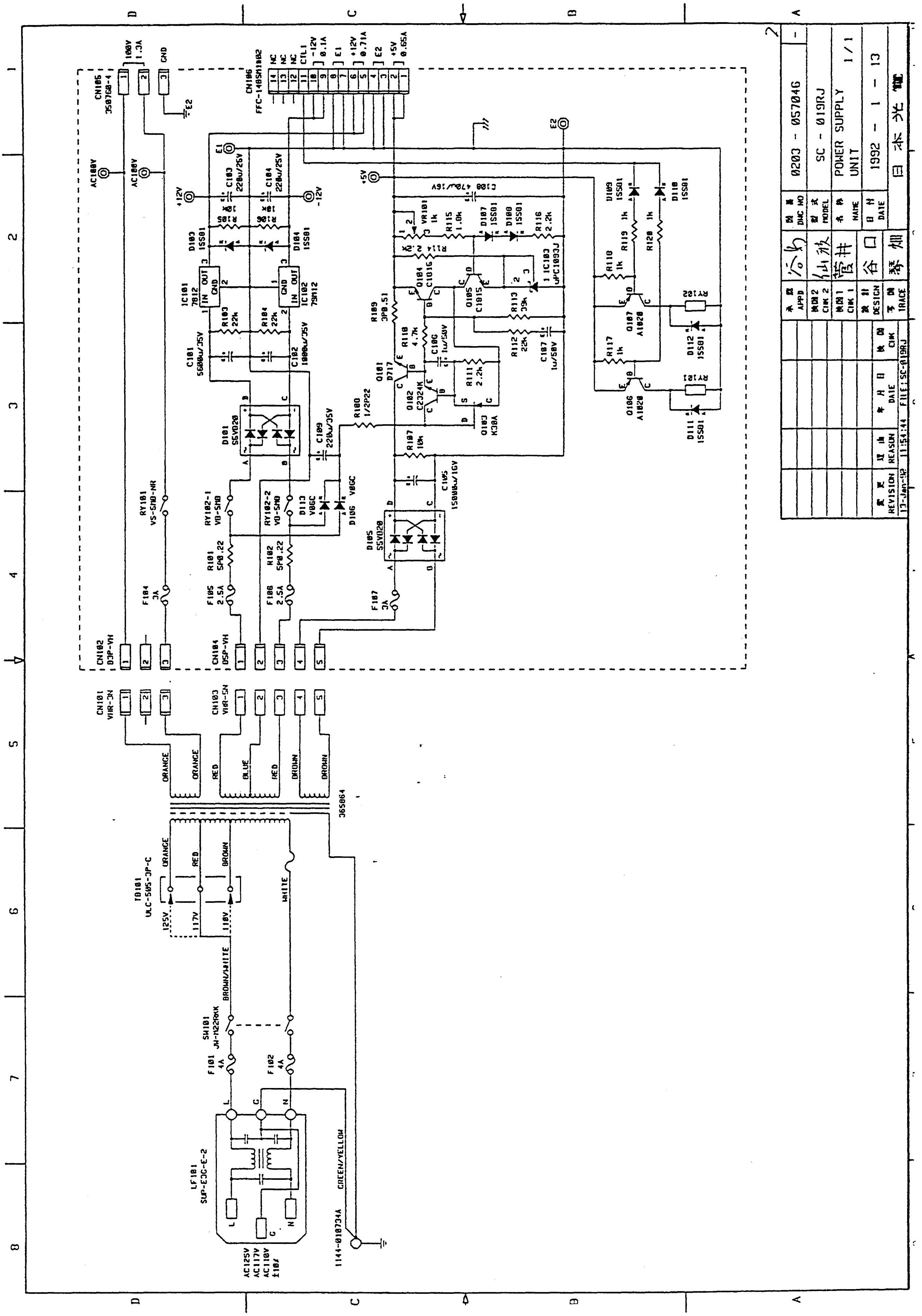
12. CIRCUIT DIAGRAM



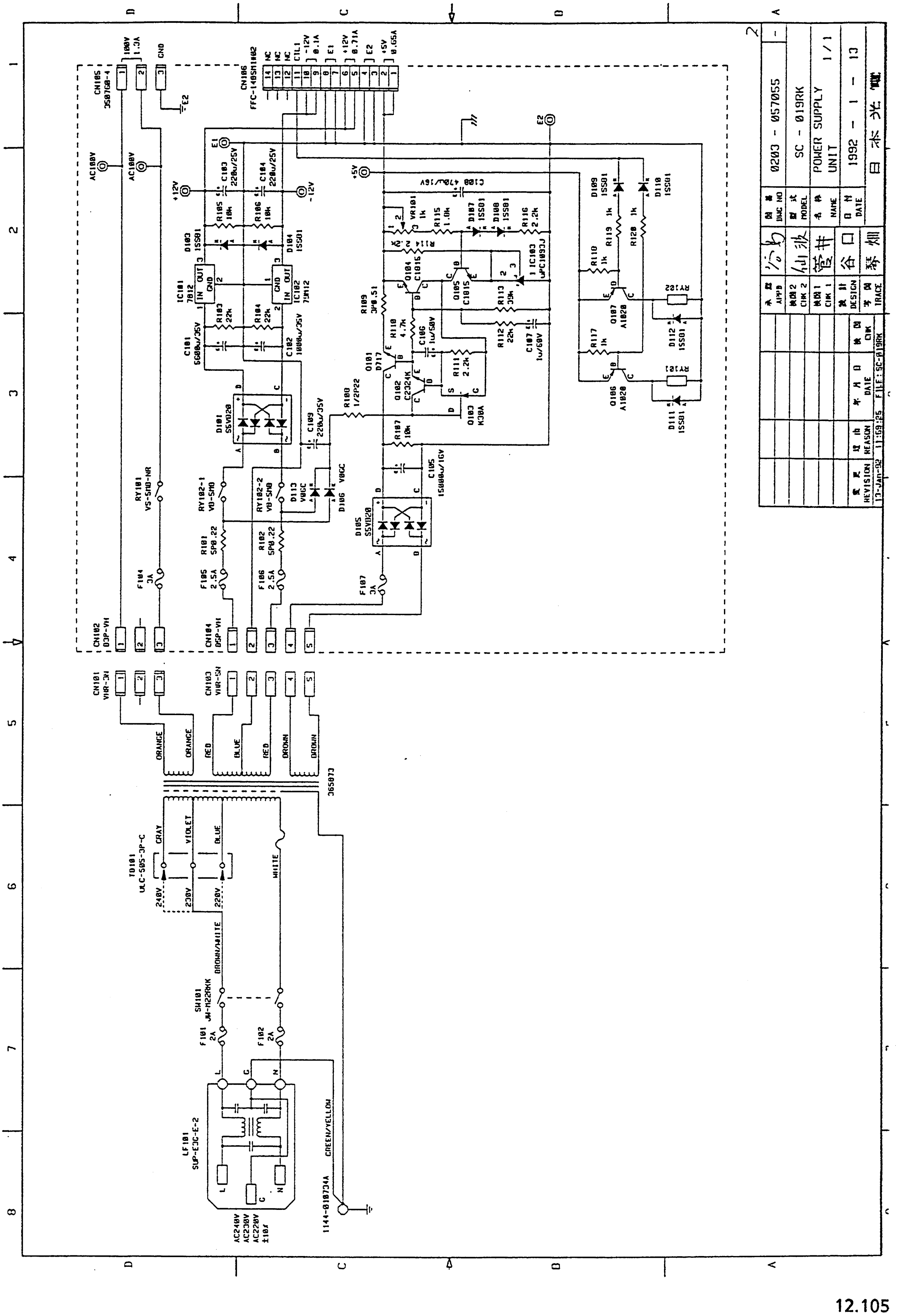
A
B
C
D
1
2
3
4
5
6
7
8
IC101
SDX1610-52
VI
VO
1
2
3
C101
0.1UF
E2
+5V
LED101
LT9000
LED102
LT9000
R101
150F
R102
499F
+12V
+5V
E2
E1
C102
10UF/20V
E2
CN101
HKP-6FL-3BT
1
2
3
4
5
6
+5V
E2
+12V
E1
REMOTE
2
-
図 番 DWG NO
0203-056377
型 式 MODEL
UP-0006
名 称 NAME
LED
1/1
日 付 DATE
1991 - 6 - 10
日 本 光 電
承 認 APPD
検 図2 CHK 2
検 図1 CHK 1
設 計 DESIGN
写 図 TRACE
変 更 REVISION
理 由 REASON
年 月 日 DATE
検 図 CHK
4-Dec-91 15:35:39 FILE:LED

NO CONTENTS

12. CIRCUIT DIAGRAM

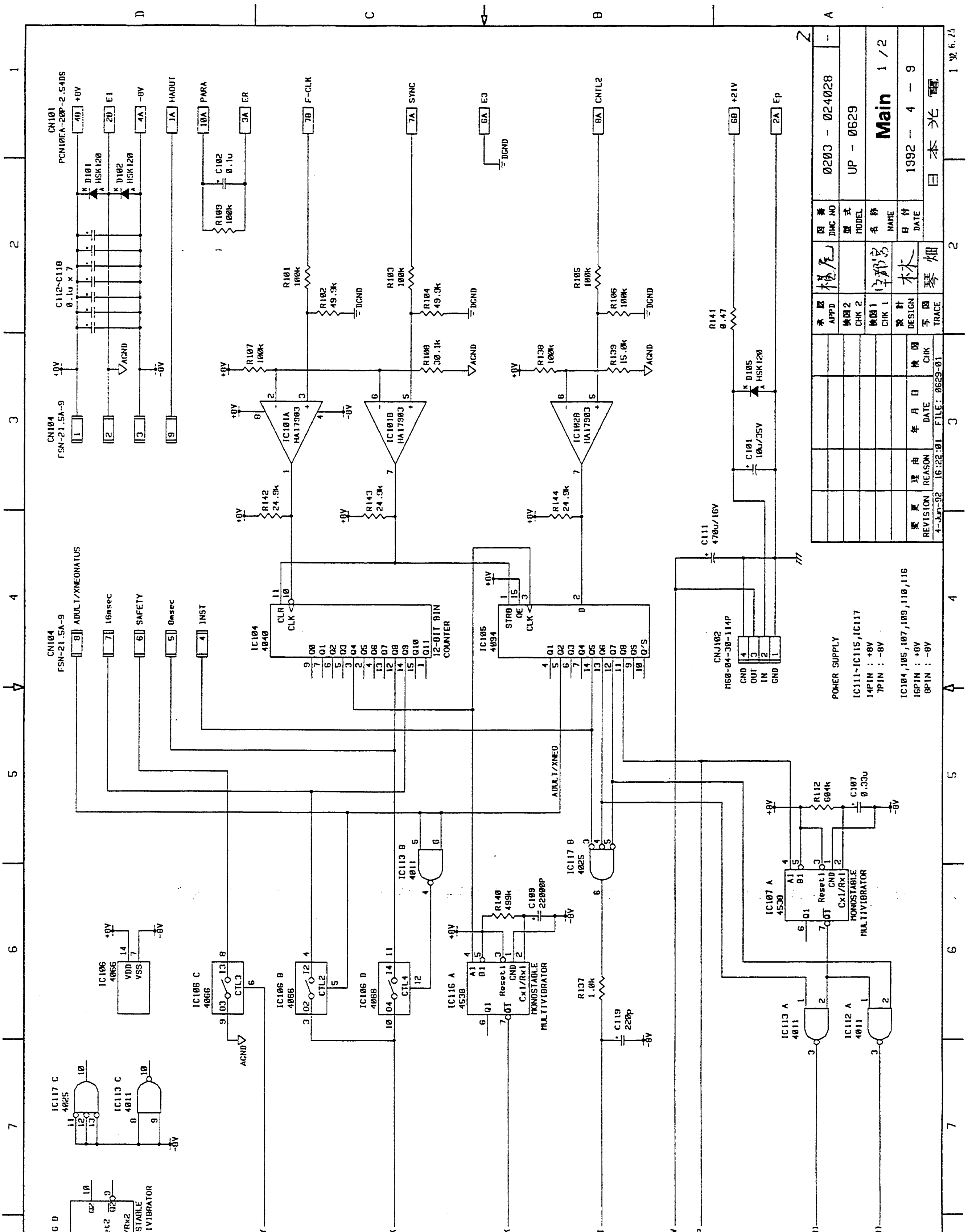

CN105 350760-4
100V 1.3A
GND
CN106 FFC-14BSM1B02
NC
CTL1
-12V 0.1A
E1
+12V 0.71A
E2
+5V 0.65A
AC100V
+12V
-12V
+5V
C103 220u/25V
C104 220u/25V
C108 470u/16V
IC101 7812
IC102 79M12
IC103 uPC1093J
C101 5600u/35V
C102 1000u/35V
D101 S5VB20
D105 S5VB20
C105 15000u/16V
C109 220u/35V
RY101 VS-5MD-NR
RY102-1 VB-5MD
RY102-2 VB-5MD
RY101
RY102
F104 3A
F105 2.5A
F106 2.5A
F107 3A
R101 5P0.22
R102 5P0.22
CN102 D3P-VH
CN104 D5P-VH
CN101 VHR-3N
CN103 VHR-5N
ORANGE
RED
BLUE
BROWN
365064
TB101 ULC-505-3P-C
125V
117V
100V
WHITE
BROWN/WHITE
SW101 JH-M22HHK
F101 4A
F102 4A
LF101 SUP-E3G-E-2
AC125V
AC117V
AC100V
±10%
GREEN/YELLOW
1144-010734A
0203 - 057046
SC - 019RJ
POWER SUPPLY UNIT
1/1
1992 - 1 - 13
REVISION
REASON
DATE
FILE:SC-019RJ
13-Jan-92 11:54:44

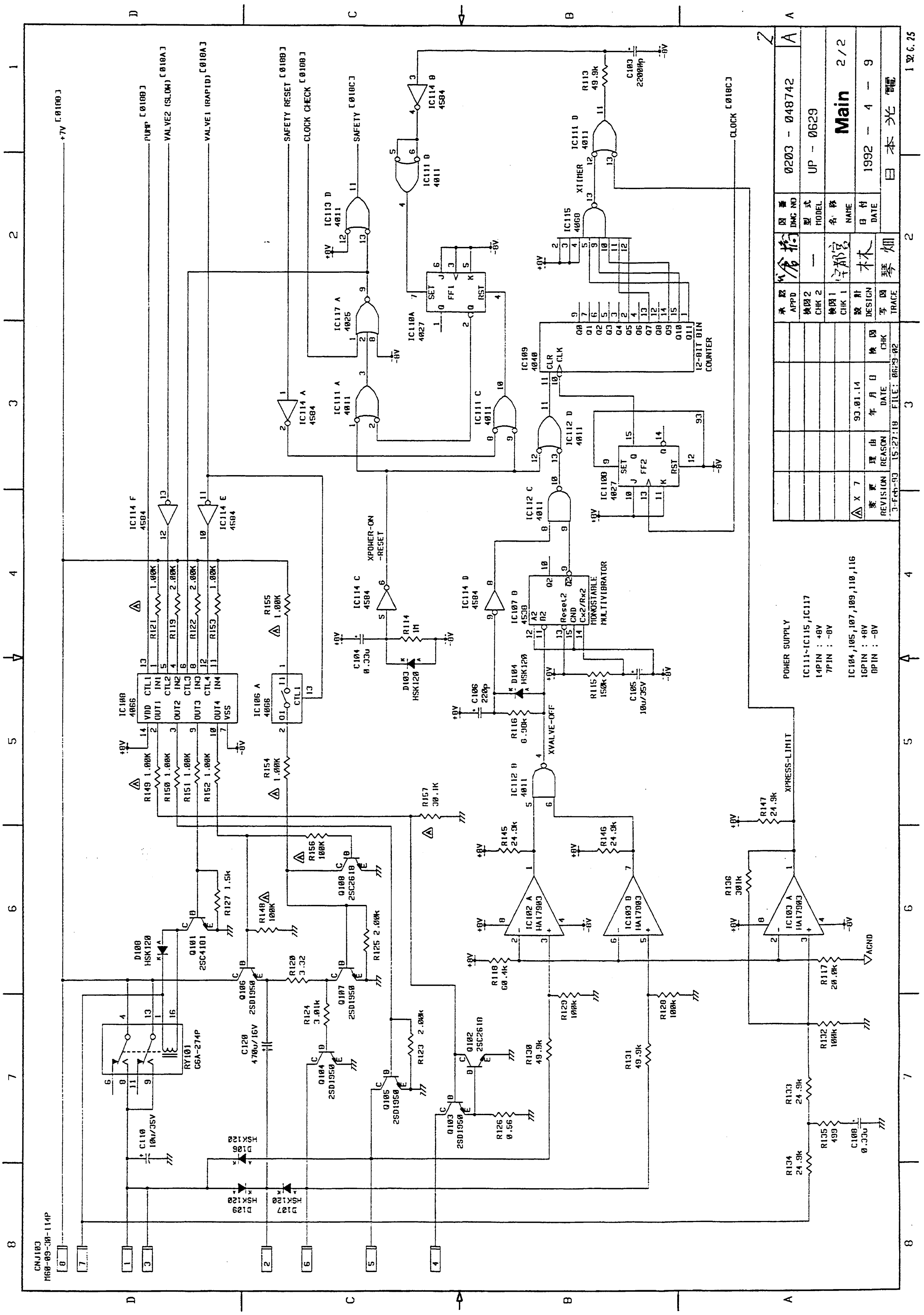
12. CIRCUIT DIAGRAM



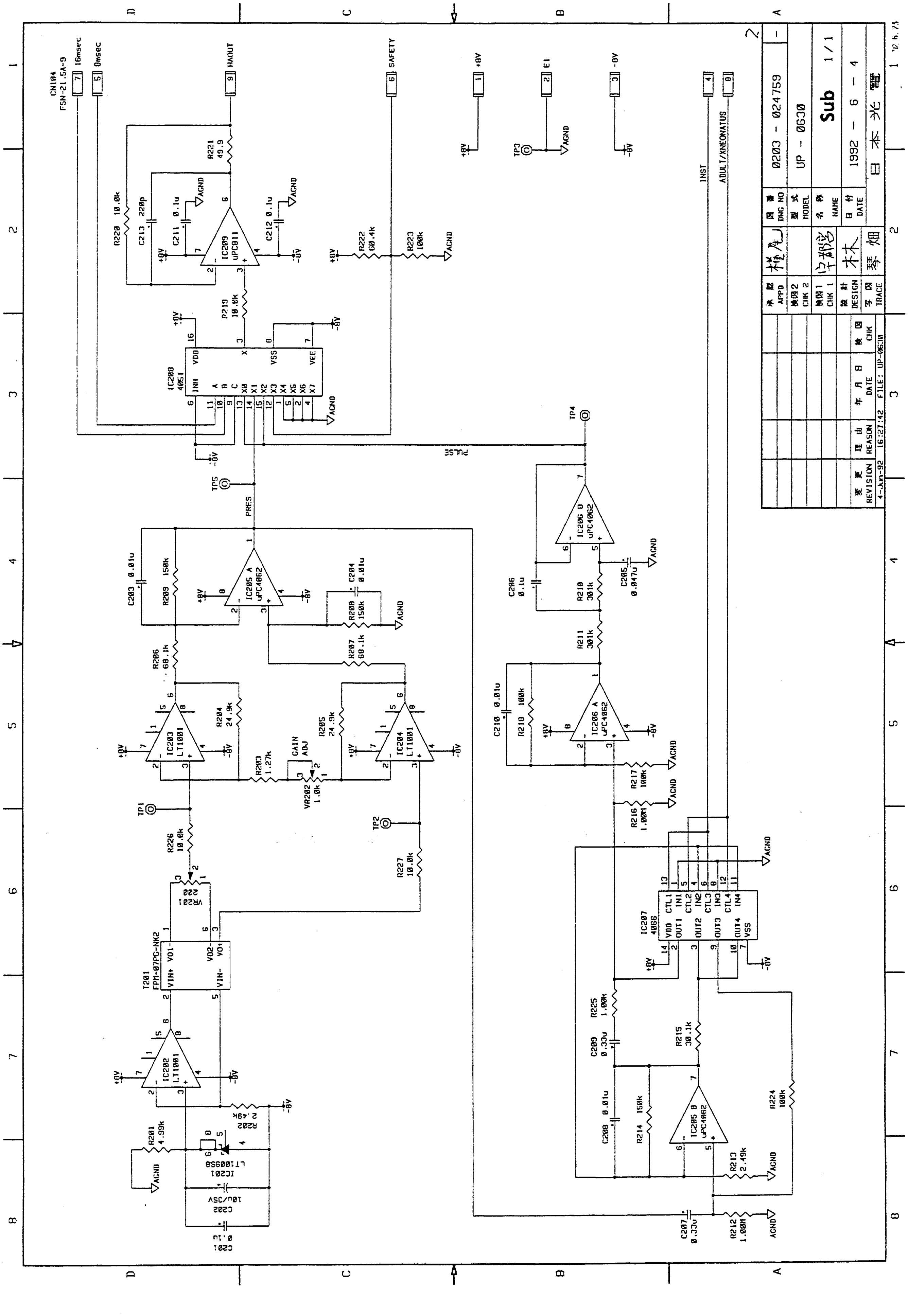
0203 - 057055
SC - 019RK
POWER SUPPLY UNIT
1/1
1992 - 1 - 13
DWG NO
MODEL
NAME
DATE
APP'D
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
13-Jan-92 11:59:25 FILE:SC-019RK
CN105 3507G0-4
100V 1.3A
GND
CN106 FFC-14BSM1N02
NC
CTL1
-12V 0.1A
E1
+12V 0.71A
E2
+5V 0.65A
AC100V
+12V
-12V
+5V
C103 220u/25V
C104 220u/25V
C108 470u/16V
R105 10k
R106 10k
D103 1SS81
D104 1SS81
IC101 7812
IC102 79M12
R103 22k
R104 22k
C101 5600u/35V
C102 1000u/35V
D101 S5VB20
C109 220u/35V
R100 1/2P22
RY101 VS-5HD-NR
RY102-1 VB-5H0
RY102-2 VB-5H0
D113 V06C
D106 V06C
R101 5P0.22
R102 5P0.22
F104 3A
F105 2.5A
F106 2.5A
F107 3A
D105 S5VB20
C105 15000u/16V
R107 10k
Q101 D717
Q102 C2324K
Q103 K30A
Q104 C1815
Q105 C1815
R108 3P0.51
R110 4.7k
C106 1u/50V
R111 2.2k
R112 22k
R113 39k
C107 1u/50V
VR101 1k
R115 1.0k
R114
D107 1SS81
D108 1SS81
R116 2.2k
IC103 uPC1093J
D109 1SS81
D110 1SS81
R110 1k
R119 1k
R120 1k
R117 1k
Q107 A1020
Q106 A1020
RY102
RY101
D112 1SS81
D111 1SS81
CN102 03P-VH
CN104 05P-VH
CN101 VHR-3N
CN103 VHR-5N
ORANGE
RED
BLUE
BROWN
365073
TD101 ULC-505-3P-C
GRAY
VIOLET
WHITE
240V
230V
220V
BROWN/WHITE
SW101 JW-M22RKK
F101 2A
F102 2A
LF101 SUP-E3C-E-2
GREEN/YELLOW
1144-010734A
AC240V AC230V AC220V ±10%

12. CIRCUIT DIAGRAM


0203 - 024028
UP - 0629
Main 1 / 2
1992 - 4 - 9
日本光電
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
4-Jun-92
16:22:01
FILE: 0629-01
CN101 PCN10EA-20P-2.54DS
CN104 FSN-21.5A-9
CN102 M60-04-30-114P
IC101A HA17903
IC101D HA17903
IC102B HA17903
IC104 4040 12-BIT BIN COUNTER
IC105 4094
IC106 4066
IC107 A 4538 MONOSTABLE MULTIVIBRATOR
IC116 A 4538 MONOSTABLE MULTIVIBRATOR
IC116 D 4538 MONOSTABLE MULTIVIBRATOR
IC113 4011
IC112 A 4011
IC117 4025
+0V
-8V
+8V
+21V
AGND
DGND
E1
E3
Ep
HAOUT
PARA
ER
F-CLK
SYNC
CNTL2
ADULT/XNEONATUS
ADULT/XNEO
16msec
8msec
SAFETY
INST
POWER SUPPLY
IC111-IC115,IC117
14PIN : +8V
7PIN : -8V
IC104,105,107,109,110,116
16PIN : +8V
8PIN : -8V
[021C] SAFETY
[021A] CLOCK
[021C] CLOCK CHECK
[021C] SAFETY RESET
[021D] +7V
[021D] PUMP
[021D] VALVE2 (SLOW)
[021D] VALVE1 (RAPID)
GND
OUT
IN
GND


0203 - 048742
UP - 0629
Main 2/2
1992 - 4 - 9
日本光電
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
DATE
CHK
3-Feb-93
15:27:18
93.01.14
FILE: 0629-02
POWER SUPPLY
IC111-IC115,IC117
14PIN : +8V
7PIN : -8V
IC104,105,107,109,110,116
16PIN : +8V
8PIN : -8V
+7V [010B]
PUMP [010B]
VALVE2 (SLOW) [010A]
VALVE1 (RAPID) [010A]
SAFETY RESET [010B]
CLOCK CHECK [010B]
SAFETY [010C]
CLOCK [010C]
XTIMER
XPOWER-ON -RESET
XVALVE-OFF
XPRESS-LIMIT
AGND
IC114 B 4584
IC111 B 4011
IC113 D 4011
IC117 A 4025
IC110A 4027
IC111 A 4011
IC111 C 4011
IC114 A 4584
IC111 D 4011
IC115 4060
IC109 4040
12-BIT BIN COUNTER
IC112 D 4011
IC110B 4027
IC112 C 4011
IC114 F 4584
IC114 E 4584
IC114 C 4584
IC114 D 4584
IC107 B 4538
MONOSTABLE MULTIVIBRATOR
IC108 4066
IC106 A 4066
IC112 B 4011
IC102 A HA17903
IC103 B HA17903
IC103 A HA17903
FF1
FF2
C103 2200p
R113 49.9k
R121 1.00K
R119 2.00K
R122 2.00K
R153 1.00K
R155 1.00K
R114 1M
C104 0.33u
D103 HSK120
C106 220p
D104 HSK120
R115 150k
C105 10u/35V
R116 0.90k
R149 1.00K
R150 1.00K
R151 1.00K
R152 1.00K
R154 1.00K
R157 30.1K
R156 100K
Q108 2SC2618
R145 24.9k
R146 24.9k
R147 24.9k
R127 1.5k
Q101 2SC4101
R148 100K
R125 2.00k
R136 301k
D100 HSK120
Q106 2SD1950
R120 3.32
Q107 2SD1950
R118 60.4k
R117 20.0k
R129 100k
R128 100k
R132 100k
RY101 G6A-274P
C120 470u/16V
R124 3.01k
Q104 2SD1950
R123 2.00k
Q102 2SC2618
R130 49.9k
R131 49.9k
R133 24.9k
Q105 2SD1950
Q103 2SD1950
R126 0.56
R135 499
C108 0.33u
C110 10u/35V
D106 HSK120
R134 24.9k
D109 HSK120
D107 HSK120
CNJ103
M60-09-30-114P

12. CIRCUIT DIAGRAM



0203 - 024759
UP - 0630
Sub 1/1
1992 - 6 - 4
日本光電
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
TRACE
REVISION
REASON
CHK
FILE: UP-0630
4-Jun-92 16:27:42
CN104 FSN-21.5A-9
16msec
0msec
HAOUT
SAFETY
+8V
E1
-8V
INST
ADULT/XNEONATUS
IC209 uPC811
R221 49.9
R220 10.0k
C213 220p
C211 0.1u
C212 0.1u
R222 60.4k
R223 100k
R219 10.0k
IC208 4051
TP3
TP4
TP5
PULSE
PRES
IC205 A uPC4062
C203 0.01u
R209 150k
C204 0.01u
R208 150k
R206 60.1k
R207 60.1k
IC203 LT1001
IC204 LT1001
R204 24.9k
R205 24.9k
R203 1.27k
GAIN ADJ
VR202 1.0k
TP1
TP2
R226 10.0k
R227 10.0k
VR201 200
T201 FPM-07PG-NK2
IC202 LT1001
R201 4.99k
R202 2.49K
IC201 LT1009S8
C202 10u/35V
C201 0.1u
IC206 B uPC4062
C206 0.1u
R210 301k
C205 0.047u
R211 301k
C210 0.01u
R218 100k
IC206 A uPC4062
R217 100k
R216 1.00M
IC207 4066
R225 1.00k
C209 0.33u
R215 30.1k
C208 0.01u
R214 150k
IC205 B uPC4062
R213 2.49k
R224 100k
C207 0.33u
R212 1.00M
AGND

Section 13 PARTS LOCATION GUIDE

13-1 Main Unit, MU-881R

- 13-1-1 MOTHER Board, UP-0798 .... 13.1
- 13-1-2 COM3 Board, UP-0563 .... 13.3
- 13-1-3 CRTC Board, UP-0795 .... 13.4
- 13-1-4 I/O Board, UP-0797 .... 13.6
- 13-1-5 MEMORY CARD Board, UP-0799 .... 13.7
- 13-1-6 CONNECTOR Board, UP-0807 .... 13.9
- 13-1-7 DPU Board, UP-0670 .... 13.10
- 13-1-8 CPU Board, UR-3027 .... 13.11
- 13-1-9 Regulator Board, UP-0813 .... 13.12

13-2 Keypad, RY-881PA

- 13-2-1 OPERATION Board, UR-3025 .... 13.13

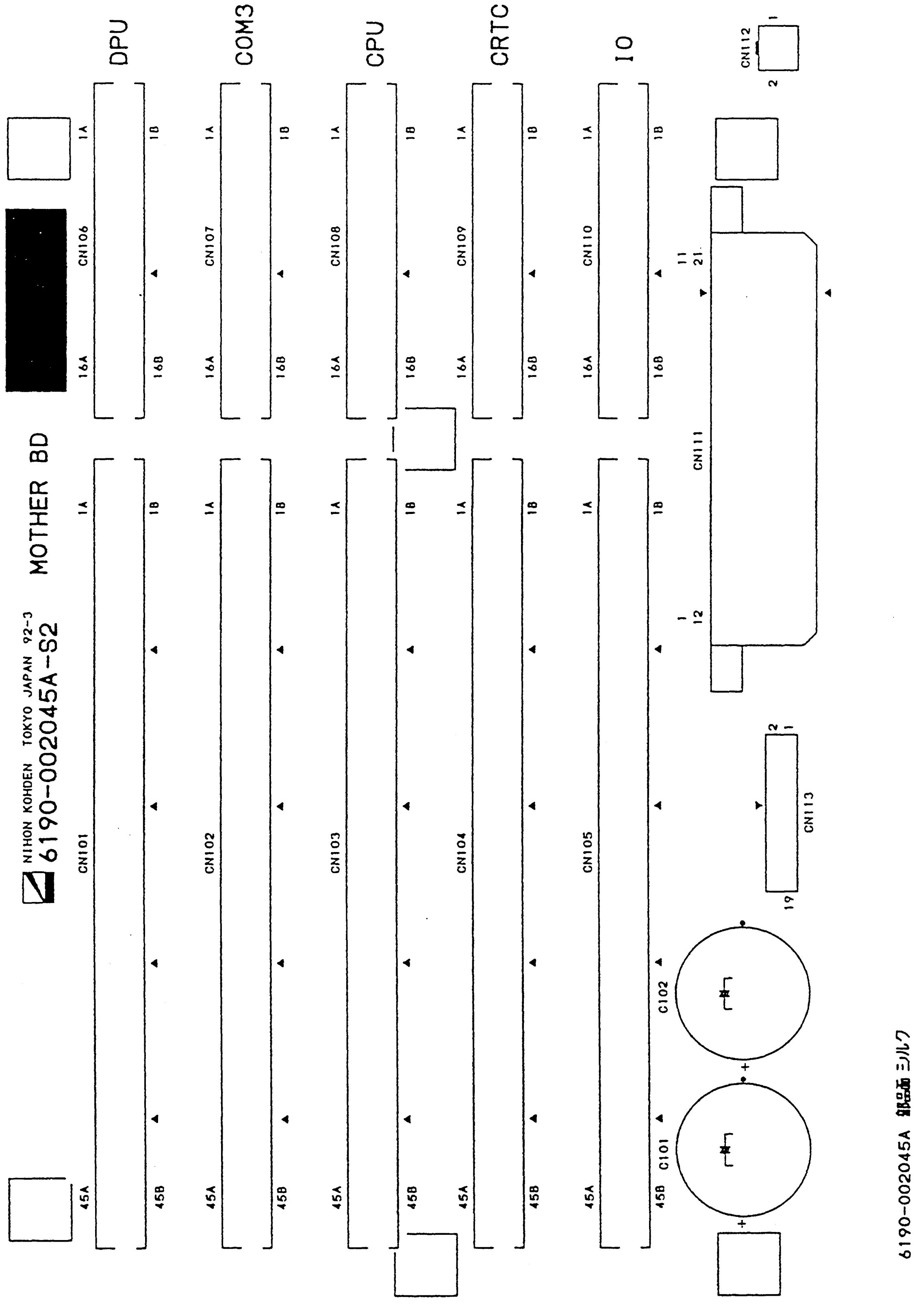
13-3 Head Amplifiers

- 13-3-1 ECG Head Amp (AC-800P) Board, UP-0272 .... 13.14
- 13-3-2 PRESS Head Amp (AP-800PA) Board, UP-0369 .... 13.14
- 13-3-3 CO Head Amp (AH-800PA) Board, UP-0318 .... 13.15
- 13-3-4 TEMP Head Amp (AW-800PA) Board, UP-0319 .... 13.15
- 13-3-5 RESPIRATION Head Amp (AR-800PA) Board, UP-0548 .... 13.16
- 13-3-6 SpO$_2$ Head Amp (AL-800PA) Main Board, UP-0551 .... 13.17
- 13-3-7 SpO$_2$ Head Amp (AL-800PA) Sub Board, UP-0552 .... 13.17
- 13-3-8 EEG Head Amp (AE-800PA) Main Board, UP-0421 .... 13.18
- 13-3-9 EEG Head Amp (AE-800PA) Sub Board, UP-0422 .... 13.18
- 13-3-10 CO$_2$ Head Amp (AG-800PA) Main Board, UP-0588 .... 13.19
- 13-3-11 CO$_2$ Head Amp (AG-800PA) Sub Board, UP-0589 .... 13.19
- 13-3-12 O$_2$ Head Amp (AG-820PA) Board, UP-0592 .... 13.20
- 13-3-13 NIBP Head Amp (AP-860PA) Main Board, UP-0629 and Sub Board, UP-0630 .... 13.25

13-4 Display Unit, VD-881R

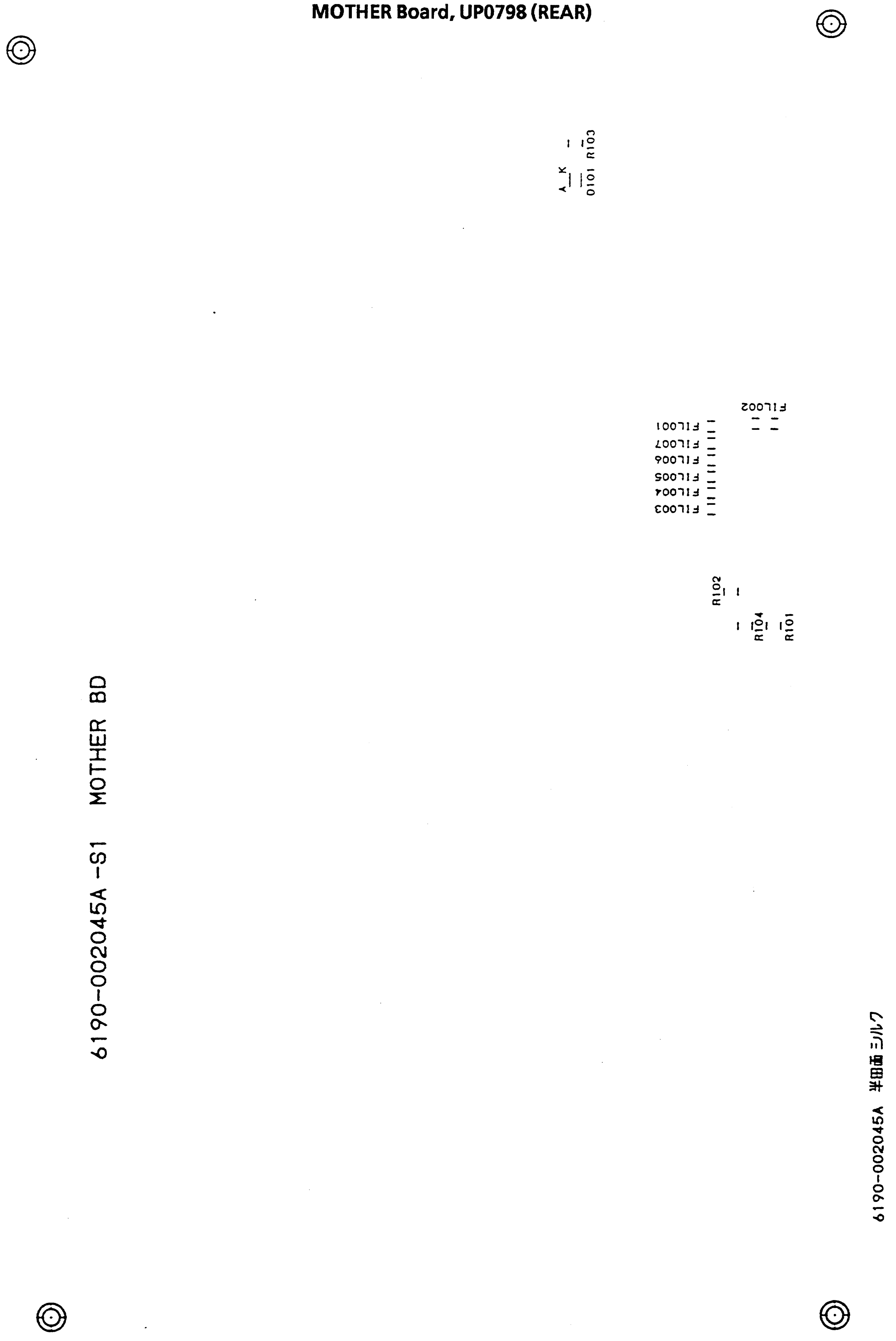
- 13-4-1 OPERATION CONTROL Board, UP-0801 .... 13.21
- 13-4-2 OPERATION (VR) Board, UP-0802 .... 13.23
- 13-4-3 LED Board, UP-0806 .... 13.23
- 13-4-4 Power Supply Unit, SC-019R 13.24

MOTHER Board, UP0798 (FRONT)

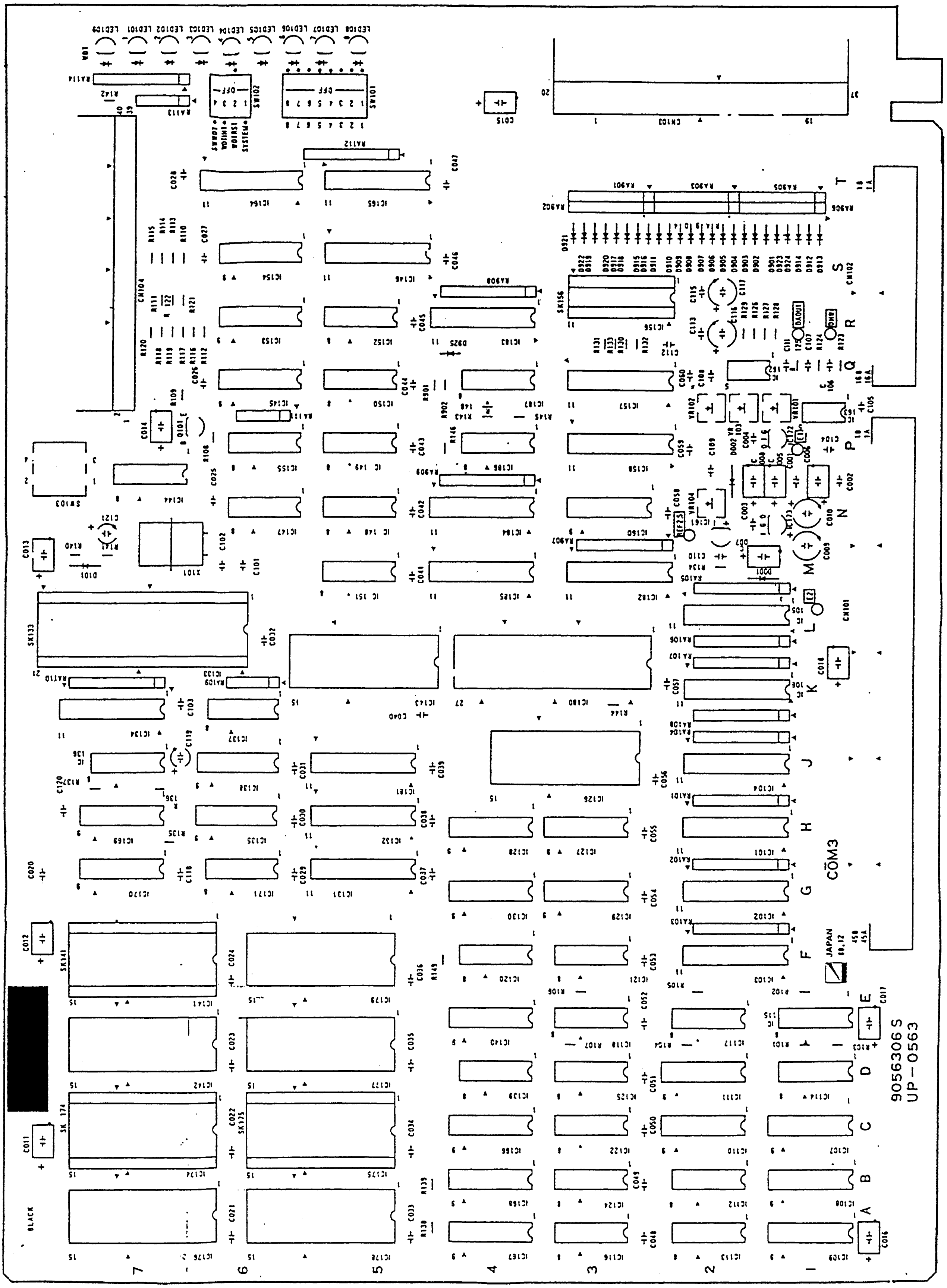

DPU
COM3
CPU
CRTC
IO
MOTHER BD
NIHON KOHDEN TOKYO JAPAN 92-3
6190-002045A-S2
CN101
CN102
CN103
CN104
CN105
CN106
CN107
CN108
CN109
CN110
CN111
CN112
CN113
C101
C102
1A
1B
16A
16B
45A
45B
1
2
11
12
21
19
+
6190-002045A 部品面 シルク

13. PARTS LOCATION GUIDE

MOTHER Board, UP0798 (REAR)

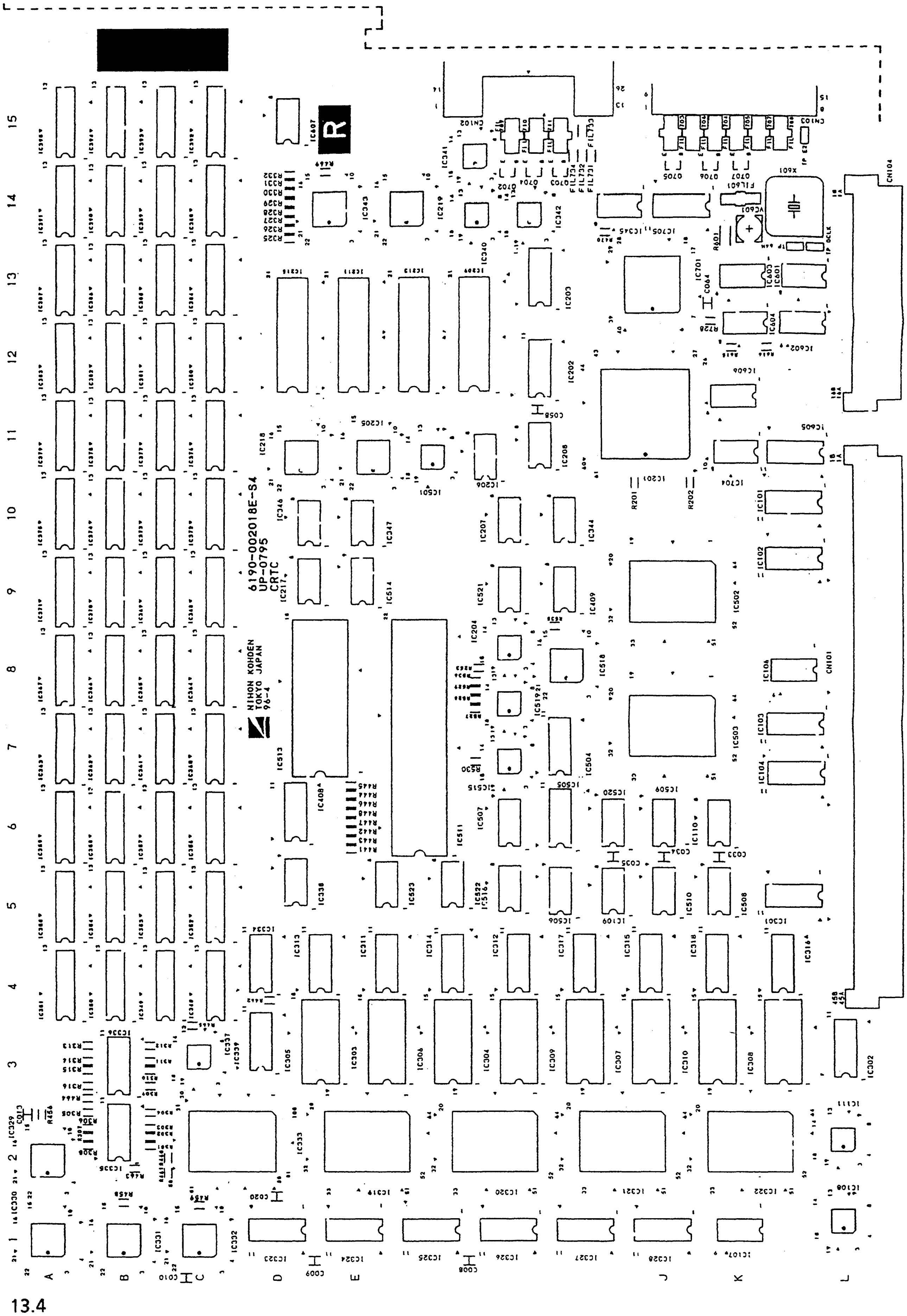

A K
D101
R103
FIL002
FIL001
FIL007
FIL006
FIL005
FIL004
FIL003
R102
R104
R101
6190-002045A -S1 MOTHER BD
6190-002045A 半田面シルク

COM3 Board, UP-0563

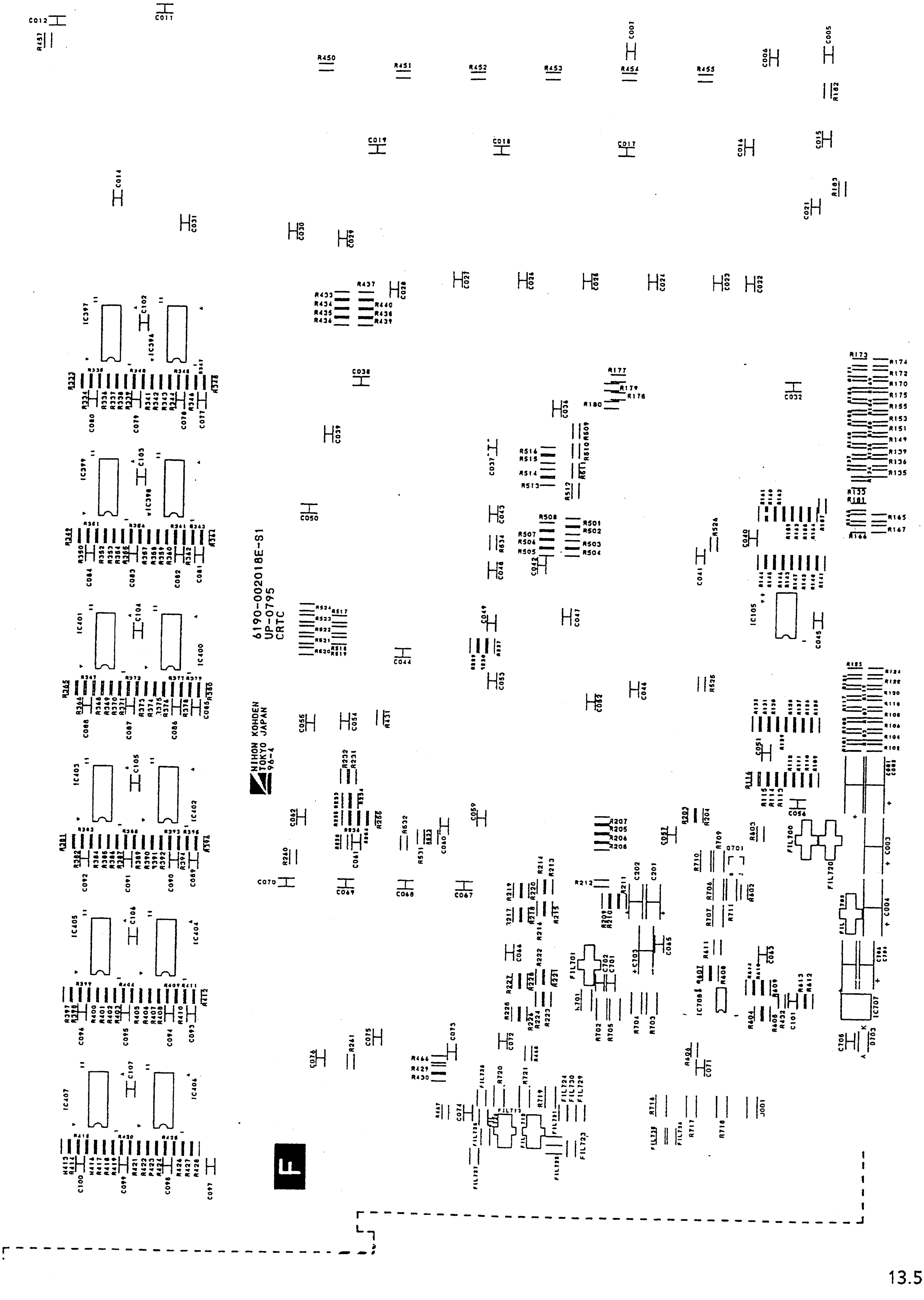

A
B
C
D
E
F
G
H
J
K
L
M
N
P
Q
R
S
T
1
2
3
4
5
6
7
COM3
JAPAN
BLACK
9056306 S
UP-0563

13. PARTS LOCATION GUIDE

CRTC Board, UP-0795 (FRONT)

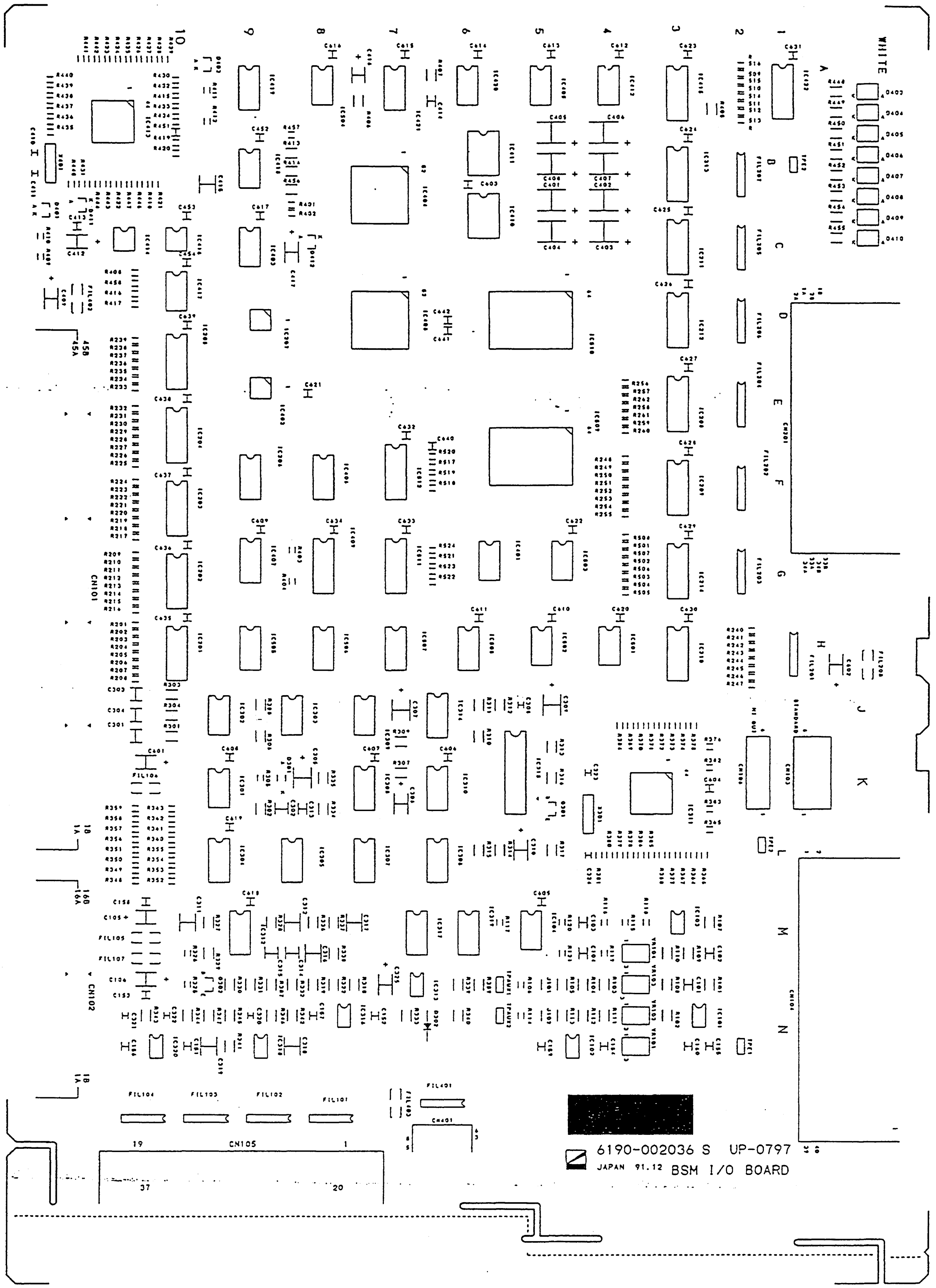

R
6190-002018E-S4
UP-0795
CRTC
NIHON KOHDEN
TOKYO JAPAN
96-4
CN101
CN102
CN103
CN104
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
A
B
C
D
E
F
G
H
J
K
L

CRTC Board, UP-0795 (REAR)


6190-002018E-S1
UP-0795
CRTC
NIHON KOHDEN
TOKYO
JAPAN
96-4
F
IC397
IC399
IC401
IC403
IC405
IC407
IC105
IC707
FIL700
FIL720
FIL701
J001

13. PARTS LOCATION GUIDE

I/O Board, UP-0797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9
8
7
6
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4
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2
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WHITE
A
B
C
D
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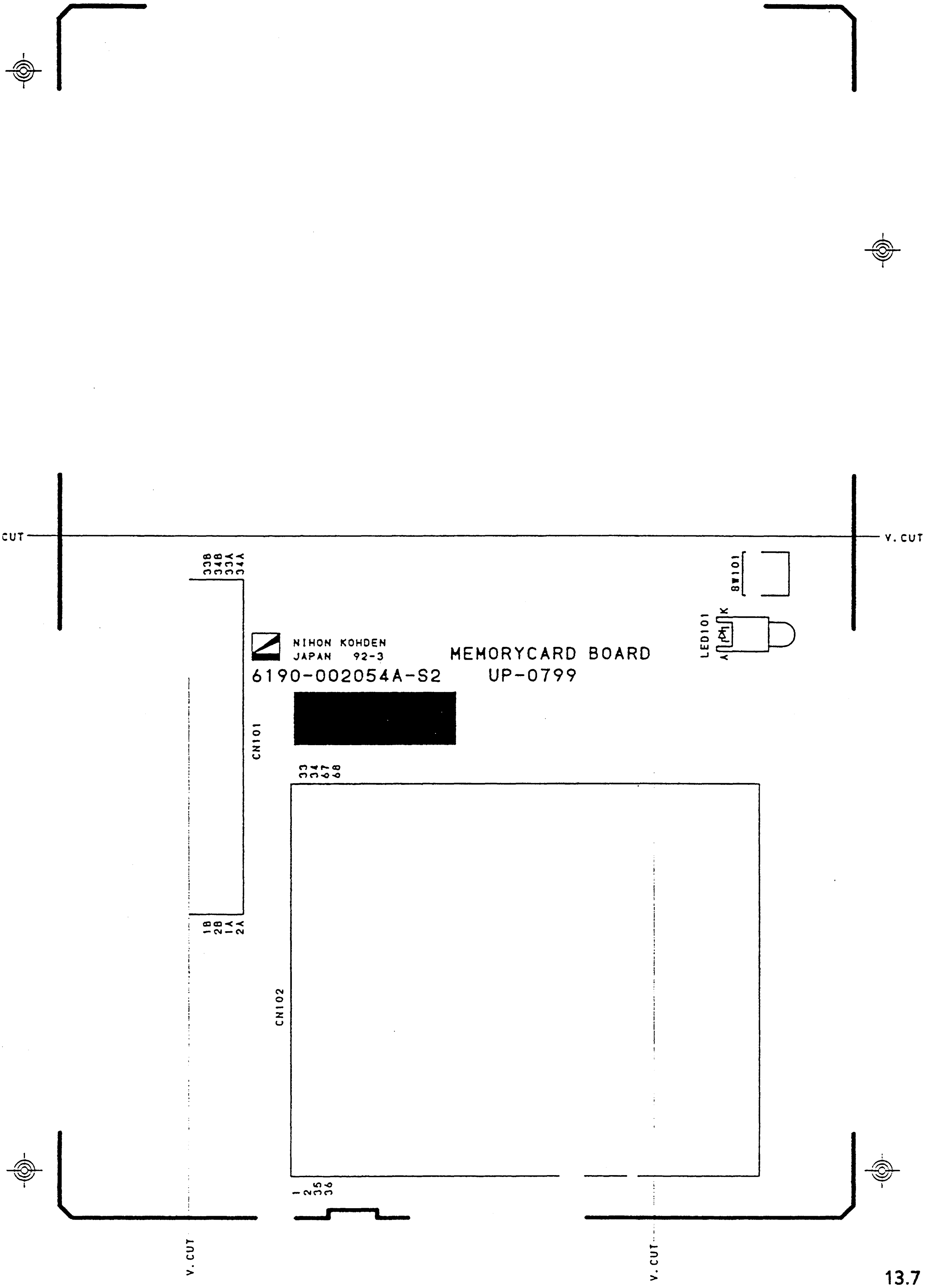
F
G
H
J
K
L
M
N
CN101
CN102
CN105
19
1
37
20
FIL104
FIL103
FIL102
FIL101
FIL401
CN401
6190-002036 S4/L1
6190-002036 S UP-0797
JAPAN 91.12 BSM I/O BOARD

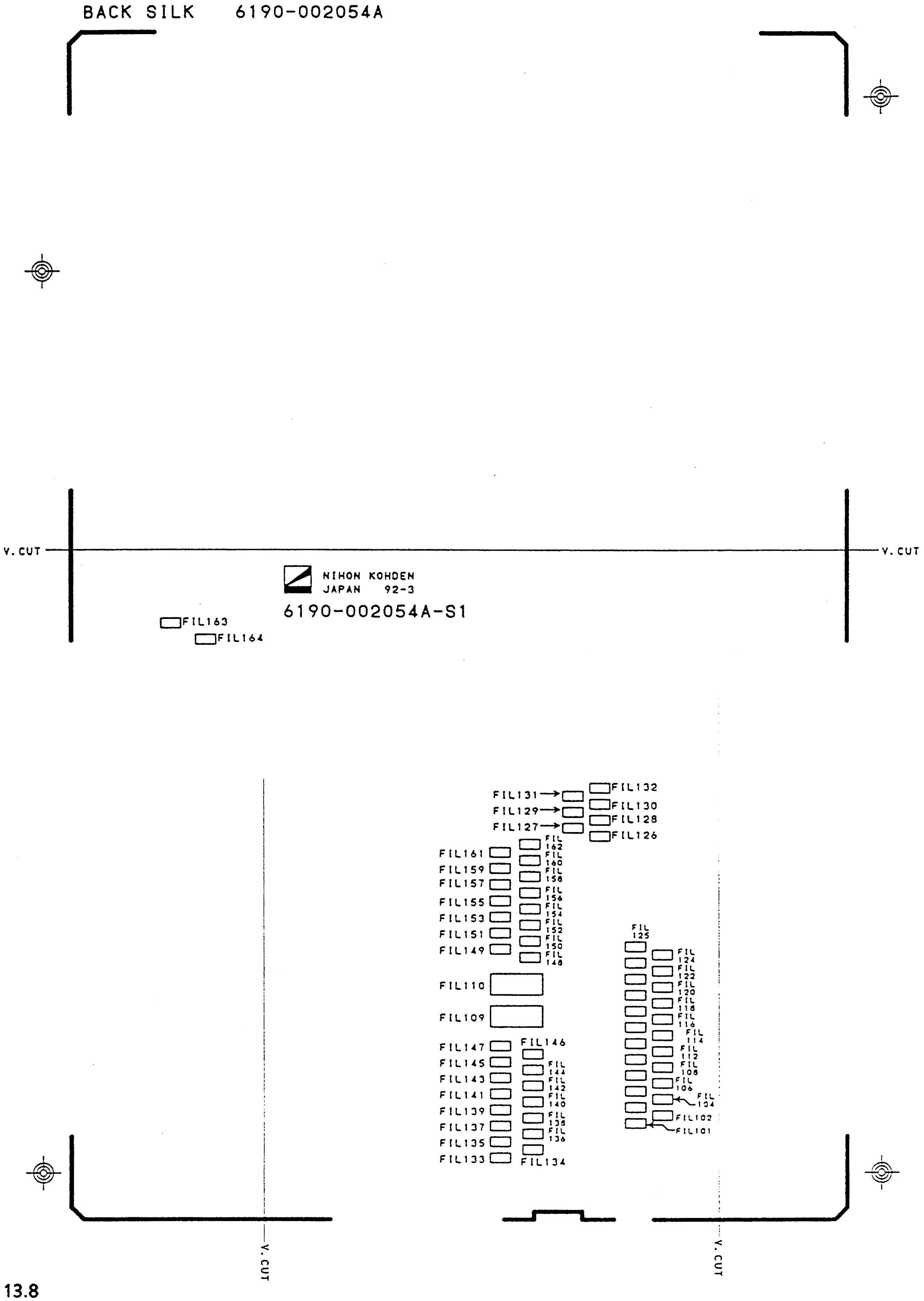
MEMORY CARD Board, UP-0799 (FRONT)

FRONT SILK 6190-002054A

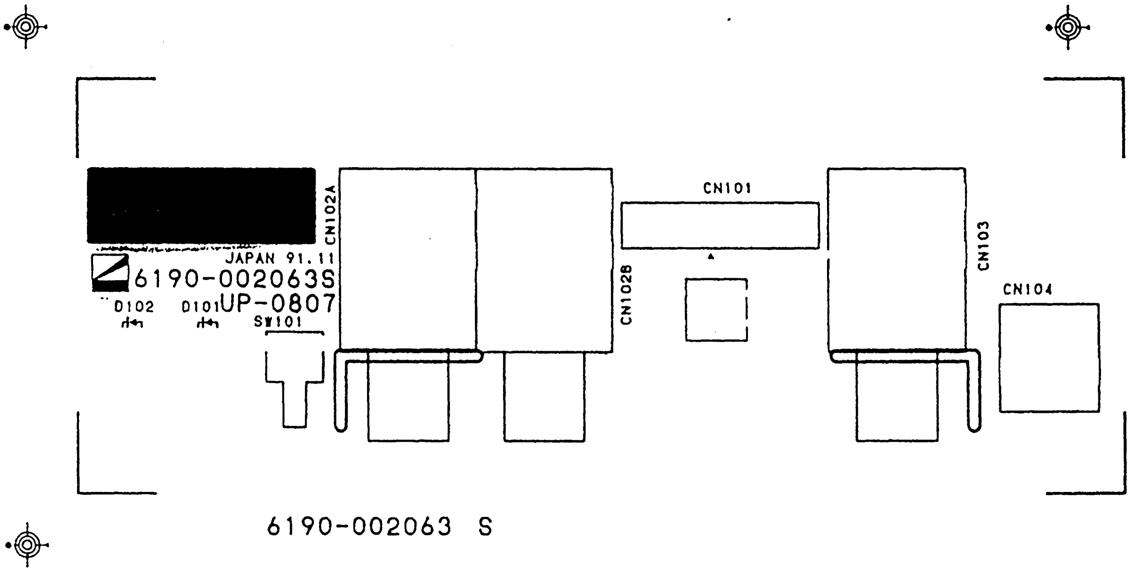

CUT
V.CUT
33B
34B
33A
34A
CN101
1B
2B
1A
2A
NIHON KOHDEN
JAPAN 92-3
6190-002054A-S2
MEMORYCARD BOARD
UP-0799
SW101
LED101
K
A
33
34
67
68
CN102
1
2
35
36
V.CUT
V.CUT

13. PARTS LOCATION GUIDE

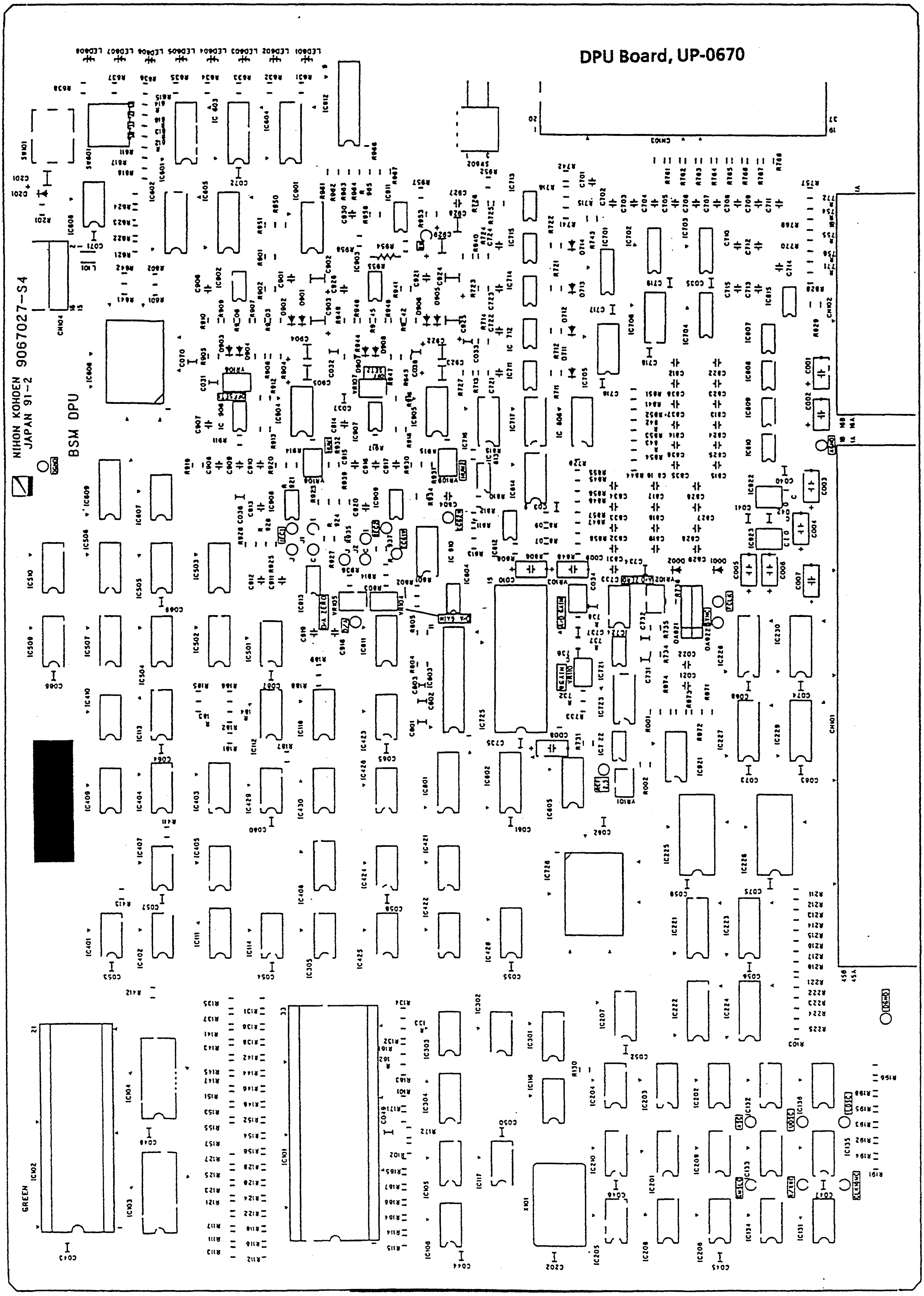
MEMORY CARD Board, UP-0799 (REAR)


BACK SILK 6190-002054A
V.CUT
V.CUT
NIHON KOHDEN
JAPAN 92-3
6190-002054A-S1
FIL163
FIL164
FIL131
FIL132
FIL129
FIL130
FIL127
FIL128
FIL126
FIL162
FIL161
FIL160
FIL159
FIL158
FIL157
FIL156
FIL155
FIL154
FIL153
FIL152
FIL151
FIL150
FIL149
FIL148
FIL125
FIL124
FIL122
FIL120
FIL118
FIL116
FIL114
FIL112
FIL108
FIL106
FIL104
FIL102
FIL101
FIL110
FIL109
FIL147
FIL146
FIL145
FIL144
FIL143
FIL142
FIL141
FIL140
FIL139
FIL138
FIL137
FIL136
FIL135
FIL133
FIL134
V.CUT
V.CUT

FRONT CONNECTOR Board, UP-0807

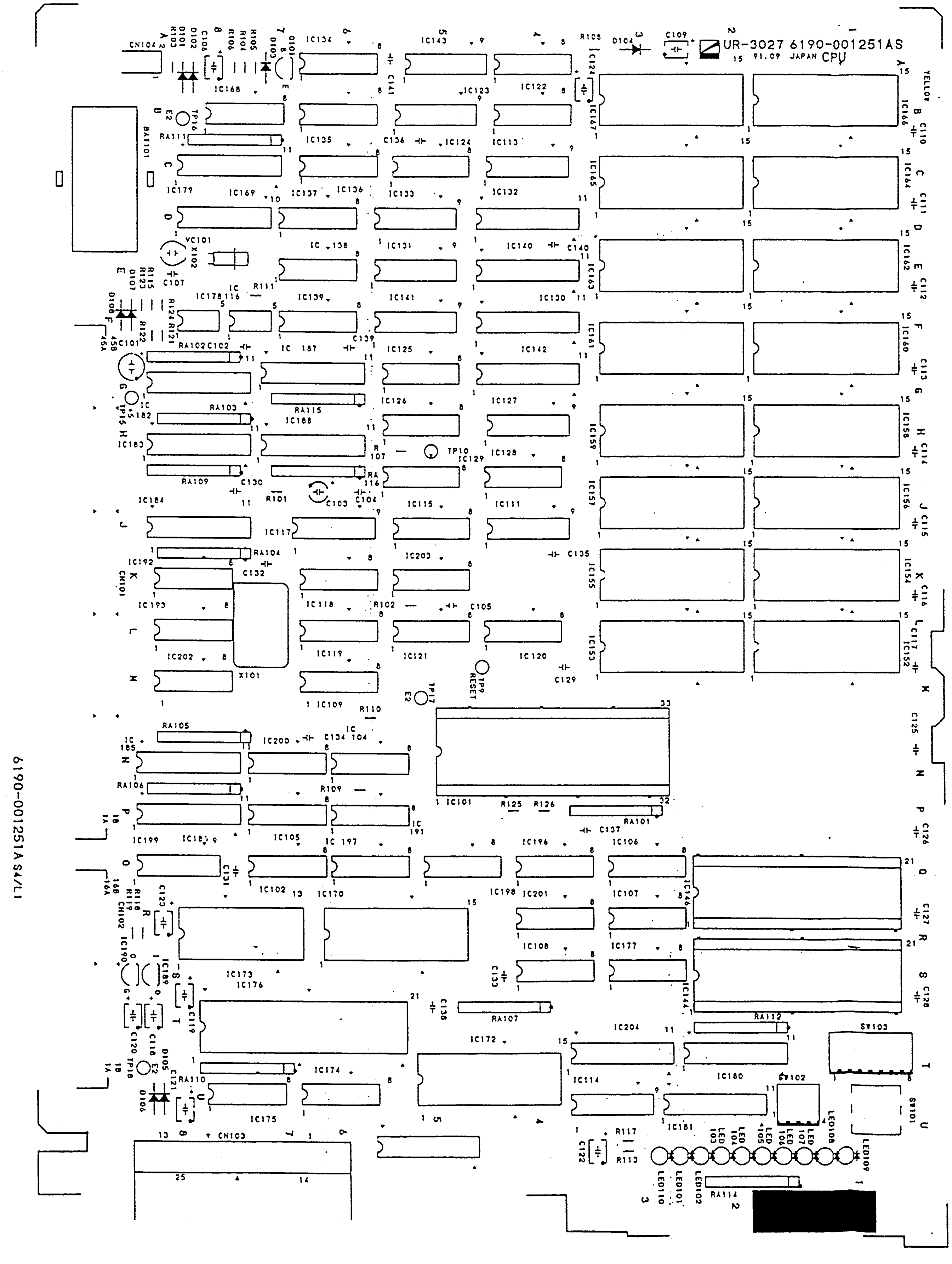

CN102A
CN101
CN103
JAPAN 91.11
6190-002063S
CN102B
CN104
D102
D101
UP-0807
SW101
6190-002063 S

13. PARTS LOCATION GUIDE


DPU Board, UP-0670

NIHON KOHDEN 9067027-S4
JAPAN 91-2
BSM DPU
GREEN
CN103
CN101
CN102
CN104
IC101
IC102
IC725
IC726
IC225
IC226
X101

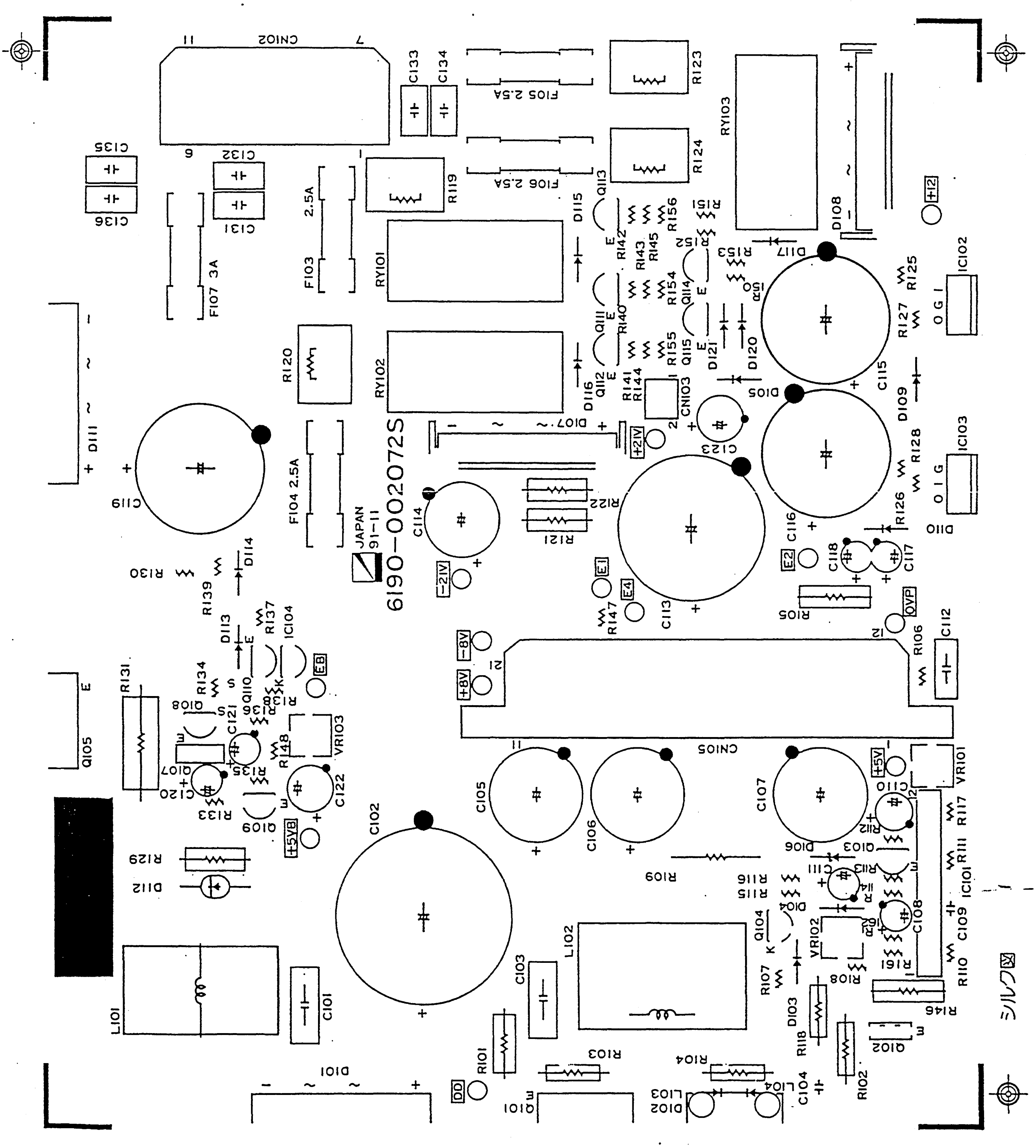
CPU Board, UR-3027


UR-3027 6190-001251AS
15 91.09 JAPAN CPU
YELLOW
CN104
CN101
CN102
CN103
BAT101
X101
X102
VC101
TP16
TP15
TP10
TP9 RESET
TP17
TP18
IC101
IC172
IC173
IC176
IC146
IC144
SW101
SW102
SW103
LED101
LED102
LED103
LED104
LED105
LED106
LED107
LED108
LED109
LED110
RA101
RA107
RA112
RA114
6190-001251A S4/L1

[redacted]

13. PARTS LOCATION GUIDE

Regulator Board, UP-0813


CN102
CN103
CN105
RY101
RY102
RY103
F103 2.5A
F104 2.5A
F105 2.5A
F106 2.5A
F107 3A
C101
C102
C103
C104
C105
C106
C107
C108
C109
C110
C111
C112
C113
C114
C115
C116
C117
C118
C119
C120
C121
C122
C123
C131
C132
C133
C134
C135
C136
D101
D102
D103
D104
D105
D106
D107
D108
D109
D110
D111
D112
D113
D114
D115
D116
D117
D120
D121
Q101
Q102
Q103
Q104
Q105
Q107
Q108
Q109
Q110
Q111
Q112
Q113
Q114
Q115
IC101
IC102
IC103
IC104
L101
L102
L103
L104
VR101
VR102
VR103
R101
R102
R103
R104
R105
R106
R107
R108
R109
R110
R111
R112
R113
R114
R115
R116
R117
R118
R119
R120
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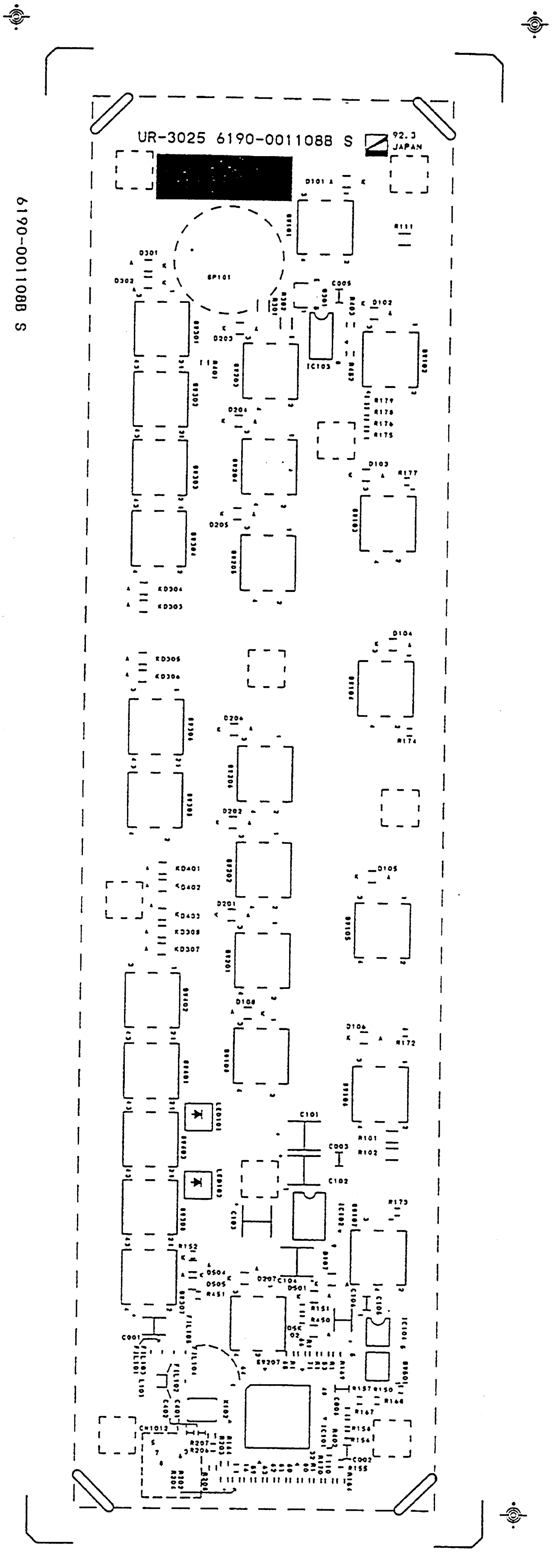
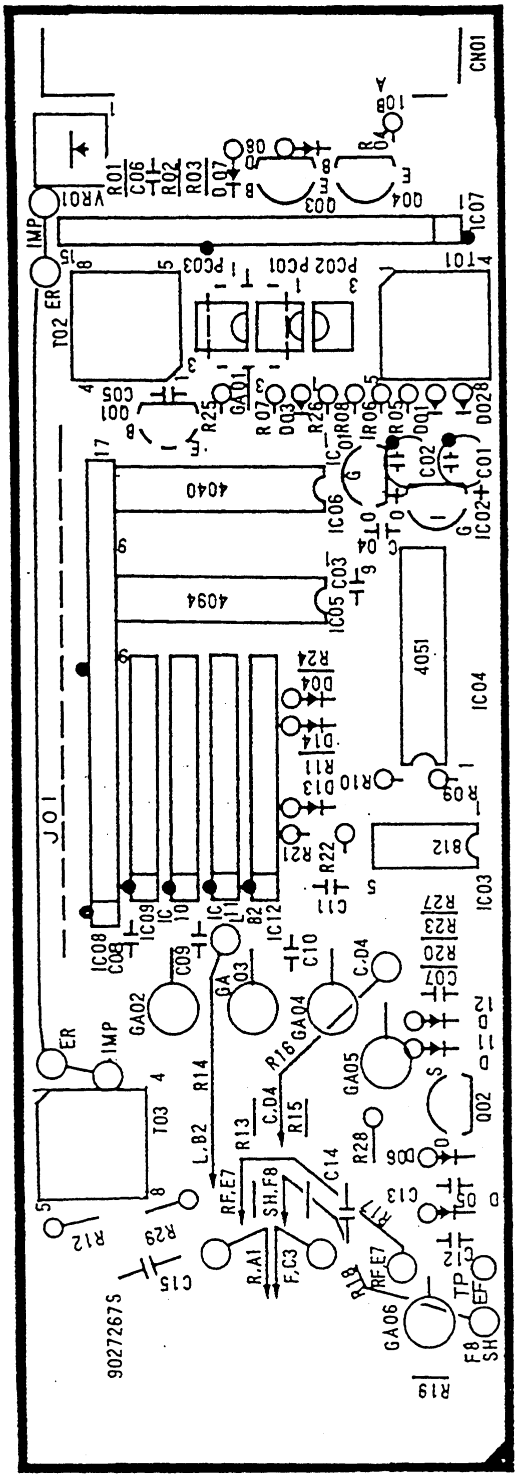
R122
R123
R124
R125
R126
R127
R128
R129
R130
R131
R133
R134
R135
R136
R137
R139
R140
R141
R142
R143
R144
R145
R146
R147
R148
R151
R152
R153
R154
R155
R156
R161
+12
+21V
-21V
+8V
-8V
+5V
+5VB
E1
E2
E4
EB
OVP
DD
JAPAN 91-11
6190-002072S
シルク図

OPERATION Board, UR-3025

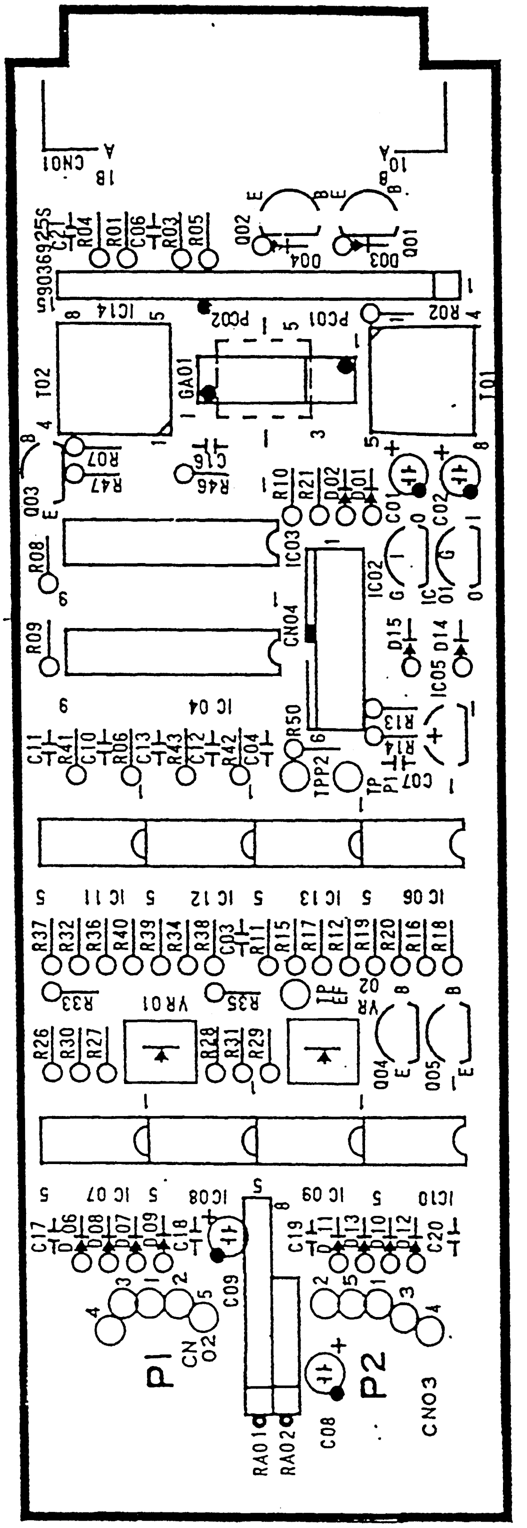

UR-3025 6190-0011088 S
92.3
JAPAN
6190-001108B S
SP101
D101
D102
D103
D104
D105
D106
D108
D201
D202
D203
D204
D205
D206
D301
D302
R111
R177
R174
R172
R173
R101
R102
R152
R151
R450
R451
IC103
C005
C101
C102
C003
C104
C001
C002
CN1012
EV207
R157
R150
R167
R156
R154
R155
R206
R207
D504
D505
D501
D207

13. PARTS LOCATION GUIDE

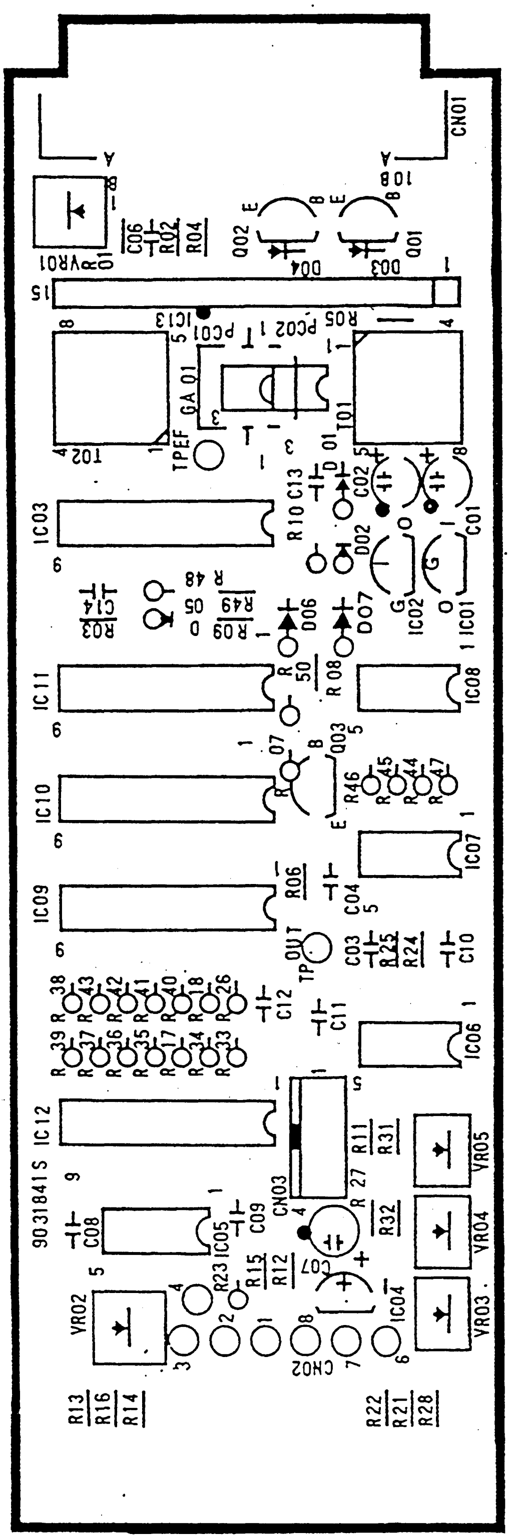
ECG Head Amp (AC-800P) Board, UP-0272


CN01
VR01
IMP
ER
T01
T02
T03
IC07
PC01
PC02
PC03
GA01
IC06
4040
IC05
4094
4051
IC04
812
IC03
IC08
IC09
IC10
IC11
IC12
J01
GA02
GA03
GA04
GA05
GA06
R19
90272675

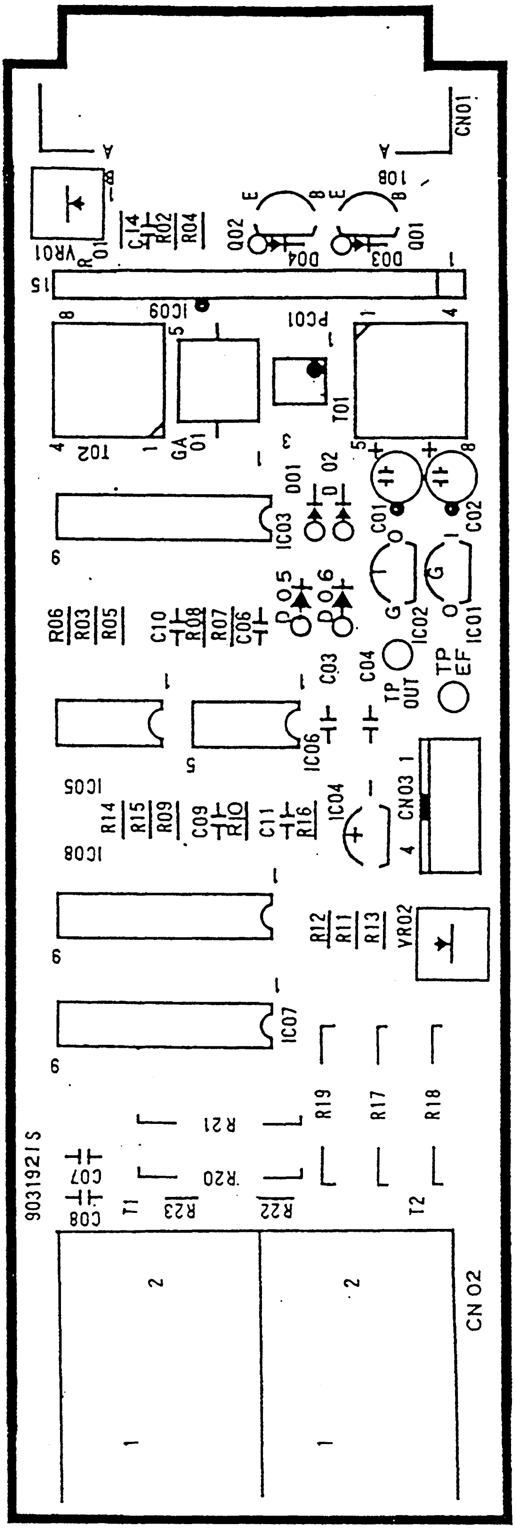
PRESS Head Amp (AP-800PA) Board, UP-0369


CN01
90369255
IC14
PC01
PC02
GA01
T01
T02
IC03
IC02
CN04
IC04
IC05
IC06
IC13
IC12
IC11
VR01
VR02
IC07
IC08
IC09
IC10
P1
P2
CN02
CN03
RA01
RA02
C08
C09

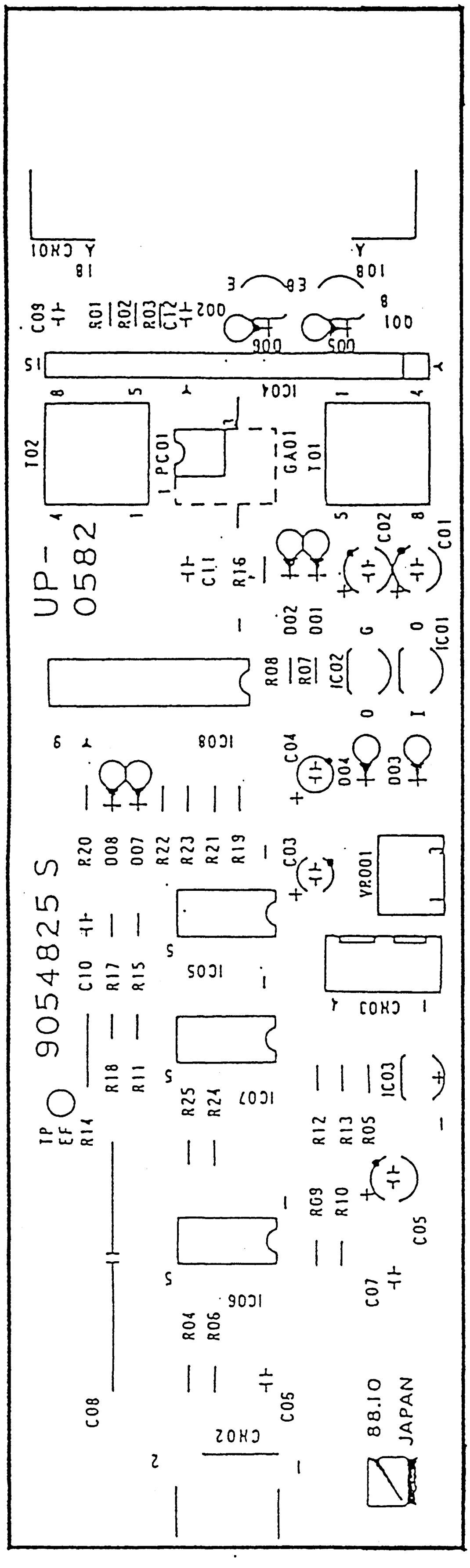
CO Head Amp (AH-800PA) Board, UP-0318


CN01
VR01
Q01
Q02
D03
D04
C06
R02
R04
IC13
PC01
PC02
R05
GA 01
T01
T02
TPEF
R10
C13
D01
C02
C01
D02
IC03
C14
R03
R48
R49
Q5
R09
D06
D07
IC02
IC01
IC11
R50
R08
IC08
Q03
R45
R44
R47
R46
IC10
IC07
IC09
R06
C04
TP OUT
C03
R25
R24
C10
R38
R43
R42
R41
R40
R18
R26
R39
R37
R36
R35
R17
R34
R33
C12
C11
IC06
IC12
CN03
R11
R31
VR05
R27
R32
VR04
9031841S
C08
IC05
C09
R23
R15
R12
C07
IC04
VR03
VR02
CN02
R13
R16
R14
R22
R21
R28

TEMP Head Amp (AW-800PA) Board, UP-0319


CN01
VR01
C14
R02
R04
Q02
Q01
D04
D03
IC09
PC01
GA 01
T01
T02
IC03
D01
D02
C01
C02
R06
R03
R05
C10
R08
R07
C06
Q5
Q6
IC02
IC01
TP OUT
TP EF
C03
C04
IC06
IC05
R14
R15
R09
C09
R10
C11
R16
IC04
CN03
IC08
R12
R11
R13
VR02
IC07
R19
R17
R18
R21
R20
9031921S
C07
C08
T1
R23
R22
T2
CN 02

RESPIRATION Head Amp (AR-800PA) Board, UP-0548


CN01
CN02
CN03
C01
C02
C03
C04
C05
C07
C08
C09
C10
C11
C12
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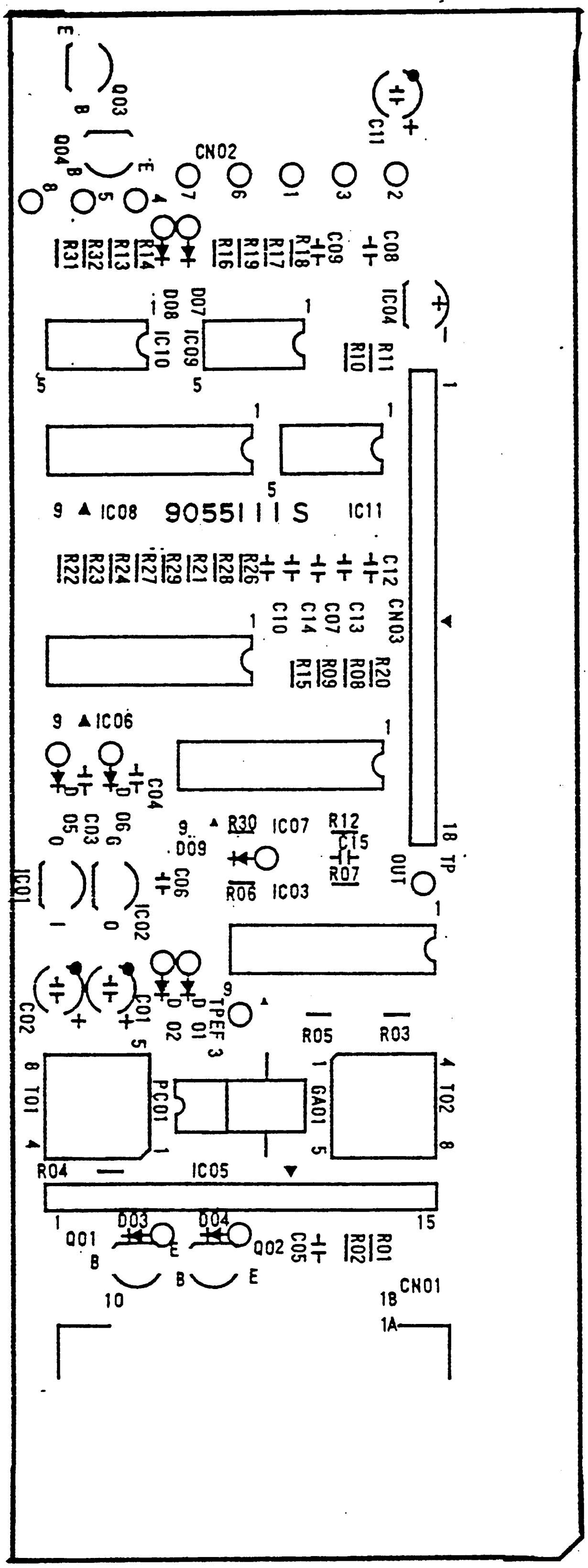
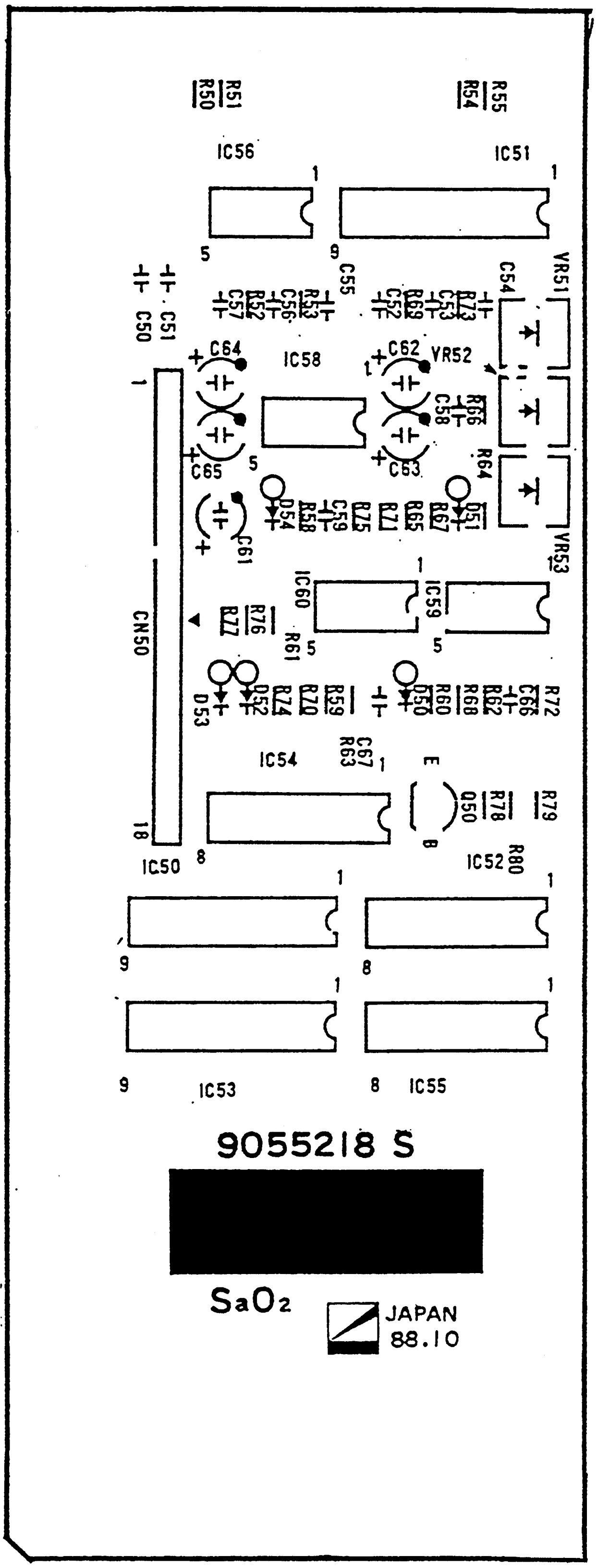
R02
R03
R04
R05
R06
R07
R08
R09
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
D01
D02
D03
D04
D05
D06
D07
D08
IC01
IC02
IC03
IC04
IC05
IC06
IC07
IC08
T01
T02
PC01
GA01
VR001
TP EF
UP-0582
9054825 S
88.10 JAPAN

SpO$_2$ Head Amp (AL-800PA) Main Board, UP-0551

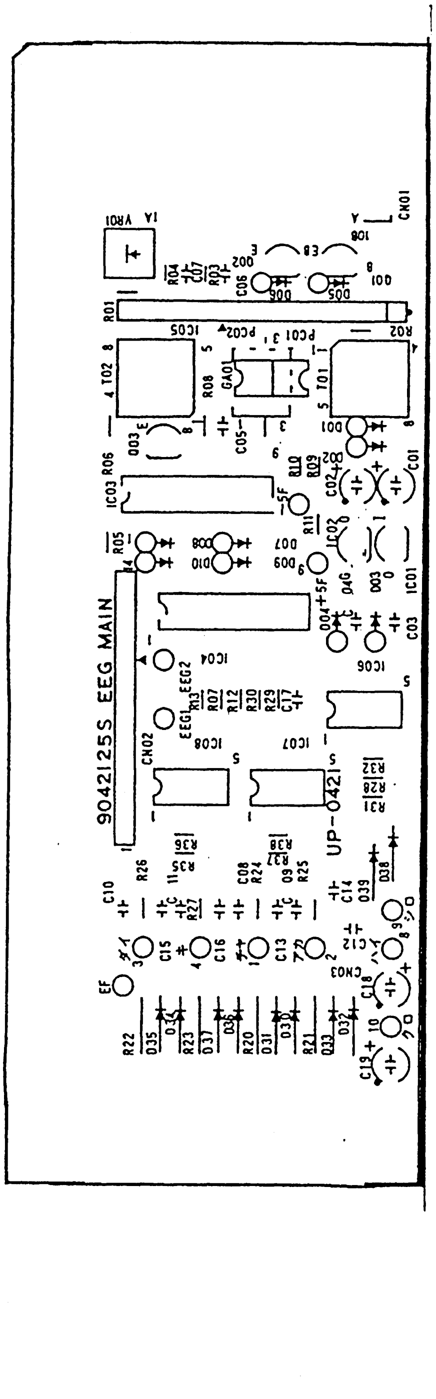

CN02
IC10
IC09
IC04
IC08
9055111 S
IC11
CN03
IC06
IC07
IC03
IC01
IC02
TP
OUT
R05
R03
T01
PC01
GA01
T02
IC05
Q01
D03
D04
Q02
CN01

SpO$_2$ Head Amp (AL-800PA) Sub Board, UP-0552


IC56
IC51
VR51
IC58
VR52
VR53
CN50
IC60
IC59
IC54
Q50
IC50
IC52
IC53
IC55
9055218 S
SaO2
JAPAN
88.10

13. PARTS LOCATION GUIDE

EEG Head Amp (AE-800PA) Main Board, UP0421


9042125S EEG MAIN
UP-0421
CN01
CN02
CN03
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T01
T02
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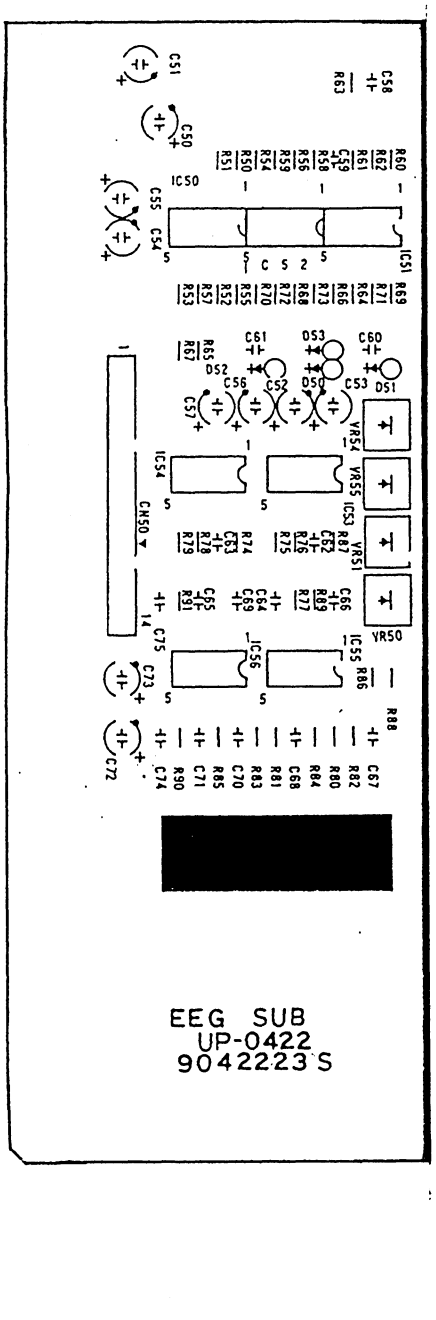
IC02
IC03
IC04
IC05
IC06
IC07
IC08

EEG Head Amp (AE-800PA) Sub Board, UP0422


EEG SUB
UP-0422
9042223S
CN50
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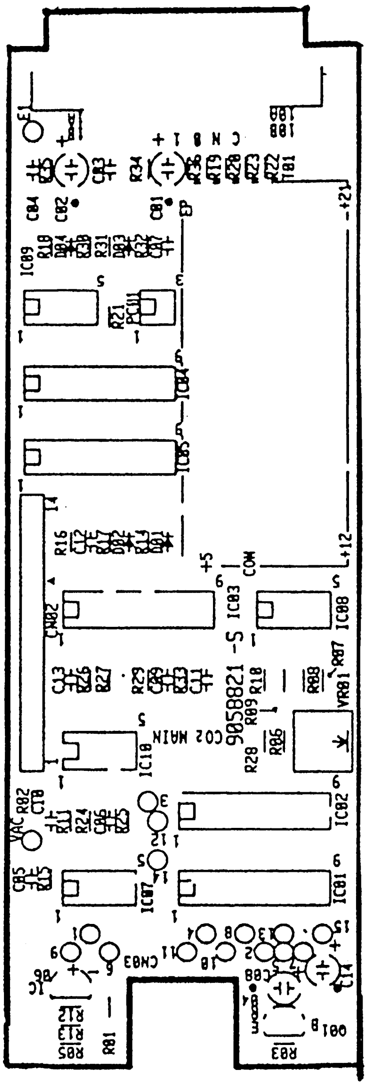
IC51
IC52
IC53
IC54
IC55
IC56
VR50
VR51
VR54
VR55

CO_2 Head Amp (AG-800PA) Main Board, UP-0588


CO2 MAIN
9058821-S
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IC02
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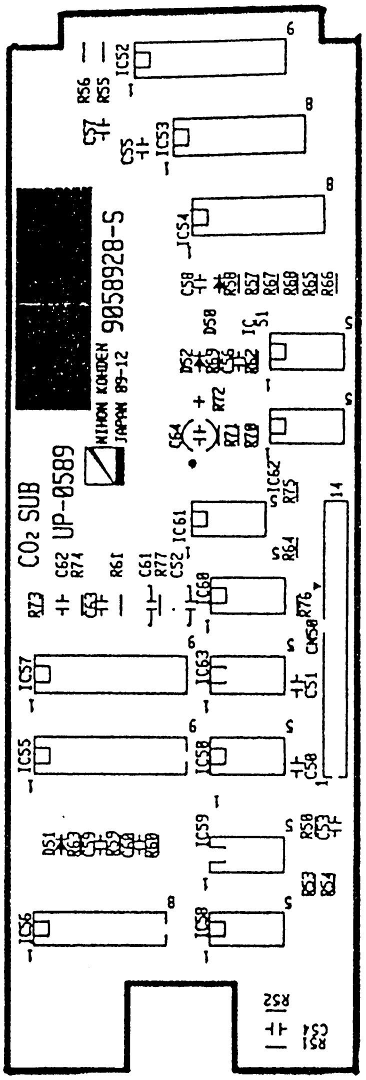
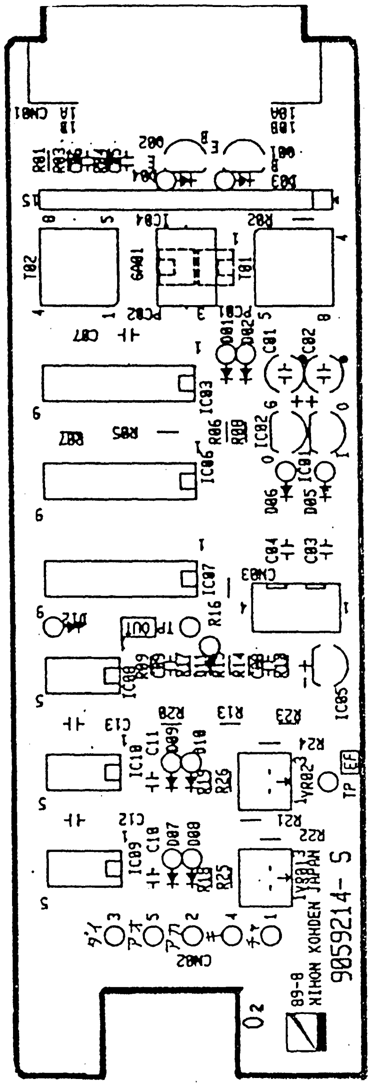
IC04
IC05
IC07
IC08
IC09
IC10
CN02
CN03
VR01
+12
+21
+5
COM
VAC

CO_2 Head Amp (AG-800PA) Sub Board, UP-0589


CO2 SUB
UP-0589
9058928-S
NIHON KOHDEN
JAPAN 89-12
IC52
IC53
IC54
IC55
IC56
IC57
IC58
IC59
IC60
IC61
IC62
IC63
CN50

13. PARTS LOCATION GUIDE

O_2 Head Amp (AG-820PA) Board, UP-0592


CN01
1A
1B
10A
10B
Q01
Q02
D01
D02
D03
D04
D05
D06
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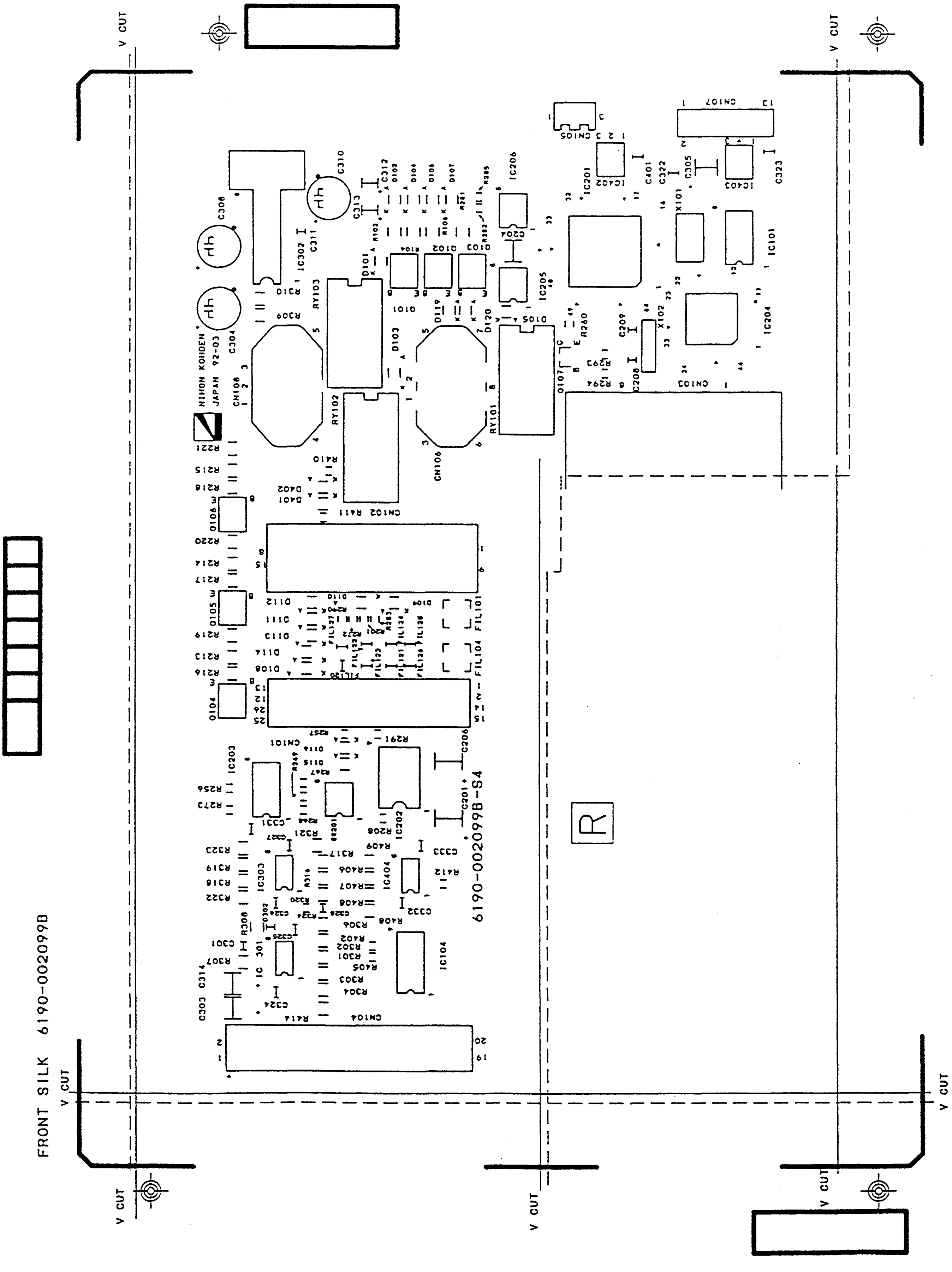
D10
D11
D12
T01
T02
IC01
IC02
IC03
IC04
IC05
IC06
IC07
IC08
IC09
IC10
PC01
PC02
GA01
CN02
CN03
C01
C02
C03
C04
C07
C08
C10
C11
C12
C13
R01
R02
R03
R05
R06
R07
R10
R13
R14
R16
R21
R22
R23
R24
R25
R26
R28
VR01
VR02
TP EF
TP OUT
9059214-5
NIHON KOHDEN JAPAN
89-8
O_2

OPERATION CONTROL Board, UP-0801 (FRONT)


V CUT
FRONT SILK 6190-002099B
6190-002099B-S4
NIHON KOHDEN JAPAN 92-03
CN101
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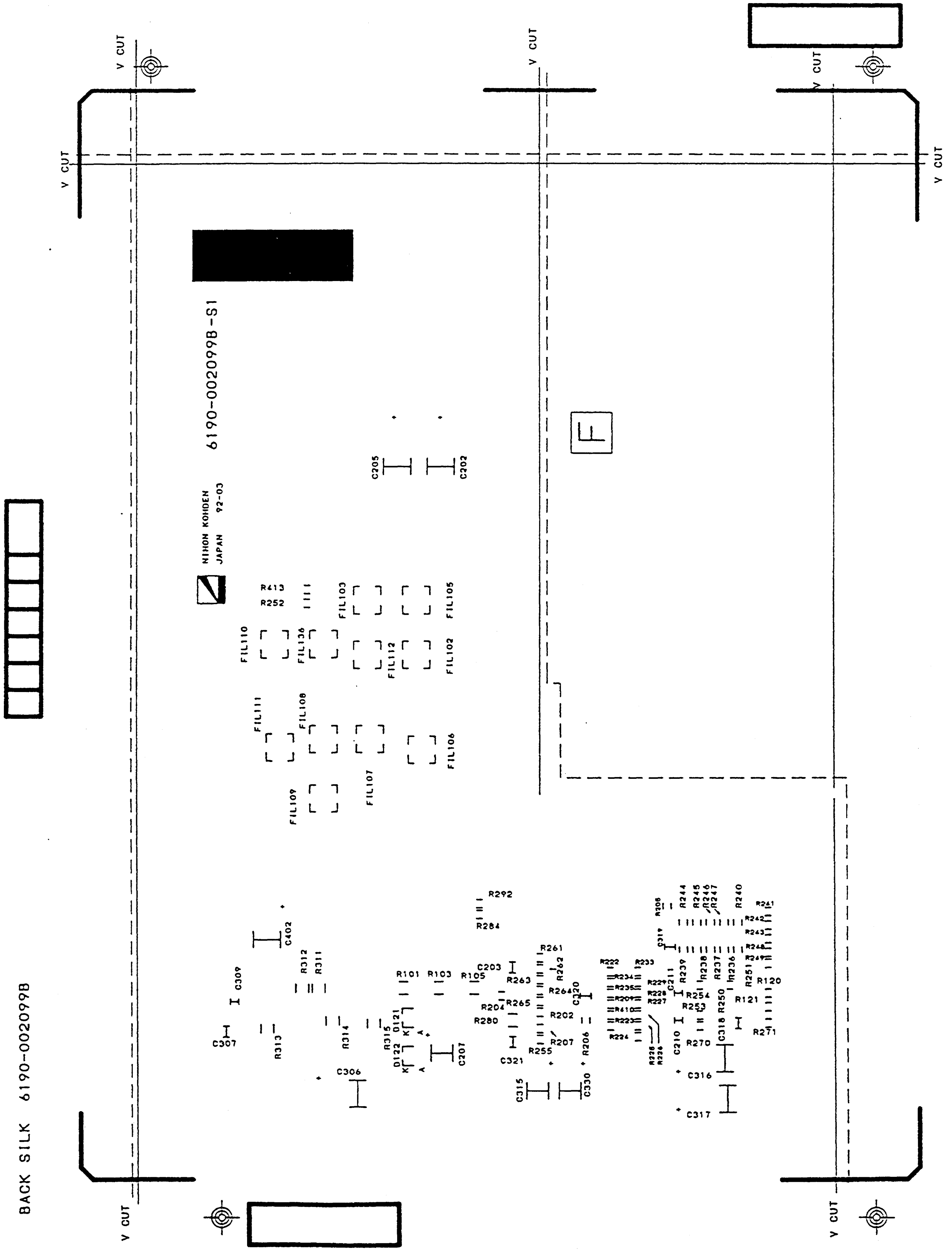
CN103
CN104
CN105
CN106
CN107
CN108
IC101
IC104
IC201
IC202
IC203
IC204
IC205
IC206
IC301
IC302
IC303
IC401
IC402
IC403
IC404
RY101
RY102
RY103
X101
X102
FIL101
FIL104
C304
C306
C310
C311
C312
C313
C314
C322
C323
R

13. PARTS LOCATION GUIDE

OPERATION CONTROL Board, UP-0801 (BACK)



V CUT
6190-002099B-S1
NIHON KOHDEN
JAPAN 92-03
F
C205
C202
R413
R252
FIL103
FIL105
FIL110
FIL136
FIL112
FIL102
FIL111
FIL108
FIL106
FIL107
FIL109
R292
R284
C402
R312
R311
C309
R313
C307
R314
R315
D121
D122
C306
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R103
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R255
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C315
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R250
C318
R270
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R245
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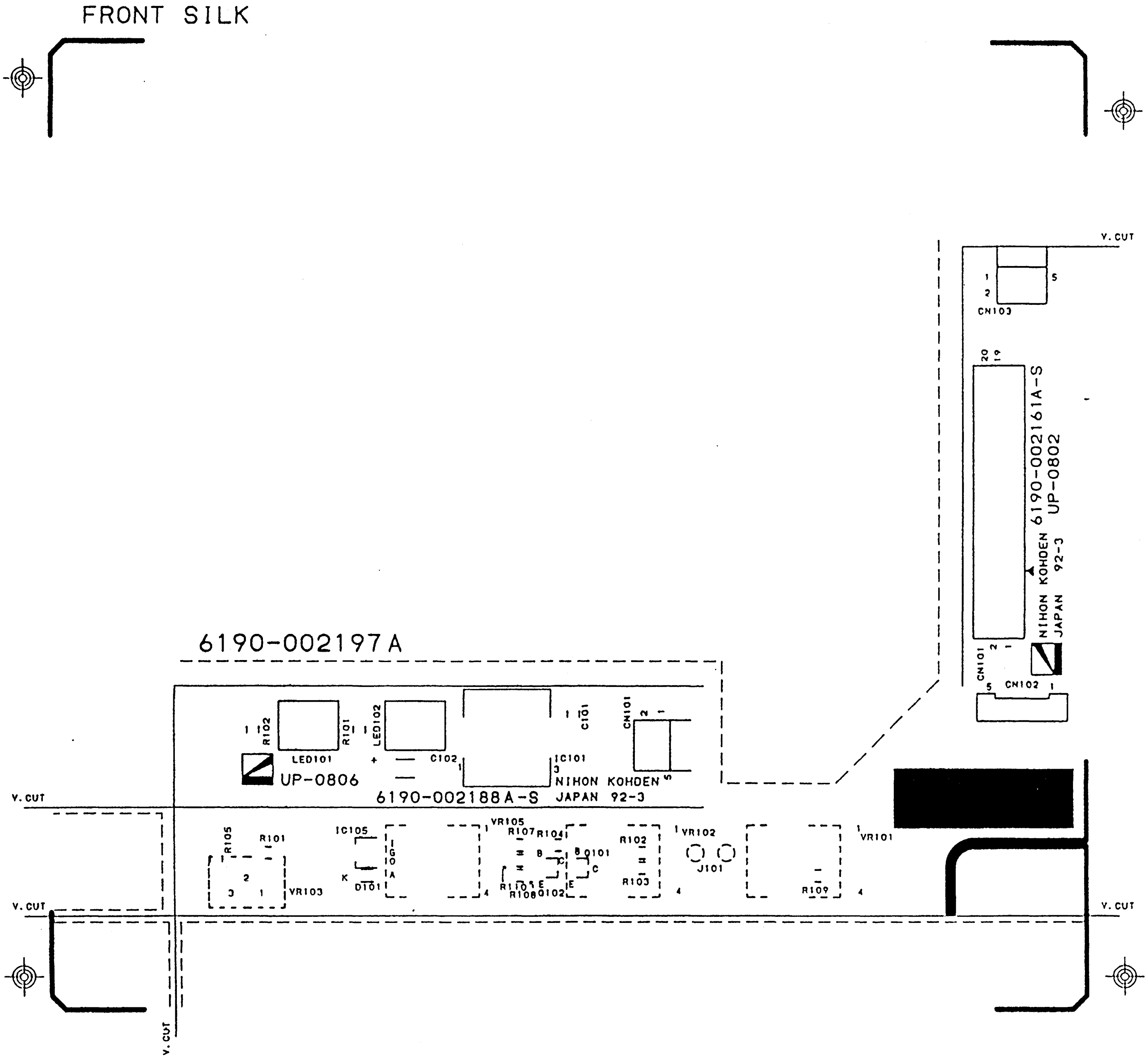
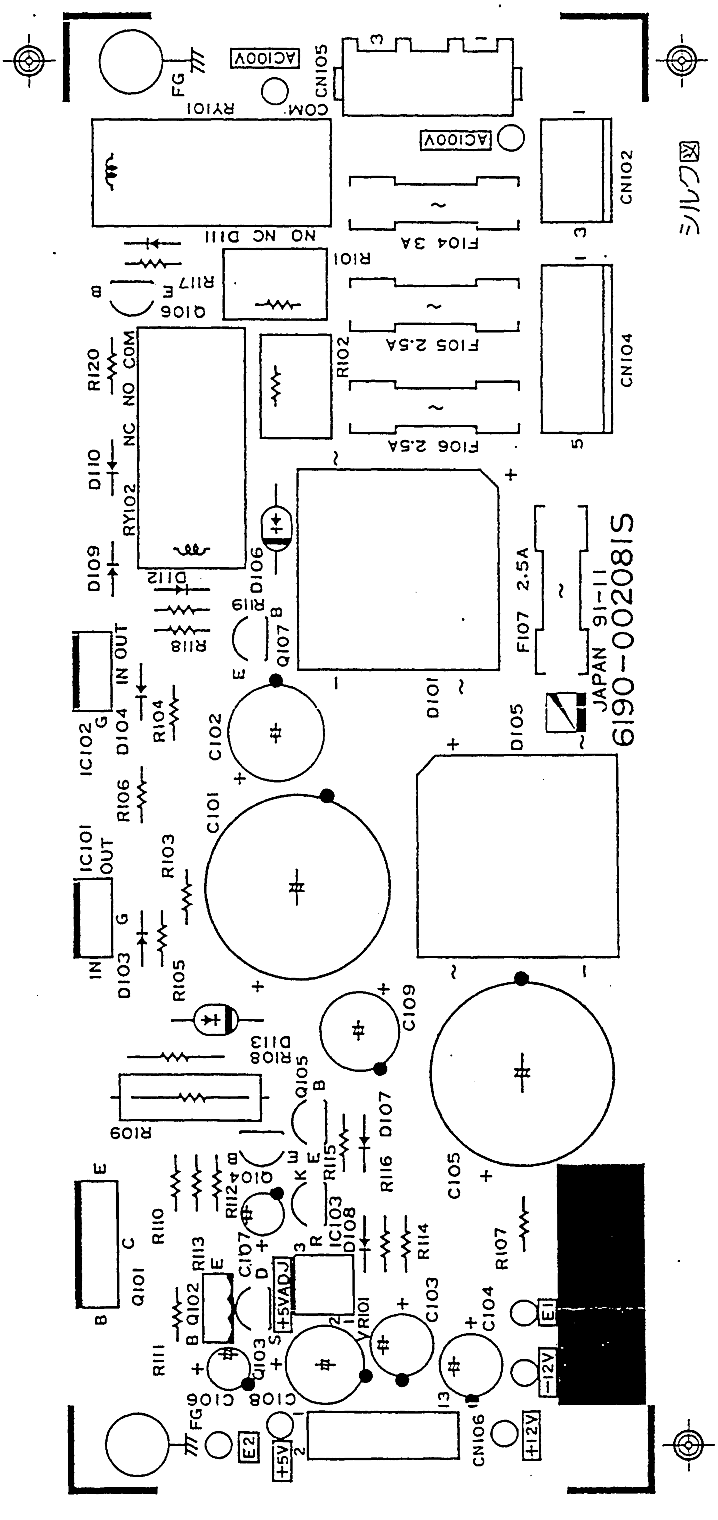
R247
R240
R241
R242
R243
R248
R249
R251
R120
R121
R271
C316
C317
BACK SILK 6190-002099B

OPERATION CONTROL (VR) BOARD, UP-0802 and LED BOARD, UP-0806,

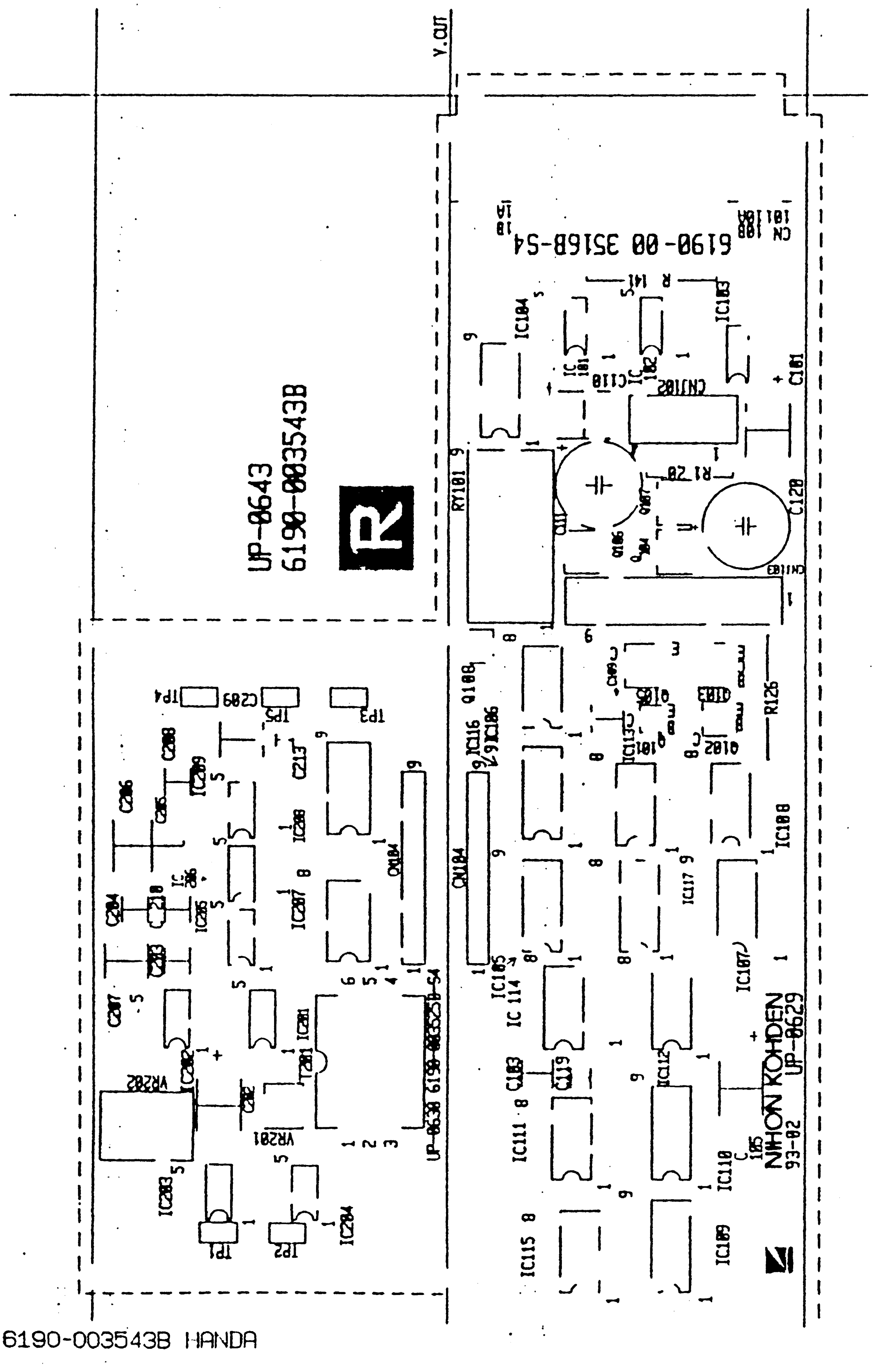

FRONT SILK
V. CUT
CN103
1
2
5
20
19
6190-002161A-S
UP-0802
NIHON KOHDEN
JAPAN 92-3
CN101
CN102
6190-002197A
R102
R101
LED102
LED101
C102
C101
IC101
CN101
UP-0806
NIHON KOHDEN
6190-002188A-S
JAPAN 92-3
R105
R101
VR103
IC105
D101
K
G
O
A
VR105
R107
R104
R110
R108
Q102
B
C
E
Q101
R102
R103
VR102
J101
R109
VR101

13. PARTS LOCATION GUIDE

Power Supply Unit, SC-019R


RY101
CN105
COM.
AC100V
FG
CN102
F104 3A
F105 2.5A
F106 2.5A
CN104
R101
R102
NO NC D111
Q106
R117
E
B
R120
NO COM
NC NO
D110
RY102
D109
D112
R119
R118
Q107
D106
IC102
G
D104
IN OUT
R104
C102
D101
D105
F107 2.5A
JAPAN 91-11
6190-002081S
IC101
OUT
IN
R106
R103
C101
D103
R105
D113
R108
Q105
C109
R109
Q104
D107
R116
R115
C105
Q101
R110
R112
C107
IC103
D108
R114
R107
Q102
R113
+5VADJ
VR101
C103
C104
R111
Q103
C108
C106
CN106
E1
E2
−12V
+12V
+5V
シルク図

NIBP Head Amp (AP-860PA) Main board, UP-0629, and Sub Board, UP-0630


Y.CUT
UP-0643
6190-003543B
R
6190-00 3516B-S4
RY101
C120
C101
CN102
IC103
IC104
IC101
IC102
C110
R141
Q106
Q107
CN103
R126
Q100
Q103
Q101
Q102
IC113
IC116
IC106
CN104
IC100
IC117
IC105
IC114
IC107
IC111
C103
C119
IC112
IC110
IC115
IC109
NIHON KOHDEN
UP-0629
93-02
TP1
TP2
TP3
TP4
TP5
C209
C213
C208
C206
C205
C204
C210
C203
C202
C207
IC209
IC208
IC206
IC207
IC205
IC201
IC202
IC203
IC204
VR201
VR202
T201
CN104
UP-0630 6190-003525B-S4

6190-003543B HANDA

Nihon Kohden Corporation
Head Office
31-4, Nishiochiai 1-chome, Shinjuku-ku,
Tokyo 161-8560, Japan

International Division Sales Department
Tokyo (Head Office)
Telephone: +81 (3) 5996-8036
Facsimile: +81 (3) 5996-8100

Nihon Kohden China Service Centers
上海维修站
上海市徐汇区南丹路 169 号 新旺大厦 3008 室
电话：021-6469-9016 传真：021-6486-7218

北京维修站
北京市西城区复兴门内大街 101 号
百盛大厦写字楼 第 7 层第 020B 室
电话：010-6603-7229 传真：010-6603-7216

广州维修站
广州市环市东路 371～375 号 世贸中心南塔 2516 室
电话：020-8777-9108 传真：020-8778-1882

沈阳维修站
沈阳市和平区北二马路 35 号
中国医药集团沈阳有限公司 2 楼 208 室
电话：024-2383-1147 转 315 传真：024-2383-2557

成都维修站
成都市一环路西二段 25 号 华立大厦 420 室
电话：028-773-6236 传真：028-773-6236

Nihon Kohden America, Inc
90 Icon Street, Foothill Ranch, CA 92610, USA
Telephone: +1 (949) 580-1555
Facsimile: +1 (949) 580-1550

Nihon Kohden Europe GmbH
Saalburgstraße 157, Bürohaus 1,
D-61350 Bad Homburg v.d.H., Germany
Telephone: +49 (6172) 309200
Facsimile: +49 (6172) 303611

Nihon Kohden Singapore PTE LTD
70 Shenton Way, #14-05 Marina House
Singapore 079118
Telephone:+65 224-6700
Facsimile: +65 224-6216

The model and serial number of your instrument are identified on the rear or bottom of the unit. Write the model and serial number in the spaces provided below. Whenever you call your distributor concerning this instrument, these two pieces of information should be mentioned for quick and accurate service.

Model ______________________________ Serial number __________________________

YOUR DISTRIBUTOR

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